United States District Court,
E.D. Texas, Texarkana Division.

LG ELECTRONICS, INC,
Plaintiff.
v.
HITACHI, LTD., et al,
Defendants.

Civil Action No. 5:07-CV-90 (DF)

Dec. 8, 2008.

Background: Holder of patents relating to digital display systems brought action against competitor, alleging infringement.

Holdings: The District Court, Folsom, J., held that:
(1) terms relating to patent for automated flat-panel display control system would be construed, and
(2) limitations relating to patent would be construed.

So ordered.

6,404,418. Cited.

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CLAIM CONSTRUCTION ORDER (4 OF 4) REGARDING U.S. PATENT NO. 5,790,096

DAVID FOLSOM**, District Judge.**

Table of Contents

I. Introduction

Please see Dkt. No. 90 for the claim-construction introduction and claim-construction legal principles. This order construes the fourth of four asserted patents. For brevity purposes, the introductory material and legal principles are included only in the first order, which construes the disputed terms of U.S. Patent No. 6,404,418.

II. U.S. Patent No. 5,790,096

The '096 Patent, entitled "Automated Flat Panel Display Control System for Accomodating Broad Range of Video Types and Formats," issued on August 4, 1998 to Jaques R. Hill, Jr., from Application No. 707,338, filed on September 3, 1996. The '096 Patent has apparently been acquired by LG.

A. Overview

The '096 Patent "relates generally to flat panel display control systems, and more specifically to electronic control systems for accepting video signals of numerous formats and types, and for displaying such video signals on a wide variety of flat panel displays." '096 Patent, col. 1, lines 8-12. According to the abstract:

An electronics control system for full color and monochrome flat panel displays which automatically accommodates video signals of numerous types and formats, whether interlaced, non-interlaced, composite, or video signals with separated sync signals. Display of such video signals on a wide selection of flat panel display systems also is accommodated. Incoming and output video rates are asynchronous. Plug-in modules allow the system to convert video signals of numerous types and modes for display on any flat panel display

system. Images are both automatically, and under user control, up-sized and down-sized, positioned and oriented to fit the flat panel display being used. Color images are automatically reduced to grey scale monochrome when a monochrome flat panel display is being used. Push-pull A/D converter circuitry for digitizing color video signals is used to reduce cost while conserving power. A further power saving feature provides for automatic power down when video reception is interrupted, and power up when the video reception is reacquired.

1. Background

The '096 Patent cites numerous patents in explaining that the "use of flat panel displays" was "well known," and that various "electronic control systems for flat panel displays" could (1) "accommodate either interlaced or non-interlaced video signals, and * * * separate out horizontal and vertical sync signals from a video signal," (2) "up-size a video image to fit a particular display, or center a small image within a larger screen," but not "perform [ ] sizing by varying the video rate as the video data is being stored," resulting in "lost" "pixel data" and "compromised" "image resolution," (3) "perform[ ] upsizing only, and * * * not accommodate down sizing," (4) "only center[ ] an image in accordance with a table look-up of fixed data," (5) "accommodate color to color, and color to monochrome processing of video signals," (6) "use[ ] a color palette in supplying color signals to a computer CRT," but not "support NTSC, PAL or HDTV video formats," (7) perform "character conversion only," but not "color to monochrome conversions for graphics," (8) "accommodate one or more of PAL, HDTV, NTSC, and VGA RGB video signals in driving the display," (9) "automatically turn[ ] off a back light when video signals are not being received," but apparently not "turn[ ] the power back on when video signals reappear, or [provide] a power conserving sequencing system," (10) "exercis[e] pixel by pixel control to achieve high resolution displays of images," and (11) "automatically detect video formats and provide asynchronous video input and output," but not perform "asynchronous operation." The '096 Patent also cites another patent that "refers to and claims a color to grey scale conversion," but "fails to disclose how such a conversion is accomplished" and a patent that "discloses a portable computer system for plugging a number of displays into a same electronics board connector" but "cannot support NTSC, PAL or HDTV systems." '096 Patent, col. 1, line 15-col. 2, line 3.

2. Disclosure

The '096 Patent is said to disclose an "electronic control system" "which automatically identifies video signal type, format, and resolution, and adapts the video image for display on a wide variety of full color and monochrome flat panel display systems." '096 Patent, col. 2, lines 28-31. According to the '096 Patent:

In accordance with the invention, images on a flat panel display may be upsized, downsized, positioned and oriented automatically or through use of user controls. Further, monochrome to color, color to monochrome, color to color, and monochrome to monochrome video processing is accommodated. Still further, power to the electronic control system is sequentially turned on and off for power conservation as video appears, disappears, and reappears.

In addition, in accordance with the invention, video data may be received at the video rate and asynchronously output to a flat panel display at the display rate without any loss of resolution. Further, both video formats and types are automatically detected.

The present invention also provides plug-in modules for an input video connector at which video is received, for color frame buffers where image content is stored, and for a flat panel interface module to which a flat panel display attaches. All known flat panel displays, and video formats and types for flat panel

displays may be accommodated without compromising power conservation. The above and other aspects of the invention are summarized below.

'096 Patent, col. 2, lines 4-24.

A "functional block diagram of an electronic control system" is illustrated in Figure 1 of the '096 Patent:

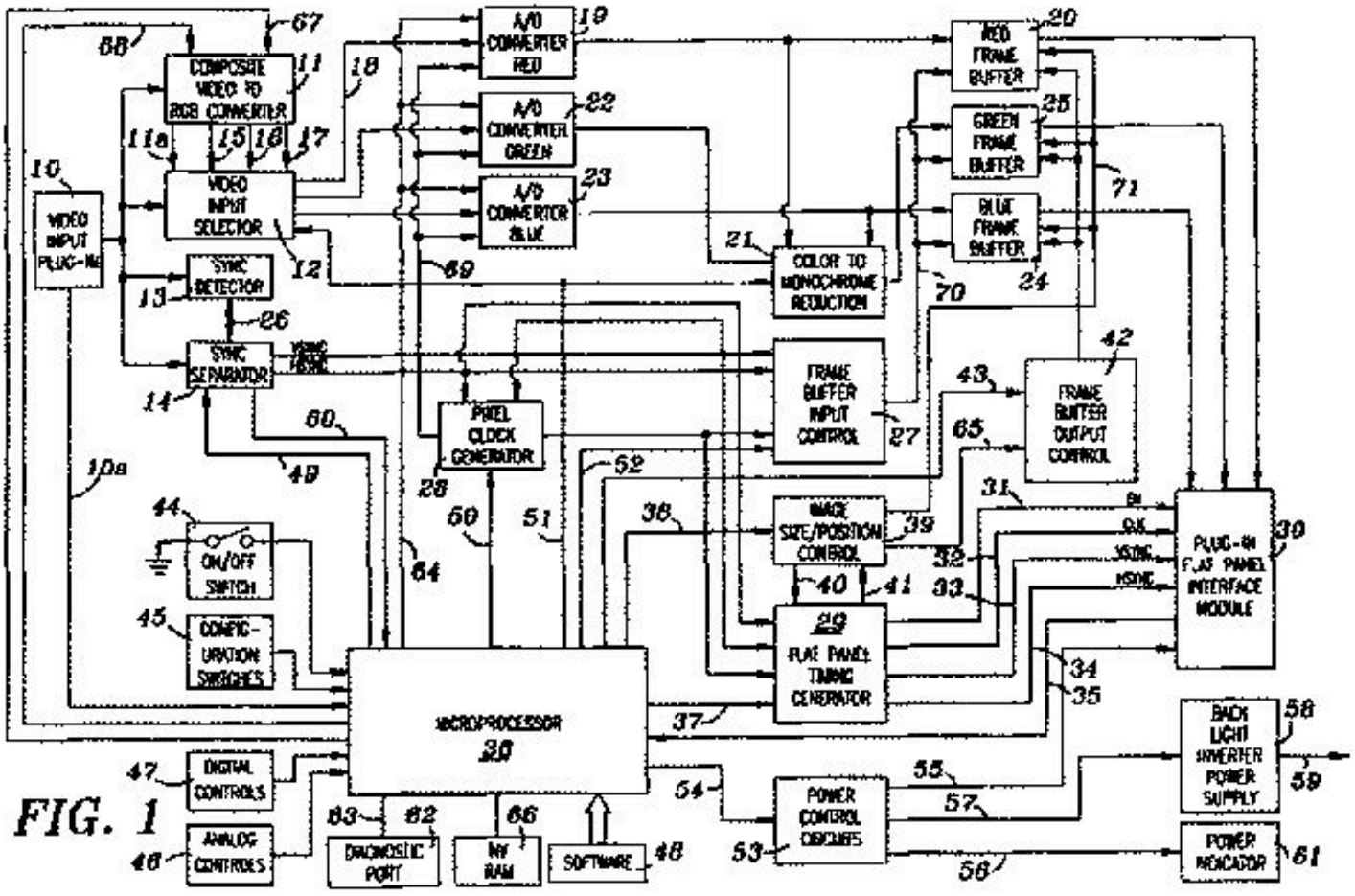


FIG. 1

The '096 Patent describes the function of each component in some detail (including "logic schematic diagrams" of various components), and explains that the "electronic control system of Fig. 1 is comprised of both off-the-shelf commercial devices and customized devices," and "is a versatile system which may adapt to any format, and which is able to accommodate video resolutions up to at least 2048x2048 (rowsxcolumns)." '096 Patent, col. 13, lines 23-29. According to the '096 Patent, "[i]n operation, the microprocessor 36 controls all functions in the electronic control system of Fig. 1. By way of example, the microprocessor manages the power operation of the electronic control system, identifies the modes of the incoming video (interlace, non-interlace, resolution, type), measures the video signal timing parameters, controls the image size, position, orientation, focus and contrast, controls the timing of the electronic control system and flat panel display, controls backlight intensity, and controls color/monochrome transition processes." ' 096 Patent, col. 11, lines 40-49.

Those components and processes are discussed in more detail below as may be necessary or helpful to construe the disputed claim terms.

3. The Asserted Claims

LG asserts claim 21, which is independent and provides:

21. A system for controlling size, position and orientation of a video image presented on a flat panel display, and in electrical communication with a memory system having stored therein said video image, and receiving a video signal from a video source, which comprises:

timing control means receiving said video signal from said video source at a video signal data rate for generating therefrom enable, vertical synchronization, horizontal synchronization, and first clock signals for driving said flat panel display, generating column start, row start, column replicate, and row replicate control signals for sizing said video image while maintaining a video signal resolution, and generating first control signals for reading said video image in said memory system;

image size/position control means in electrical communication with said timing control means and responsive to said column start, row start, column replicate, and row replicate control signals and said first control signals for generating output column address control signals, output row address control signals for said memory system, and a pixel clock signal; and

frame buffer output control means in electrical communication with said timing control means, said memory system, said image size/position control means, and said flat panel display, and responsive to said pixel clock signal for reading said video image from said memory system.

'096 Patent, col. 31, line 59-col. 32, line 19.

B. Claim Construction

1. Agreed Terms

The parties agree to constructions for the following terms:

Claim Term	***Agreed Construction***
"generating therefrom"	Generating from said video signal.

See Dkt. No. 64, at 27.

2. Disputed Terms

a) "orientation"

The term appears in the preamble of claim 21 (the disputed term is in boldface):

21. A system for controlling size, position and **orientation** of a video image presented on a flat panel display, and in electrical communication with a memory system having stored therein said video image, and

receiving a video signal from a video source, which comprises: * * * *

'096 Patent, col. 31, line 59-col. 32, line 19 (emphasis added).

(1) The Parties' Positions

The parties propose the following constructions:

LG	***Hitachi***
The extent to which a display is rotated or flipped.	The state of said video image describing whether it has been rotated 90 degrees, 180 degrees, or mirrored.

See Dkt. No. 64, at 23.

According to LG, this word is "straightforward." Dkt. No. 47, at 44. LG urges that the specification "provides a broad recitation of the manner in which an image may be displayed on a flat panel," namely, (1) "[t]he specification describes a system to permit adjustment of the way in which a visual representation of a video image is presented on a flat panel display, including controlling the size (how large the image appears), position (location of the image as presented), and orientation (extent to which the image is rotated or flipped)," and (2) Figures 12(a)-12(e) illustrate that "[a]n image may be 'normal' (250), rotated (253 or 254), flipped and rotated (251), and flipped so as to form a mirror image (252)." *Id*. at 44-45. LG contends "[t]he various 'orientations' shown in Figure 12 are simply examples of the claimed 'orientation' and the claim should not be limited to any particular orientation as urged by Defendants." *Id*. at 45. LG also argues that its proposed construction is "further supported by the common definition from extrinsic sources," i.e., dictionaries. *Id*.

Hitachi responds that the "specification discloses circuitry with a very limited ability to rotate/orient images by altering the order in which image pixel data is read from memory." Dkt. No. 48, at 15. Hitachi points to the specification at column 8, lines 57-64 in urging that "[t]he only ***possible*** orientations are 90 degrees, 180 degrees, or mirrored:"

The order in which data is read out of the frame buffers determines the form in which the image will be presented on the flat panel display screen. A timing signal that controls the reading of data from the frame buffer memory is output by control unit 39 to control unit 42 on line 65. The different *possible* presentation forms are described in more detail below in connection with the description of FIG. 12.

Id. at 15. Hitachi notes that "Figure 12 of the patent shows only 90 degree, 180 degree, and mirrored orientations" and cites column 9, lines 3-7, in arguing that "***only*** these transformations are possible with the disclosed circuitry:"

By reversing the order of reading frame buffer rows and columns, a video image may be presented in portrait form. *That is, rotated by ninety degrees*. Further, by reading the columns from the right-most to the left-most column, the image can be presented in *mirror-image* form.

Id. at 15. Hitachi contends LG's "proposed construction would allow for orientations at any angle from 0 to 360 (deg.)," which would be "impossible with the disclosed circuitry [because] the specification neither describes nor enables such orientations." *Id*. at 15-16. Under LG's construction, Hitachi urges, "claim 21 is invalid under Section 101 (lack of utility as non-operational) and Section 112, para. 1 (as both not described

and not enabled)." *Id*. at 16. Finally, Hitachi argues that LG's "reliance on common English dictionary definitions is inappropriate * * * because the limited disclosure in the specification does not support a broad, general-purpose definition of 'orientation.' " *Id*. at 16.

LG replies that Hitachi is "attempting to limit [its] construction to the disclosed embodiment in the '096 Patent," which is impermissible because "there is no language in claim 21 to limit the term 'orientation' * * * [and] a review of the other claims of the '096 patent confirms this." Dkt. No. 55, at 38. LG notes that "independent claim 27 recites 'orienting said display image,' while dependent claim 28 recites 'wherein said display image is one or more of an upside down image form, a portrait image form, a mirror-image form, and a rotated image form.' " *Id*. LG concludes that "the 'orientation' set forth in independent claim 27 is presumed to be of broader scope than that disclosed in dependent claim 28 and terms should be construed consistently among the claims." Dkt. No. 55, at 38, *citing* Acumed L.L.C. v. Stryker Corp., 483 F.3d 800, 806 (Fed.Cir.2007); Rexnord Corp. v. Laitram Corp., 274 F.3d 1336, 1342 (Fed.Cir.2001).

Finally, LG argues that Hitachi's proposed construction "would exclude one of the forms-namely, the 'NORMAL' orientation labeled as Fig. 12a-of the very embodiment that [Hitachi] cite[s] as support." Dkt. No. 55, at 38. LG asserts that its own proposed construction "encompasses the presentation forms shown in Figure 12 (namely 0, 90, 180, and 270 degrees and mirror-image) and comports with the ordinary meaning of the term." *Id*. at 39.

(2) Construction

[1] The non-asserted claims use this term in much the same way as asserted claim 21, *i.e.*, to describe the appearance of a "video image." Overall, though, the claim language provides little guidance regarding the meaning of "orientation," beyond distinguishing other characteristics of "video image" appearance, namely, size and position.

It is clear from the claims and specification, however, that "size, position and orientation" refer to how a video image is presented on a video display. What "orientation" means is more clear when discussed with "size" and "position." According to the specification, "size" refers to just that, *i.e.*, the size of the video image on the display, "position" refers to how the video image fits on the video display, and "orientation" refers to the direction of the video image on the display.

For example, with respect to sizing, the specification explains that "the video image may be up-sized or down-sized." '096 Patent, col. 2, lines 48-49; *see* id. at col. 9, lines 16-19 ("For example, in order to *stretch or zoom an image horizontally,* the control unit 42 will repeat a column address as often as required to achieve the desired horizontal stretching." (emphasis added)); col. 9, lines 12-20 ("In addition to controlling the reading of video data out of the frame buffers to achieve the above video presentations, the control unit 42 also addresses the frame buffer memory locations in a manner to *up-size or down-size an image on the display screen*. In the case of *vertical stretching or zooming,* a row address is repeated in like manner." (emphasis added)); col. 25, lines 33-40 ("The remaining switch pairs operate similarly, with switches 324 and 325 controlling the movement of the video image to the left or to the right, switches 326 and 327 controlling the movement of the video image up or down, *switches 328 and 329 controlling the horizontal expansion or contraction of the video image, and the switches 330 and 331 controlling the vertical expansion or contraction of the video image* ." (emphasis added)); and col. 9, lines 21-24 ("The *up and down sizing* is independent of whether the image output is being presented 'normally', upside-down, mirrored, in portrait form (left or right), or in any other presentation form." (emphasis added)).

With respect to positioning, the specification explains that "the image can be positioned left-to-right, right-to-left, or up or down" so as to "center the video image on the display screen." '096 Patent, col. 9, lines 30-31, 66-67; *see* id. at col. 14, line 63-col. 15, line 2 ("More particularly, at logic step 101, the pixel clock generator 28 is programmed to assume a 640 column video signal, the counters of the frame buffer input control unit 27 and the frame buffer output control unit 42 are set to zero, and the image size/position control unit 39 is *programmed to accom-modate a 1-to-1 sized image positioned in the upper left image corner at row 0 and column 0*." (emphasis added)); col. 25, lines 33-40 ("The remaining switch pairs operate similarly, with *switches 324 and 325 controlling the movement of the video image to the left or to the right, switches 326 and 327 controlling the movement of the video image up or down,* switches 328 and 329 controlling the horizontal expansion or contraction of the video image, and the switches 330 and 331 controlling the vertical expansion or contraction of the video image." (emphasis added)).

With respect to orientation, the specification explains that "the video image may be rotated in 90 (deg.) increments for presentation in portrait form, or rotated 180 (deg.) to accommodate LCD displays with different optical vertical viewing cycles, or presented in mirror-image form for use in overhead projection systems." '096 Patent, col. 2, lines 53-57. The specification provides in Figure 12, "a graphic illustration of the variety of image presentations that are provided by the electronic control system." '096 Patent, col. 24, lines 42-44.

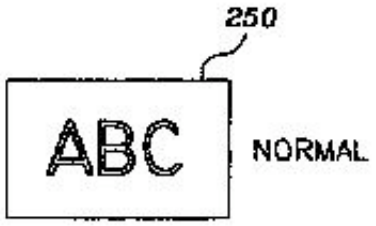


FIG. 12a

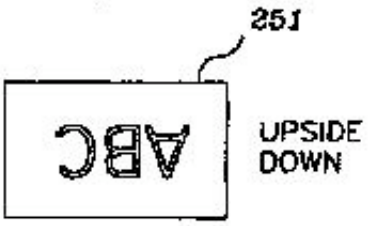


FIG. 12b

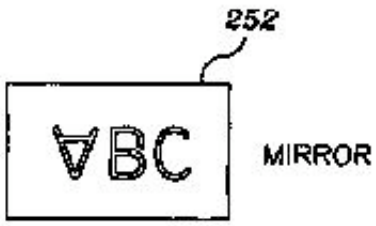


FIG. 12c

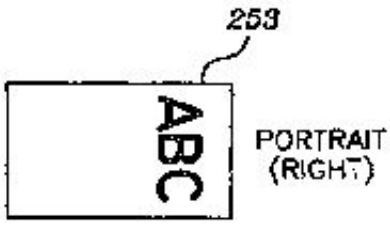


FIG. 12d

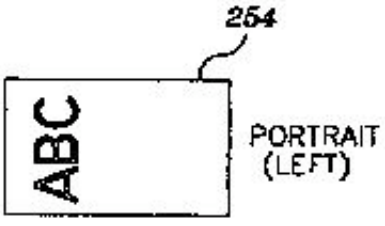


FIG. 12e

According to the specification, "[p]resentation 250 shows a straight up and down image, while presentation 251 presents an upside down image. Further, presentation 252 shows a mirror image. The above described portrait images are shown in presentations 253 and 254 as respectively a portrait right image and a portrait left image." '096 Patent, col. 24, lines 44-49.

For example, the specification explains, a "video image" may be "displayed upside down on the display screen." Apparently, "[t]his form of display is particularly useful with LCD displays that have a vertical viewing angle that is opposite to that of the viewing angle of user. By reversing the order of reading frame buffer rows and columns, a video image may be presented in portrait form. That is, rotated by ninety degrees. Further, by reading the columns from the right-most to the left-most column, the image can be presented in mirror-image form. A mirror-image [p]resentation is especially useful in overhead projection viewing, and in other applications where the image is first viewed by the user as a reflection in a mirror as with television teleprompters." '096 Patent, col. 9, lines 1-12; *see* id. at col. 9, lines 21-24 ("The up and down sizing is independent of whether the image output is being presented 'normally', upside-down, mirrored, in portrait form (left or right), or in any other presentation form.").

Thus, as the parties note, video image orientation refers to the degree of rotation of the video image, or how the video image is mirrored. The dispute appears to concern whether the claim is limited to the 90 (deg.) or 180 (deg.) orientations and mirroring disclosed in the specification, *e.g.,* those of Figure 12. The Court finds that it is not. One reason is because Figure 12 also discloses 0 (deg.) (normal) and 270 (deg.) orientations. Another reason is because the specification describes those orientations as "possible" orientations. See '096 Patent, col. 8, lines 62-64 ("The *different possible presentation forms* are described in more detail below in connection with the description of FIG. 12 [a "preferred embodiment."]) (emphasis added); '096 Patent, col. 3, lines 30-35 ("The accompanying drawings, which are incorporated in and constitute a part of the specification, illustrate a *preferred embodiment* of the invention, and together with the general description given above and the detailed description of the *preferred embodiment* given below, serve to explain the principles of the invention.") (emphasis added); '096 Patent, col. 28, lines 31-40 ("The invention has been described and shown with reference to particular embodiments, but variations within the spirit and scope of the general inventive concept will be apparent by those skilled in the art. Accordingly, it should be clearly understood that the form of the invention as described and depicted in the specification and drawings is illustrative only, and is not intended to limit the scope of the invention. All changes which come within the meaning and range of the equivalence of the claims are therefore intended to be embraced therein.").

Hitachi urges that "orientations at any angle from 0 to 360 (deg.)" are "impossible with the disclosed circuitry." According to Hitachi, LG's proposed construction would render the claim as lacking utility under s. 101 or invalid under s. 112(1) as both not appropriately supported by the written description and not enabled. Presumably, Hitachi refers to angles other than the 0 (deg.), 90 (deg.), 180 (deg.) and 270 (deg.) angles disclosed in the specification. Regardless, Hitachi provides no support for the assertion, whether from intrinsic or extrinsic evidence. *See* Talbert Fuel Sys. Patents Co. v. Unocal Corp., 275 F.3d 1371, 1376 (Fed.Cir.2002) ("We agree that a construction that renders the claimed invention inoperable should be viewed with extreme skepticism. However, Talbert did not demonstrate inoperability or provide any basis for judicially interpreting the claim to adjust the temperature range that Talbert states is the inoperable limitation." (citation omitted)). In any event, "[c]onstruction of the claims here is not so difficult a problem as to require resort to the validity maxim." MBO Labs., Inc. v. Becton, Dickinson & Co., 474 F.3d 1323, 1332 (Fed.Cir.2007) ("[V]alidity construction should be used as a last resort, not a first principle * * *.").

Thus, the Court construes "orientation" to mean "the extent to which a display is rotated or flipped."

b) "video image"

This phrase appears in claim 21 (the disputed term is in boldface):

21. A system for controlling size, position and orientation of a **video image** presented on a flat panel display, and in electrical communication with a memory system having stored therein said video image, and receiving a video signal from a video source, which comprises:

timing control means receiving said video signal from said video source at a video signal data rate for generating therefrom enable, vertical synchronization, horizontal synchronization, and first clock signals for driving said flat panel display, generating column start, row start, column replicate, and row replicate control signals for sizing said **video image** while maintaining a video signal resolution, and generating first control signals for reading said **video image** in said memory system;

image size/position control means * * *; and

frame buffer output control means in electrical communication with said timing control means, said memory system, said image size/position control means, and said flat panel display, and responsive to said pixel clock signal for reading said **video image** from said memory system.

'096 Patent, col. 31, line 59-col. 32, line 19.

(1) The Parties' Positions

The parties propose the following constructions:

LG	***Hitachi***
Data used to generate a visual representation of a video frame.	A video frame described by a set of rows and columns generated from the video signal.

See Dkt. No. 64, at 11.

LG urges the terms "video image," "video signal" and "video signal data rate" are "interrelated because the flat panel display control system of the ' 096 patent visually displays video images on a flat panel screen by storing and processing data carried on a video signal received at a data rate." Dkt. No. 47, at 46. With respect to the first term, *i.e.*, "video image," LG argues this term "clearly requires a construction that includes a video image stored in a memory system for later processing and presentation on a flat panel display," *i.e.*, as illustrated in Figure 12. *Id*. According to LG, Hitachi misses that "key point," which "lies at the center of the dispute." *Id*. In LG's view, "[o]f course, what is stored in a memory is data (i.e., logical 1s and 0s) that can be read by a computer system in which the memory belongs," and the "video image" "consequently must include the 'data' that can be stored or manipulated by the system." *Id*. Thus, LG contends "video image" "refers to data that is used to generate a visual representation ultimately displayed on a flat panel display." *Id*.

Hitachi responds that the patent "defines a 'video image' as '[a] set of rows (lines) and columns that describe a video image. Also referred to as a video frame.' " Dkt. No. 48, at 11 (quoting '096 Patent, col. 4, lines 31-

32). Hitachi further asserts that "this term is important to claim 21 because the claim has several other limitations directed to 'said video image,' including: * * * 'a memory system having stored therein ***said video image;***' 'for sizing ***said video image;***' 'for reading ***said video image*** in said memory system;' and 'reading ***said video image*** from said memory system.' " Id. Hitachi urges that "[t]he difference between 'a' and 'said' in [LG's] proposed construction is significant, because it improperly broadens the claim" and that " 'said video image' means 'the same video image' not just 'a video image.' " Id.

Hitachi states that LG "hopes to argue that the rest of the claim need not deal with the ***same*** 'said video image,' so long as some of the 'data used to generate' the image (*i.e.,* only part of the image, or even part of the data in some manipulated or altered form) satisfies the remainder of the claim." Dkt. No. 48, at 12. Hitachi argues, however, that "the same 'said video image' must satisfy all the requirements of claim 21" and further urges that its "proposed construction defines the video image to be a video frame, consistent with the rest of claim 21 because the same video image is used throughout the claim." *Id.*

Hitachi contends that "[u]nder [LG's] construction, every electronic signal disclosed in the '096 patent is a 'video image,' as all signals, in some way or another, could be argued to be 'used' to generate the eventual and ultimate result of the display of a video frame." Dkt. No. 48, at 12 n. 10. Hitachi asserts, "[t]his is too broad and not supported by the clear language of the specification" and "the issue is whether the video image is exactly that (the image itself), as opposed to (a) merely a subset of some (but not necessarily all) of the complete set of image data, or (b) some other data that is not the image itself, but that is merely used 'to generate a video frame.' " *Id.* Hitachi concludes that LG's "broad construction contradicts the remainder of claim 21 by opening the door to something other than 'said video image.' " *Id.* Finally, Hitachi argues that its "proposed construction also includes the requirement that the video image is 'generated from the video signal,' " as described in the '096 Patent specification at column 2, lines 12-17 and 28-31. Id.

LG replies that Hitachi's "construction of 'video image' is based on a misreading of the '096 patent," which "defines a '***Frame***' (not 'video image') as 'a set of rows (lines) and columns that describe a video image. Also referred to as a video frame." Dkt. No. 55, at 39. LG urges that "a 'video frame' can describe a video image; thus, the video frame contains data that is used to generate a visual representation of the video image." *Id* . LG also argues that "[t]he specification, including Figures 3a and 3b (*e.g.,* the 'image content' signals), of the '096 patent further support [LG's] construction that 'video image' is a 'visual representation' of the ***data*** in a video signal." Id.

LG characterizes Hitachi's construction as "nonsensical" because it "excludes the embodiment of the invention disclosed in the '096 patent, and even contradicts their own description of the claim." Dkt. No. 55, at 39. Specifically, LG urges that Hitachi's construction, "which [Hitachi] admit[s] cannot be 'merely a subset of some (but not necessarily all) of the complete set of image data'-precludes these very aspects of the invention, because, for example, by down-sizing the video image, the device necessarily presents a subset of the image data (by removing portions of the image to shrink it)." *Id.* at 40.

With respect to Hitachi's "a video image" and "said video image" argument, LG "agrees that the term 'said video image' needs to be used consistently through the claim," and contends "this is the reason why the term 'video image' should be construed to be 'data used to generate a visual representation of a video frame.' " *Id.*

Finally, LG argues that "Claim 21 requires that the element satisfying the 'video image' limitation be 'presented on a flat panel display' (Col.31:60), 'stored' in 'a memory system' (Col.31:61-62), 'siz[ed]' when presented on the flat panel display (Col.32:3), and 'read[ ]' from 'said memory system' (Col. 32:5-6 & 18-

19) ." LG further argues that "[o]nly [its] proposed construction satisfies these limitations, because 'data' is what is stored and read from the claimed memory system and presented and sized on the flat panel display to provide the video image viewed by the user." Dkt. No. 55, at 40. LG also contends that its "construction is not 'too broad' *-*-* because it is expressly limited to data that is used to create the visual representation of a video frame." *Id*.

(2) Construction

[2] Turning first to the language of the claim at issue, claim 21, FN1 the preamble makes a number of things clear:

FN1. Of the other claims of the '096 Patent, only claim 3 recites a "video image," and does so only once, *i.e.*, in the context of a "image size/position control means in electrical communication with said microprocessor means, said frame buffer means, and said flat panel timing generator means for generating image control signals to control size, position and orientation of a *video image* presented on said flat panel display." (emphasis added)

21. A system [1] for controlling size, position and orientation of a video image presented on a flat panel display, and [2] in electrical communication with a memory system having stored therein said video image, and [3] receiving a video signal from a video source, which comprises: * * *
'096 Patent, col. 31, line 59-col. 32, line 19 (numbering added). Thus, the "video image" may have a "size, position and orientation." The "video image" may be stored in, and may be read in and from, "a memory system," which supports the "data" aspect of LG's proposed construction. Also, a "video image" is not the same thing as a "video signal."
The body of claim 21 further makes clear that the "video image" is subject to "sizing" by "column start, row start, column replicate, and row replicate control signals," is read in memory by "first control signals," and is read out of memory by a "frame buffer output control means." This language seemingly supports Hitachi's proposed construction.

The focus thus turns to the specification, which provides the following defined terms:

Video Line: A horizontal video line also referred to as a row or video row.

Frame: A set of rows (lines) and columns that describe a video image. Also referred to as a video frame.

Interlace: Interlaced video is where a first frame of video contains only the odd rows (video lines), e.g., 1, 3, 5, etc., and the second frame of video contains only the even rows (video lines), e.g., 2, 4, 6, etc. Interlaced video requires two complete frames of video to completely describe an image.

'096 Patent, col. 4, lines 29-38. According to these definitions, a video image is ultimately made up of rows and columns. These rows and columns may be arranged in one (non-interlaced) or more (interlaced) sets, called video frames. *See also* '096 Patent, col. 2, lines 40-44 ("[T]he microprocessor of the electronic control system can automatically detect and accommodate a change in format, for example a change between NTSC and PAL formats, and determine whether a video image is interlaced or non-interlaced."). Thus, a video image is made up of one or more video frames, which are in turn made up of rows and columns. *See also* '096 Patent, col. 21, lines 4-6 ("The latch in turn receives a count of the number of flat panel columns

in a video image from the microprocessor 36 on bus 186."); id. at col. 21, lines 11-14 ("A second input of the comparator 189 is connected to the output of a binary latch 190, which receives a count of flat panel rows in a video image on bus 191.").

But the specification also describes these columns (and presumably rows), on a more fundamental level, as data. *See* '096 Patent, col. 23, lines 31-33 ("That is, one converts odd columns while the other converts even columns of video data."). In other words, a "video image" is data that is processed to generate an on-screen video display. *See* '096 Patent, col. 8, line 65-col. 9, line 1 ("[I]f the control unit 42 reads the frame buffer video data beginning at the last line and then proceeding to the first, the video image will be displayed upside down on the display screen."); id. at col. 9, lines 12-13 ("controlling the reading of video data out of the frame buffers to achieve the above video presentations"); id. at col. 20, lines 36-44. ("[W]hen a monochrome video signal is to be displayed on a flat panel color display, green video data is fed from the green color A/D converter 22, through the color to monochrome reduction device 21 and green color frame buffer 25, to the flat panel interface module 30 of Figure 1. Thereafter, under control of the microprocessor 36, the green video data is supplied to the red, green and blue inputs of the flat panel display to have the monochrome image displayed in black and white."); id. at col. 26, lines 22-25 ("The video image data for the flat panel display appears at the output of FIFO 356. The output FIFO allows video data to continue to be supplied to the flat panel display when the memory array 355 is unavailable during write cycles."); id. at col. 27, lines 55-63 ("With the frame buffers operating in a fully asynchronous manner, video data may be read out of the frame buffers and through the output FIFO 356 to the flat panel display. During the brief 'burst write' time, the frame buffer is being written into, and therefore cannot be read. However, the output FIFO contains enough video data so that output to the flat panel display is not interrupted. The output FIFO is not filled during the frame buffer write time, but the FIFO continues to output data to the flat panel display."); id. at col. 26, line 66-col. 27, line 1 ("In operation, the microprocessor 36 programs the latches 405 and 408 with the start and stop location of the incoming video image."); id. at col. 18, lines 22-24 ("the microprocessor 36 receiving the video format or mode of the incoming video data from the video input connector 10"). *See also* '096 Patent, col. 9, lines 34-36 ("[T]he microprocessor 36 accesses application software stored in memory unit 48 to process video signals for display on the flat panel display screen (not shown)."). Thus, both parties are, in part, correct.

Nevertheless, interpreting this term at its most basic level makes the most sense in the context of the claims. Again, in claim 21, "video image" is stored in memory, and in the specification, the video image is stored in memory as data, *i.e.,* video column and line data is stored in various memory addresses. *See, e.g.,* '096 Patent, col. 9, lines 13-16 ("In addition to controlling the reading of video data out of the frame buffers to achieve the above video presentations, the control unit 42 also addresses the frame buffer memory locations in a manner to up-size or down-size an image on the display screen."); id. at col. 9, lines 26-29 ("[T]he control unit 42 also positions an image on the flat panel display screen by addressing the frame buffer memory locations commencing at any location in the memory space."); id. at col. 20, lines 61-64 ("This clock signal is the same clock signal as that used to create the flat panel timing, and also is used to create frame buffer memory addresses of output video data."). The "video image" is also sized, positioned and oriented, and the specification explains that such manipulation occurs by changing how the data is read out of memory. *See, e.g.,* '096 Patent, col. 22, lines 25-28 ("In operation, the image size/position control unit 39 provides image positioning, image size, and image orientation by modifying the memory addresses that are presented to the frame buffers 20, 24, and 25.").

The claims also indicate that the data making up the "video image," first recited in the preamble as stored in memory, are the same data that are, in the body of the claim, read in and from memory. The data may be

used more than once, of course, for up-sizing the video image to fit a screen. *See* '096 Patent, col. 9, lines 12-16 ("In addition to controlling the reading of video data out of the frame buffers to achieve the above video presentations, the control unit 42 also addresses the frame buffer memory locations in a manner to up-size or down-size an image on the display screen. For example, in order to stretch or zoom an image horizontally, the control unit 42 will repeat a column address as often as required to achieve the desired horizontal stretching. In the case of vertical stretching or zooming, a row address is repeated in like manner."). For down-sizing, the converse is true, *i.e.*, data (or a column of data) is skipped.

Also, the specification explains that if a color video image is to be displayed on a monochrome screen, some of the video image data is processed to create new weighted image data. The specification explains that "[i]f color video is to be displayed on a monochrome display, the red, blue and green video signals received by the device 21 must be reduced to monochrome video according to a weighting or color mixing standard," such as that of Table 1:

TABLE I			
NTSC	5/16	9/16	2/16
Weighting	Red	Green	Blue
Equal	5/16	6/16	5/16
Weighting	Red	Green	Blue
Green Only	0/16	16/16	0/16
	Red	Green	Blue
User	?/l6	?/16	?/l6
Defined	Red	Green	Blue

'096 Patent, col. 7, lines 20-32. *See* id. at col. 8, lines 34-36 ("The microprocessor 36 reads the configuration switches 45 to control the weighting (or mixing) of the colors by the color to monochrome reduction device 21."); id. at col. 20, lines 8-23 ("In operation, when color video information is to be displayed on a monochrome flat panel display, one of the equations set forth in Table I above is programmed by the microcontroller 36 into the color to monochrome reduction device 21, and weighting values for red, blue and green color are written by the microprocessor into the latch registers 164, 166, and 168. More particularly, latch 164 contains the weighting for the color red, latch 166 contains the weighting for the color green, and latch 168 contains the weighting for the color blue. The AND gates 163, 165 and 167 transition to a logic one level only when both a color video data signal and a weighting for that color are received. Thus, only weighted color values are allowed to pass to OR gate 169, where the color data is mixed only in the amounts indicated by the weightings. The output of OR gate 169 is one bit of monochrome grey scale."). In other words, less than all of the video image data, or further-processed data, may be used to generate a video display. Hitachi's argument that video image data cannot be "a subset of some (but not necessarily all) of the complete set of image data," must therefore be rejected. Hitachi's argument that "video image" cannot connote data that "is not the image itself, but that is merely used 'to generate a video frame,' " must similarly be rejected.

Thus, the Court construes the term "video image" to mean "data that forms a visual representation when displayed."

c) "video signal"

This phrase appears in claim 21 (the disputed term is in boldface):

21. A system for controlling size, position and orientation of a video image presented on a flat panel display, and in electrical communication with a memory system having stored therein said video image, and receiving a **video signal** from a video source, which comprises:

timing control means receiving said **video signal** from said video source at a **video signal** data rate for generating therefrom enable, vertical synchronization, horizontal synchronization, and first clock signals for driving said flat panel display, generating column start, row start, column replicate, and row replicate control signals for sizing said video image while maintaining a **video signal** resolution, and generating first control signals for reading said video image in said memory system;

image size/position control means * * *; and

frame buffer output control means * * *.

'096 Patent, col. 31, line 59-col. 32, line 19 (emphasis added).

(1) The Parties' Positions

The parties propose the following constructions:

LG	***Hitachi***
A signal containing data used to generate a visual representation of a video frame.	An electronic signal containing information specifying the location and brightness of each point on a display, along with the timing signals to place the image properly on the display. Video signal formats include VGA, SVGA, XGA, NTSC, PAL and SECUM video.

See Dkt. No. 64, at 25.

LG urges its proposed construction "to ensure consistency between construction of various terms within claim 21, and preserve the interconnection between the terms 'video image' and 'video signal' as claimed." Dkt. No. 47, at 47. According to LG, Hitachi's proposed construction "not only fails to preserve continuity among the claim terms, but also injects unnecessary confusion into a term that is otherwise well-understood." *Id*. LG urges that "including a list of specific information contained within the 'video signal,' such as 'location and brightness of each point on a display' and 'timing signals to place the image properly on the display' will not assist the finder of fact in understanding this relatively simple term, and such limitations are not requirements of the clear language." *Id*.

Hitachi urges that "[t]he specification defines a 'video signal' as including 'formats and types' * * * and further defines a 'video format' as a signal including timing and brightness signals:

Video Format (Modes): The timing characteristics of a video type including number of rows and columns, frames per second, and whether the video lines are interlaced or noninterlaced. Formats for composite video include (i) NTSC11 (National Television Standards Committee) with 525 lines of video interlaced at 60 Hz, (ii) PAL (Phase Alternating Line) with 625 lines of video interlaced at 50 Hz, (iii) HDTV (High Definition Television) which currently has no universally accepted format but as used herein has 1125 lines of video at 100 Hz, and (iv) numerous variations of NTSC and PAL. Formats for component video include (i) RGB (sync on green) in NTSC, PAL or other video format; (ii) RGB (sync on green) in non-interlaced format at

different numbers of lines and columns; (iii) VGA with 640 x 480 non-interlaced video at 60 Hz, 720 x 400 non-interlaced video at 60 Hz, and 640 x 350 non-interlaced video at 60 Hz, (iv) SVGA with 800 x 600 non-interlaced video, (v) XGA with 1024 x 768 non-interlaced video, and (vi) SXGA with 1280 x 1024 non-interlaced video.

Dkt. No. 48, at 13 (citing '096 Patent, col. 4, lines 45-65).

Hitachi contends "[t]he specification defines 'video type' as a signal that includes picture signals and timing signals" and cites "several examples wherein the timing signals are carried within the video signal." Dkt. No. 48, at 13. Hitachi urges that its construction "is also consistent with several technical dictionary definitions" and notes that it comports with "the only embodiment described in the '096 patent." Id. at 13-14. Finally, Hitachi asserts that LG's construction "would read on non-video signals, such as synchronization or memory read/write signals, which do not contain the actual video data, but which are only used (in some unspecified way) to generate a displayed frame." Id. at 14.

In response, LG argues that Hitachi's "attempt to shoehorn the definitions of other phrases-namely, 'Video Type' and 'Video Format'-into the 'video signal' claim term should be rejected [because] [n]either the claim nor the specification requires such limits on the 'video signal' claim term." Dkt. No. 55, at 41. LG notes that "in the 'Video Format' section of the specification quoted by [Hitachi], the passage includes a reference to 'HDTV (High Definition Television) which ***currently has no universally accepted format*** but as used herein has 1125 lines of video at 100 Hz ...' " *Id*. LG argues that Hitachi failed "to include 'HDTV in its proposed construction even though the specification discloses that such signals can be accepted by the claimed system in Table VI." *Id*. Finally, LG urges that its construction does not read on non-video signals because it "is expressly directed to video signals by requiring such signals to contain 'data used to generate a visual representation of a video frame'- *i.e.*, a signal containing a 'video image.' " *Id*.

(2) Construction

[3] In claim 21, the "video signal" is received by the "system" from a "video source" "at a video signal data rate." The claim language provides no additional guidance in construing this term.

The specification explains that "[t]he invention relates generally to flat panel display control systems, and more specifically to electronic control systems for accepting video signals of numerous formats and types, and for displaying such video signals on a wide variety of flat panel displays." ' 096 Patent, col. 1, lines 8-12. Hitachi views this language as defining a "video signal" in terms of formats and types, thus invoking various limitations from the specification-defined term "video format:"

Video Format (Modes): The timing characteristics of a video type including number of rows and columns, frames per second, and whether the video lines are interlaced or non-interlaced. Formats for composite video include (i) NTSC (National Television Standards Committee) with 525 lines of video interlaced at 60 Hz, (ii) PAL (Phase Alternating Line) with 625 lines of video interlaced at 50 Hz, (iii) HDTV (High Definition Television) which currently has no universally accepted format but as used herein has 1125 lines of video at 100 Hz, and (iv) numerous variations of NTSC and PAL. Formats for component video include (i) RGB (sync on green) in NTSC, PAL or other video format; (ii) RGB (sync on green) in non-interlaced format at different numbers of lines and columns; (iii) VGA with 640x480 non-interlaced video at 60 Hz, 720x400 non-interlaced video at 60 Hz, and 640x350 non-interlaced video at 60 Hz, (iv) SVGA with 800x600 non-interlaced video, (v) XGA with 1024x768 non-interlaced video, and (vi) SXGA with

1280x1024 non-interlaced video.

'096 Patent, col. 4, lines 45-65.

The specification describes many video signal aspects. *See, e.g.,* '096 Patent, col. 2, lines 28-31 ("An electronic control system is disclosed which automatically identifies video signal type, format, and resolution, and adapts the video image for display on a wide variety of full color and monochrome flat panel display systems."); '096 Patent, col. 5, lines 16-17 ("a full color composite video signal"); id. at col. 5, line 64 ("analog red, green and blue video signals"); id. at col. 6, lines 22-23 ("identify the type of the video signal being received"), col. 10 lines 34-35 ("high rate video signals"); id. at col. 11, line 45 ("the video signal timing parameters"); id. at col. 12, lines 58-59 ("extracting synchronization signals from the incoming video signal"); id. at col. 14, lines 5-7 ("extracts the horizontal sync and vertical sync signals from the video signal"); id. at col. 11, lines 43-45 ("identifies the modes of the incoming video (interlace, non-interlace, resolution, type), measures the video signal timing parameters"); id. at col. 16, lines 19-21 ("low amplitude video signals to be digitized as if they were at full amplitude"). But these references do not define "video signal" *per se*. The claim simply recites "video signal," not "video signal format" or "video signal timing" or some other "video-signal"-related term. In short, Hitachi's argument misses the point of the video signal, namely, to carry video data.

Thus, the Court construes the term "video signal" to mean "a signal that contains data that forms a visual representation when displayed."

d) "video signal data rate"

This phrase appears in claim 21 (the disputed term is in boldface):

21. A system for controlling size, position and orientation of a video image presented on a flat panel display, * * *, which comprises:

timing control means receiving said video signal from said video source at a **video signal data rate** for generating therefrom enable, vertical synchronization, horizontal synchronization, and first clock signals for driving said flat panel display, generating column start, row start, column replicate, and row replicate control signals for sizing said video image while maintaining a video signal resolution, and generating first control signals for reading said video image in said memory system;

image size/position control means * * *; and

frame buffer output control means * * *.

'096 Patent, col. 31, line 59-col. 32, line 19 (emphasis added).

(1) The Parties' Positions

The parties propose the following constructions:

LG	***Hitachi***
The frequency of the video signal.	The frequency of the signal that carries the video data being input from the video source.

See Dkt. No. 64, at 26.

According to LG, "[t]he parties seem to agree that [this] phrase * * * is associated with a video signal frequency," but Hitachi limits the claim to being 'associated only with a "number that reflects the vertical frequency.' " Dkt. No. 47, at 47-48. In LG's view, "[t]he video signal data rate also may include other information, such as data related to frame rate, pixel rate, and bandwidth, which may be described more generally as 'frequency' information." *Id*. at 48.

In response, Hitachi altered its proposed claim construction from "the number that reflects the vertical frequency of the video signal from the video source" to the construction noted above. Dkt. No. 48, at 14. Hitachi urges that LG's "construction is vague in that it does not expressly require the 'video signal ***data*** rate' to be the frequency of the video ***data***" and may cause confusion "in the scenario in which the video signal being input from the video source includes nondata frequencies, such as timing signal frequencies." *Id*.

In response, LG notes Hitachi's altered claim construction in suggesting "that the dispute between the parties has been narrowed or eliminated." Dkt. No. 55, at 42. Regardless, LG urges that "it is clear from the plain language of the claim that the video signal is received from a video source; thus, [Hitachi's] inclusion of this phrase in its proposed construction is superfluous and would only confuse the jury." *Id*.

(2) Construction

[4] The parties' dispute appears to be resolved. Claim 21 expressly calls for the "video signal" to be "from a video source at a video signal data rate." Thus, there is no need to repeat that in construing this term. Further, it is the signal itself that is received at that rate. All the data carried by the signal are thus received at that rate, as well. In any event, Hitachi's reference to "the signal that carries the video data" is understood to refer to the claimed "video signal." Thus, there appears to be no substantive difference between the parties' positions.

The specification does not use this term, nor the term "data rate." The specification does, however, refer to a "video rate," which appears to be the same thing. *See* '096 Patent, col. 2, lines 12-15 ("[I]n accordance with the invention, video data may be received at the video rate and asynchronously output to a flat panel display at the display rate without any loss of resolution."). For example, the specification explains, that "[t]he microprocessor 36 also works in co-operation with the A/D converters 19, 22, and 23 to accommodate high rate video signals in the range of 25 to 40 MHz." ' 096 Patent, col. 10, lines 33-35. In other words, the video rate refers to the video signal frequency, as the parties urge.

Thus, the Court construes the term "video signal data rate" to mean "the frequency of the video signal."

e) "flat panel display"

This phrase appears in claim 21 (the disputed term is in boldface):

21. A system for controlling size, position and orientation of a video image presented on a **flat panel display,** and in electrical communication with a memory system having stored therein said video image, and receiving a video signal from a video source, which comprises:

timing control means receiving said video signal from said video source at a video signal data rate for generating therefrom enable, vertical synchronization, horizontal synchronization, and first clock signals for driving said **flat panel display,** generating column start, row start, column replicate, and row replicate control signals for sizing said video image while maintaining a video signal resolution, and generating first control signals for reading said video image in said memory system;

image size/position control means * * *; and

frame buffer output control means in electrical communication with said timing control means, said memory system, said image size/position control means, and said **flat panel display,** and responsive to said pixel clock signal for reading said video image from said memory system.

'096 Patent, col. 31, line 59-col. 32, line 19 (emphasis added).

(1) The Parties' Positions

The parties propose the following constructions:

LG	***Hitachi***
A display device other than a cathode-ray tube (CRT), having flat front, including liquid crystal (LCD) and plasma flat panel technology.	An electronic display with a package thickness that is a small fraction of the display's height or length.

See PR 4-5d CC at 28.

According to LG, "[t]he specification repeatedly describes the term' flat panel display' as including liquid crystal (LCD), electroluminescent, gas plasma, FED, and/or other flat panel types." Dkt. No. 47, at 48. LG also relies on dictionary definitions to support distinguishing CRT display. LG urges that the specification's reference to a CRT display is in connection with prior art, and that "use of a flat panel display rather than a CRT * * * is mandated by many of the goals of the invention." *Id*. at 50.

Hitachi argues that both parties "rely on extrinsic evidence that defines a flat panel display by the depth of the display" but that LG impermissibly "seeks to define this term by exclusion, stating that it cannot include a CRT." Dkt. No. 48, at 16. Hitachi suggests that LG's construction is really an attempt to undermine Hitachi's Rule 3 disclosures, "presumably so that LGE can argue to a jury that the Court has ***already decided*** that any distinction between a CRT and a flat panel display is significant and relevant in terms of the invalidity of claim 21." *Id*.

In response, LG argues that Hitachi ignores (1) "the express and limiting language in the preamble of the claim which recites a 'system for controlling the size, position and orientation of a video image presented ***on a flat panel display,***' " and (2) "the 'orientation' limitation in claim 21, which is clearly directed to solving problems unique to flat panel displays such as LCD displays." Dkt. No. 55, at 43. Finally, LG urges that Hitachi's "phrases 'package thickness' and 'a small fraction of are vague and undefined * * * and would unnecessarily confuse the finder of fact." *Id*.

(2) Construction

[5] The specification provides numerous examples of flat panel displays, "including LCD,

electroluminescent, gas plasma, and FED display systems." ' 096 Patent, col. 3, lines 7-8. The specification's only reference to a CRT, though, is in the Background of the Invention:

Still further, electronic control systems for flat panel displays are known which accommodate color to color, and color to monochrome processing of video signals. *See* U.S. Pat. Nos. 5,193,069; 5,293,485; and 4,922,237. While U.S. Pat. No. 5,193,069 refers to and claims a color to grey scale conversion, the patent fails to disclose how such a conversion is accomplished. U.S. Pat. No. 5,293,485 discloses a complex system which uses a color palette in supplying color signals to a *computer CRT*. The system cannot support NTSC, PAL or HDTV video formats. U.S. Pat. No. 4,922,237 discloses a character conversion only, and cannot perform color to monochrome conversions for graphics. Electronic control systems for flat panel displays also are known which accommodate one or more of PAL, HDTV, NTSC, and VGA RGB video signals in driving the display.

'096 Patent, col. 1, lines 34-48. The apparent distinction here is that a CRT cannot support certain video formats, not that CRTs are not "flat panel" displays. During prosecution, the examiner essentially repeated that in a first office action that otherwise largely concluded that the claims were allowable. *See* Dkt. No. 69, Exh. '096 Pages 51-100, at HCX AS 0015734 [Office Action of November 20, 1997] ("Zenda [U.S. Patent No. 5,293,485] discloses a complex system which uses a color palette in supplying [color] signals to a computer CRT, but the [system] does not support NTSC, PAL, or HDTV video formats."). The intrinsic record thus draws a distinction between CRTs and flat panel displays, *i.e.,* the applicant did not lump the two together. Both were known in the prior art.

In general, though, when a term is a term of art, the term is given its art-recognized meaning. Here, "flat-panel display" is a term of art. One technical reference simply defines this term as "[a]n electronic display in which a large orthogonal array of display devices, such as electroluminescent devices or light-emitting diodes, form a flat screen." McGraw-Hill Dictionary of Scientific and Technical Terms 770, 1437 (5th ed.1994), 817, 1522 (6th ed.2003). Another reference defines this term as "[a] very thin display screen used in portable computers and increasing as a replacement for a CRT with desktop computers." Random House Webster's Computer and Internet Dictionary 217 (3d ed.1999). Yet another source defines a "flat panel display" as "[a] type of display device where the depth is much less than a conventional cathode ray tube for the same image size. Various flat panel technologies, including LCDs and plasma panels are competing to produce reliable high-resolution color displays, both large and small." Dictionary of Computing 193 (4th ed.1996) (included in Dkt. No. 47, Exh. 5, at LG A-V 025317). A further reference provides the following definition for the disputed term: "An electronic display with a package thickness that is a small fraction of the display's height or length." The McGraw-Hill Illustrated Dictionary of Personal Computers 186 (4th ed.1995) (included in Dkt. No. 48, Exh. 4, at HCX AS 0192687). These definitions are consistent with how that term is used in the specification.

Thus, the Court construes the term "flat panel display" to mean "a flat electronic screen, formed from an array of display devices that use liquid crystal, electroluminescent, gas plasma, or similar technologies."

f) "column replicate control signal" & "row replicate control signal"

These phrases appear in claim 21 (the disputed phrases are in boldface):

21. A system for controlling size, position and orientation of a video image presented on a flat panel

display, * * * which comprises:

timing control means receiving said video signal from said video source at a video signal data rate for generating therefrom enable, vertical synchronization, horizontal synchronization, and first clock signals for driving said flat panel display, generating column start, row start, **column replicate,** and **row replicate control signals** for sizing said video image while maintaining a video signal resolution, and generating first control signals for reading said video image in said memory system;

image size/position control means in electrical communication with said timing control means and responsive to said column start, row start, **column replicate,** and **row replicate control signals** and said first control signals for generating output column address control signals, output row address control signals for said memory system, and a pixel clock signal; and

frame buffer output control means * * *.

'096 Patent, col. 31, line 59-col. 32, line 19 (emphasis added).

(1) The Parties' Positions

The parties propose the following constructions:

Phrase	***LG***	***Hitachi***
"column replicate control signal"	Signal that controls the number of times a particular column address identified at least in part by a column start control signal is read out of the frame buffer in order to control the size of video image on a display screen.	An electronic signal that repeats an entire column of pixels in the image.
"row replicate control signal"	Signal that controls the number of times a particular row address identified at least in part by a row start control signal is read out of the frame buffer in order to control the size of video image on a display screen.	An electronic signal that repeats an entire row of pixels in the image.

See Dkt. No. 64, at 29.

LG urges that "the dispute between the parties surrounds the nature of the claimed replicate signals and the corresponding description in the patent." Dkt. No. 47, at 50. According to LG, "the column or row of pixels in the image is not repeated, but rather, a particular column and row address is replicated." *Id*. LG contends that "[t]he specification describes that frame buffer output control unit 42 is programmed to access frame buffers 20, 24, and 25-in which a video image is stored-at a particular start column and start row memory address. In the case where no up-sizing or downsizing is to be performed prior to presenting the video image on a flat panel display, the frame buffer output control unit 42 continues reading the frame buffers according to the count up/down value." *Id*. at 51. LG urges that "the size of the video image to be displayed on the flat panel display may be changed by using horizontal and vertical replication" as "shown in Figure 8." *Id*. According to LG, "[t]he inputs to Figure 8 (i.e., image size/position control unit 39) include * * * column and row replicate values [that] are used to re-size a video image." *Id*. LG argues that "in a simple example of resizing a video image horizontally, a primary column address is determined based on the image column start value on line 203 and a clock on line 218. The primary column address is applied to one input of the adder/subtractor 205, and the column replicate value is applied to the second data input of the adder/subtractor 205. The replicate value then is added or subtracted from the primary column address as

determined by the sign of the replicate value. The resulting output of the adder/subtractor 205 is a column address which is applied to the frame buffer output control unit 42." *Id*. at 51-52. Thus, LG urges, "the column replicate value 209 represents a number of times a particular column address is read out of the frame buffer and the row replicate value 216 represents a number of times a particular row address is readout of the frame buffer," which in turn "controls the size of video image on a display screen." *Id* . at 52.

Hitachi argues that "the column replicate and row replicate signals control the number of times an ***entire*** column or row of pixels is repeated in the video image" and notes that "the only embodiment disclosed in the patent can replicate only an entire row or column of pixels, not an individual pixel or subsets of pixels within a displayed row or column." Dkt. No. 48, at 17. Hitachi also cites Figure 8, in noting that "the Column Replicate Value 209 and the Row Replicate Value 216 are values that are latched in respective Binary Latches 208 and 215 * * * [and][t]hese latched values determine how many times an entire column or row of address signals is repeated as output Column Address signals 207 and output Row Address signals 217." *Id*. Finally, Hitachi urges that LG's constructions "only refer to replication of a particular pixel at a particular row and column address, rather than a complete row or column, * * * [which] broaden[s] these terms so that they cover the situation where only a single pixel from within a row or column is replicated, but without replication of the complete row or the complete column that contains that pixel." *Id*. at 18.

In response, LG argues that the "specification does not require 'the column replicate and row replicate signals control the number of times an ***entire*** column or row of pixels is repeated in the video image' [but rather] the signals control the number of times a particular ***column address*** or ***row address*** is repeated in the video image and that the addressing can be commenced at ***any location in the memory space.***" Dkt. No. 55, at 43-44. LG urges that the example cited by Hitachi "is not discussing whether the ***entire*** row or column is repeated; instead, it is an example showing how to determine the Column Replicate or Row Replicate Factors, which merely calculate ***which*** nth row or nth column is repeated or skipped." *Id*. at 44. LG also notes that "the table above this passage clearly indicates that the start position for the row or column can fall anywhere between the ranges of 0 and 2047." *Id*.

(2) Construction

[6] [7] There is no dispute that this phrase refers to a signal; rather, the parties dispute what this signal does. The claim terms themselves suggest what they are for, *i.e*., controlling column/row replication. Those words suggest what Hitachi urges, *i .e*., that the columns and rows are replicated. According to the specification, the number of times that a column or row is repeated depends on the image size parameters set at the "image size/position control unit 39" (Figure 1). FN2

FN2. *See supra* Part II. A for a reproduction of Figure 1.

The specification explains that "a command is issued to set the stored image size and position parameters into the image size/position control unit (39) by way of line 38." The specification further provides the "parameter codes and representations" in Table X below:

TABLE X

Code	Representation	Range	Description
0	Upper Left Column Image Start Position	0000 to 2047	Upper Left Column Position For Image Start

1	Upper Left Row Image Start Position	0000 to 2047	Upper Left Row Position For Image Start
2	Column Replicate Factor	X:Y	Where X Is The Column Repeat Number. Y Is The Column Replicate Number.*
3	Row Replicate Factor	X:Y	Where X Is The Row Repeat Number. Y Is The Row Replicate Number.*

According to the specification, "[t]he rows in the above table marked with an asterisk are further explained by the following example. Where X=2 and Y=l, every row and column is repeated. Where X=l and Y=5, every fifth row and column is repeated. Further, when X=2 and Y=10, every row and column is repeated, and every tenth row and column is repeated again." '096 Patent, col. 16, lines 45-50.

According to the specification, Table XII "illustrates how the *input controls* to the image size/position control unit 39 affect the image display on the flat panel screen:"

TABLE XII

INPUT	DISPLAY EFFECT
Image Column Start	
(Latch 202)	Move image left-to-left
Image Row Start	
(Latch 210)	Move image up / down
Column Replicate Value	
(Latch 208)	Expand/contract image horizontally
Row Replicate Value	
(Latch 215)	Expand/contract image vertically
Column Count Up/Down	Image appears left-to-right
	Image appears right-to-left
Row Count Up/Down	Image appears top-to-bottom
	Image appears bottom-to-top

'096 Patent, col. 23, lines 1-3. The row replicate value (215) controls vertical sizing, and the column replicate value (209) controls vertical sizing. In other words, the row replicate value is the claimed "row replicate control signal" and the column replicate value is the claimed "column replicate control signal."

Figure 8 is said to illustrate the "logic schematic diagram of image size/position control unit 39," and shows where the row and column replicate values are used:

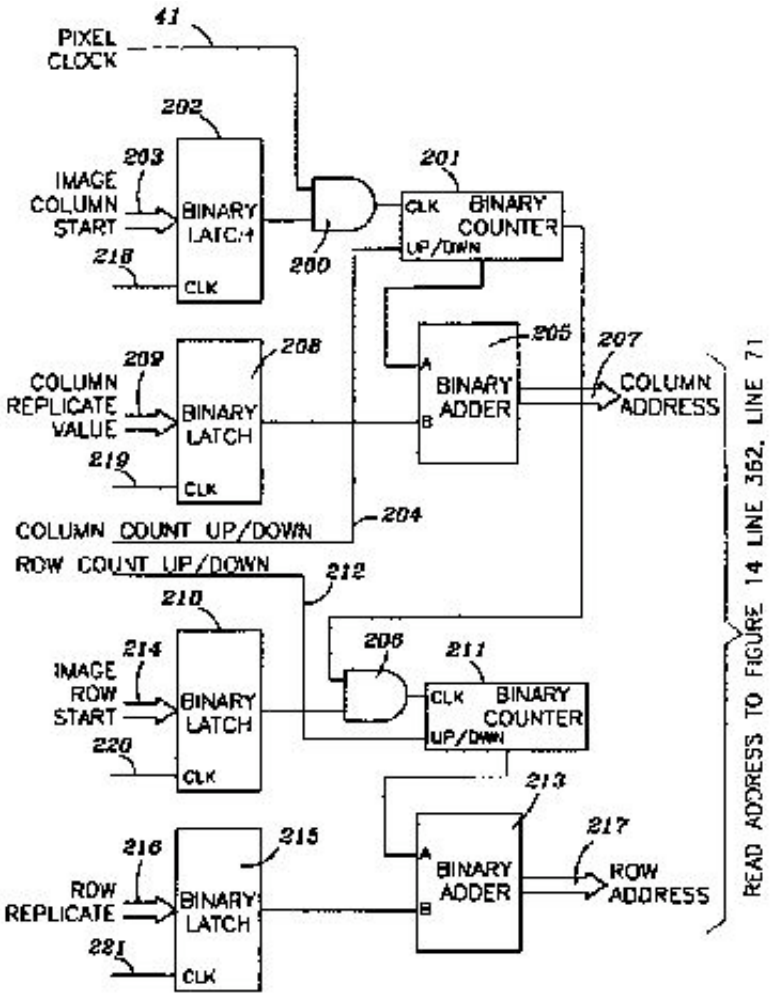


FIG. 8

The specification explains that "the image size/position control unit 39 provides image positioning, image size, and image orientation by modifying the memory addresses that are presented to the frame buffers 20, 24, and 25 [of Figure 1]." Apparently, the microprocessor (36) provides a number of signals to the image size/position control unit:

(1) "a column starting position into latch 202, the output of which enables the counter 201,"

(2) "a *column replicate value* on bus 209 into latch 208,"

(3) "an image row start value into latch 210 by way of bus 214,"

(4) "a *row replicate value* into latch 215 by way of bus 216,"

(5) latch output "clock signals" on lines 218, 219, 220 and 221"

(6) "a column count up/down control signal on line 204 to the up/down input of counter 201," and

(7) "a row count up/down control signal on line 212 to the up/down input of counter 211."

'096 Patent, col. 22, lines 28-41 (emphasis added).

The image size/position control unit processes the row/column replicate signals as follows:

When the pixel clock signal on line 41 and the output of latch 202 are a logic one, the binary counter 201 is enabled and begins counting up or down, depending upon the logic level of line 204. Further, when the count value output of the counter 201 and the output of latch 210 are a logic one, the gate 206 enables the counter 211. The counter begins counting up or down depending upon the logic level of the control signal on line 212. A *primary column address* from counter 201 is applied to one input of the adder/subtractor 205, and the *column replicate value* of latch 208 is applied to the second data input of the adder/subtractor 205. The replicate value then *is added or subtracted from the primary column address* as determined by the sign of the replicate value. *The resulting output of the adder/subtractor 205 is a column address* which is applied by way of bus 207 to the frame buffer output control unit 42 by way of busses 207 and 71.

In like manner, when the overflow output of counter 201 and the image row start signal at the output of latch 210 are a logic one, the counter 211 is enabled, and the counter 211 counts up or down depending upon the logic level of the line 212. The output of the counter 211 is a *primary row address from which the row replicate value at the output of latch 215 is added or subtracted* depending upon the sign of the replicate value. The *resulting output of adder/subtractor 213 is a row address* which is applied by way of busses 217 and 71 to the frame buffer output control unit 42.

'096 Patent, col. 22, lines 41-67 (emphasis added). The resulting output, *i.e.*, the column and row addresses resulting from the replicate value addition or subtraction, is thus sent to the frame buffer output control unit (42) (Figure 1).

The specification explains what the frame buffer output control unit does in connection with Figure 17:

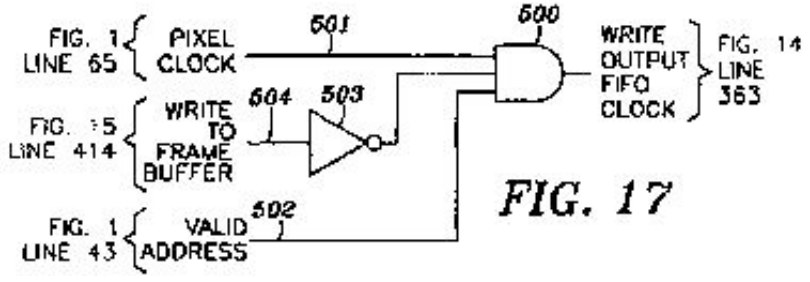


FIG. 17

According to the specification, "a logic AND gate 500 receives a pixel clock signal on line 501 from the flat panel timing generator 29 by way of line 41, the image size/position control unit 39 and line 65 of Fig. 1. Further, a write to frame buffer signal is received on line 504 from line 414 of Fig. 15 [illustrating frame

buffer input control unit 27 of Figure 1]. The valid address signal 502 is received by the microprocessor 36 on line 43. This signal is set by the microprocessor to allow video data to be read from the frame buffers 20, 25 and 24 of Fig. 1." '096 Patent, col. 27, lines 46-54. It is not clear, though, what the frame buffer output control unit does with the output of the image size/position control unit. The illustration of the image size/position control unit in Figure 8 actually points to Figure 14, which is said to illustrate the frame buffer used in Figure 1 (there are three: red frame buffer 20, green frame buffer 25 and blue frame buffer 24). The focus thus turns to Figure 14.

Figure 14 illustrates the row/column read address from the image size/position control unit at line 362 (line 71 of Figure 1).

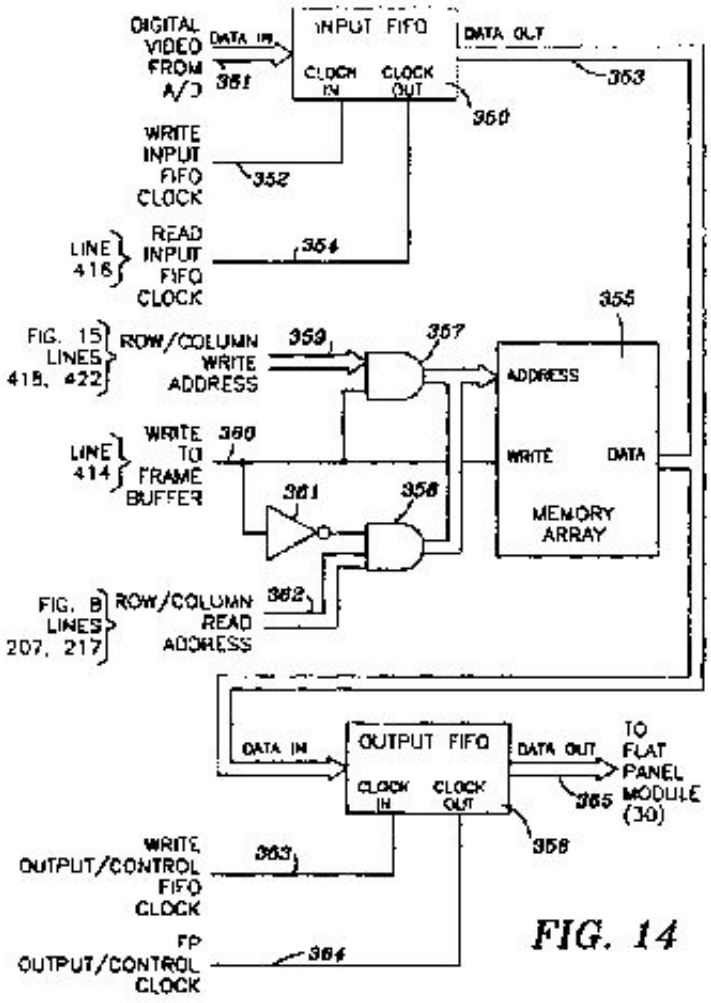


FIG. 14

Briefly, the input of gate 358 is apparently connected to the frame buffer output control unit 42 via bus 362. *See* '096 Patent, col. 25, lines 50-60 ("The address input of the memory array 355 is connected to the outputs of AND gates 357 and 358. One input of the gate 357 is connected to a bus 359 on which frame buffer input control unit 27 supplies a row/column write address signal. The second input of the gate 357 is connected to a line 360, which in turn is connected to a write input of the memory array 355 and to the input of an inverter 361. The output of inverter 361 is connected to a first input of gate 358, the second input of which is

connected to a bus on which the frame buffer output control unit 42 supplies a row/column read address signal."). According to the specification, "[d]ata is read out of or written into the memory array 355 * * *. Further, the addresses of the memory locations into which data is written is controlled by gate 357, and the *addresses of the memory locations from which data is read is controlled by gate 358*. From the memory array 355, the video data is read into the FIFO 356 at the video rate of the flat panel display as determined by the clock signal appearing on line 363 from the frame buffer output control unit 42, and read out of the FIFO at a different clock rate received from the frame buffer output control unit 42 on line 364. The video image data for the flat panel display appears at the output of FIFO 356." '096 Patent, col. 26, lines 11-23 (emphasis added).

Although the specification's description is perhaps not as clear as it could be, it is reasonably clear that the row/column replicate control signals control how often a row or column is repeated by controlling the number of times that a column address is read out of the frame buffer. In other words, video data is stored and read out of addresses within the memory. Some of those addresses are for row video data, and some are for column video data. A column or a row may be replicated by twice reading the same column or row data out of a memory address.

What is quite clear, though, is that the specification describes use of the row/column replicate control signals to repeat entire rows and columns of pixels, not individual pixels on a screen. In other words, the claimed control signals are not used together to pinpoint a particular pixel for replication. That a screen may have a great number of pixel locations does not change that. The specification discloses flat panel displays with lines of pixels and columns of pixels. *See* '096 Patent, col. 2, lines 45-47 ("The microprocessor also can detect various VGA video modes such as, by way of example only, 640 x480, 800x600, 1024x768, 1280x1024 pixels."); '096 Patent, col. 13, lines 23-26 ("[T]he electronic control system of FIG. 1 is a versatile system which may adapt to any format, and which is able to accommodate video resolutions up to at least 2048x2048 (rowsxcolumns)."); '096 Patent, col 12, lines 32-53, discussing the rows and columns that are replicated:

TABLE VIII		
FLAT PANEL CODE	MANUFACTURER/MODEL NO.	PARAMETERS
00	Sharp 640 x 480	rows = 480 columns = 640 max clock = 25 MHz image start column-44 image start rows = 34
01	Sharp 800 x 600	rows = 600 columns = 800 max clock = 40 MHz image start columns = 88 image start rows =

		image start rows = 23
02	NEC 640 x 480	rows = 480 columns = 640 max clock = 25 MHz image start column = 48 image start row = 23
03	NEC 800 x 600	rows = 600 columns = 800 max clock = 40 MHz image start columns = 128 image start rows = 21

Indeed, LG's argument that addressing could begin "at any location in the memory space" relies on the specification's disclosure of positioning, not sizing. *See* '096 Patent, col. 9, lines 25-31 ("Under the control of the microprocessor 36 and the image size/position control unit 39, the control unit 42 also positions an image on the flat panel display screen by addressing the frame buffer memory locations commencing at any location in the memory space. By changing the starting address of the video to be read, the image can be positioned left-to-right, right-to-left, or up or down."). That is, any column/row intersection could serve as a reference point for repositioning the image on the screen. That is a much different situation than resizing the image. In any event, the applicant knew what pixel-by-pixel control was, but did not describe the claimed replicate control signals as used for pixel-by-pixel control. *See* '096 Patent, col. 1, lines 56-58 ("U.S. Pat. No. 5,327,240 is mentioned only as a reference exercising pixel by pixel control to achieve high resolution displays of images." FN3). LG's argument to the contrary must therefore be rejected.

FN3. The abstract of the '240 Patent reads:
A method is provided for deinterlacing pixels in a video display system operable to display images as a plurality of pixels arranged in first and second fields of interlaced rows, at least one video component level quantified by a numerical video component value characterizing each pixel in an image with the video component levels for the pixels in the first and second fields being updated on alternate scans. A global mean video component value is computed from the video component values generated for a previous scan of at least one of the first and second fields. A global standard deviation is computed for the global mean. A local mean video component value is computed from the video component values generated for a plurality of pixels being updated as part of the current scan of the first field and defining a neighborhood of a pixel in the second field being deinterlaced. A local standard deviation is computed form the local mean video component value. The local standard deviation is compared with a selective multiple of the global standard deviation and if the local standard deviation is less than the selected multiple of the global standard deviation, the video component value generated for the pixel being deinterlaced as part of the previous scan of the second field is carried forward and if the local standard deviation exceeds the selected multiple of the global standard deviation then the video component value for the pixel being deinterlaced is set to the

computed local mean video component value.

As for LG's proposed limitations that the column address be "identified at least in part by a [column/row] start control signal," and the proposed limitation "in order to control the size of video on a display screen," the claim separately calls for the column and row start signals, and states that they, along with the column/row replicate control signals, are used "for sizing said video image." The claim does not further define the relationship between the start and replicate signals. There is no need to repeat or go beyond that in construing these terms.

Thus, the Court construes the term "column replicate control signal" to mean "a signal that controls the number of times a column of pixels is repeated by controlling how often video data is read from a column address in memory." A "row replicate control signal" means "a signal that controls the number of times a row of pixels is repeated by controlling how often video data is read from a row address in memory."

g) "sizing said video image"

This phrase appears in claim 21 (the disputed term is in boldface):

21. A system for controlling size, position and orientation of a video image presented on a flat panel display, * * * which comprises:

timing control means receiving said video signal from said video source at a video signal data rate for generating therefrom enable, vertical synchronization, horizontal synchronization, and first clock signals for driving said flat panel display, generating column start, row start, column replicate, and row replicate control signals for **sizing said video image** while maintaining a video signal resolution, and generating first control signals for reading said video image in said memory system;

image size/position control means * * *; and

frame buffer output control means * * *.

'096 Patent, col. 31, line 59-col. 32, line 19 (emphasis added).

(1) The Parties' Positions

The parties propose the following constructions:

LG	***Hitachi***
Controlling the size of the video image on the display screen.	Altering the size of the existing video image that is stored in said memory

See Dkt. No. 64, at 30.

LG urges that the dispute "centers on whether the size of the video image need be controlled (as we urge) or altered (as Defendants urge)." Dkt. No. 47, at 52. According to LG, "microprocessor 36 programs image

size/position control unit 39 'to accommodate a 1-to-1 sized image,' " and then "determines whether a video image to be presented is to be upsized, downsized, or unaltered." *Id*. "If a change in sizing has occurred, microprocessor 36 'reprograms the image size/position control unit 39 with new size values (horizontal and vertical replication)' "; however, "[i]f no such sizing is to take place (i.e., the video image is to remain unaltered) microprocessor 36 moves on to its next logic step and does not reprogram image size/position control unit 39, thus causing the unit 39 to remain programmed to accommodate a 1-to-1 sized video image." *Id*. at 52-53. Thus, LG contends, this phrase "need not require an 'altering' of a video image to be presented on a flat panel display." *Id*. at 53.

Hitachi argues that "the issue here is ***not*** whether the Court ultimately decides to adopt [LG's] construction of 'controlling' or [Hitachi's] construction of 'altering' * * * [but rather] that [LG's] construction violates clear Federal Circuit precedent by ignoring the words of the claim itself." Dkt. No. 48, at 18. Hitachi urges that LG "again replaces '***said*** video image' with '***a*** video image' * * * [and] "implicitly concedes that the video image is re-sized by controlling the readout from memory in its construction of column and row replicate control signals ('number of times a particular column/row address ... is read out of the frame buffer')." Dkt. No. 48, at 18-19. Hitachi concludes that the "specification makes clear that it is the video image in memory-with column and row memory addresses-that is re-sized" and urges that "the claim element can be no broader than [Hitachi's] construction, because this is the only embodiment described in the specification. *Id*. at 19.

In response, LG modified its original proposed construction, "Controlling the size of a video image on a screen display," to replace "the indefinite articles in its original construction with the definite article 'the' so that [LG's] proposed construction * * * dispatches Defendants' manufactured criticism of [LG's] proposal." Dkt. No. 55, at 44-45.

(2) Construction

[8] The parties appear to have resolved the dispute over this term. As Hitachi notes, the claim calls for "sizing said video image," namely, the video image stored in the "memory system."

Beyond that, the foregoing discussion of column and row replicate control signals makes clear that sizing is accomplished by adding or removing lines and/or columns to achieve a certain fit on a display screen. Again, though, it is not clear whether that is truly in dispute. This is an apparatus claim that calls for "control signals for resizing * * *." In accordance with the specification, an image may be "upsized" or "downsized" or left "unaltered." Again, that does not appear to be in dispute.

Thus, the Court concludes that in the context of claim 21, "sizing said video image" means "controlling the size of the video image on the display screen."

h) "while maintaining a video signal resolution"

This phrase appears in claim 21 (the disputed term is in boldface):

21. A system for controlling size, position and orientation of a video image presented on a flat panel display, * * * which comprises:

timing control means receiving said video signal from said video source at a video signal data rate for generating therefrom enable, vertical synchronization, horizontal synchronization, and first clock signals for

driving said flat panel display, generating column start, row start, column replicate, and row replicate control signals for sizing said video image **while maintaining a video signal resolution,** and generating first control signals for reading said video image in said memory system;

image size/position control means * * *; and

frame buffer output control means * * *.

'096 Patent, col. 31, line 59-col. 32, line 19 (emphasis added).

(1) The Parties' Positions

The parties propose the following constructions:

LG	***Hitachi***
Without requiring a change in the video signal resolution received from the video source.	Without losing pixel data from said video signal from said video source.

See Dkt. No. 64, at 31.

LG contends that "[o]ne of the principal features of the '096 patent is to receive a video image of diverse video formats and resolutions and be able to accept, process, and display the video image on a flat panel display while maintaining a resolution of the video signal (despite any adjustments in size, position, and/or orientation)"-all "without requiring the video source to provide a video signal having the features * * * dependant on how the video image is to be presented on the flat panel display and/or the type of flat panel display being used." Dkt. No. 47, at 53. According to LG, "the system disclosed by the '096 patent performs the work of presenting a video image on a flat panel display in a manner compatible with hardware (e.g., flat panel display) constraints and user preferences (e.g., up-sizing, down-sizing, rotating, shifting side-to side) while accepting the video signal exactly as it is provided by the video source and without requiring any work on the part of the video source to adjust for the ultimate outcome of the presentation of the video image." Id. at 53-54.

Hitachi argues that "[t]he' Background of the Invention' section of the specification defines this term in distinguishing the invention over the prior art:"

The system disclosed in [prior art] U.S. Pat. No. 5,267,045 is defective, however, in that it performs sizing by varying the video rate as the video data is being stored. As a result, *pixel data is lost and image resolution is compromised*.

Dkt. No. 48, at 19 (citing '096 Patent, col. 1, lines 26-30).

Hitachi concludes: "the specification teaches that, in order to leave pixel data uncompro-mised, one needs to size the video image without losing any pixel data, *i.e.,* all of the pixel data in the original image must be present in the resulting image." Dkt. No. 48, at 19. Hitachi urges that "the real issue is the meaning of the term 'resolution,' " which was never addressed by LG. *Id*.

In reply, LG urges that its construction "focuses on the 'real issue' of this disputed claim term-which is clarifying the claim language with respect to how the video signal resolution is maintained while sizing the

video image." Dkt. No. 55, at 45. LG argues that this is "accomplished by accepting a wide variety of video signals without requiring the video source to provide a signal with a specific characteristics, such as signal resolution." *Id*. With respect to the term "resolution," LG argues that "the Court need not redefine every single word in a disputed phrase, especially when the meaning of the word (like 'resolution' here) would be clear to the fact finder." Dkt. No. 55, at 45 (citing O2 Micro Intern. Ltd. v. Beyond Innovation Tech. Co., Ltd., 521 F.3d 1351, 1362 (Fed.Cir.2008)).

Furthermore, LG asserts that "Defendants' proposed construction should be rejected because it is vague and improperly excludes certain embodiments covered by claim 21," such as the ability to "up-size or down-size an image on the display screen." Dkt. No. 55, at 46. LG notes that Hitachi's "construction precludes such aspects of the invention, because, for example, by down-sizing the video image, the device necessarily loses pixel data in the image by only presenting a subset of the data (by removing portions of the image to shrink it)." *Id*.

(2) Construction

[9] According to the specification, "in accordance with the invention, video data may be received at the video rate and asynchronously output to a flat panel display at the display rate without any loss of resolution." '096 Patent, col. 2, lines 12-15. *See also* id. at col. 2, lines 28-31 ("An electronic control system is disclosed which automatically identifies video signal type, format, and resolution, and adapts the video image for display on a wide variety of full color and monochrome flat panel display systems."); ' 096 Patent, col. 11, lines 42-44 ("the microprocessor manages the power operation of the electronic control system, identifies the modes of the incoming video (interlace, non-interlace, resolution, type)"). That is, the video data may be received at one rate and output to the display at another rate, all without losing resolution.

The asynchronous data input/output of the prior art, however, resulted in lost pixel data and compromised image resolution:

The system disclosed in U.S. Pat. No. 5,267,045 is defective, however, in that it performs sizing by varying the video rate as the video data is being stored. As a result, pixel data is lost and image resolution is compromised.

'096 Patent, col. 1, lines 26-30.FN4 The prior art, of course, used video rate differences to effect sizing. The system of the ' 096 Patent accommodated video rate differences, but did not use it to effect sizing. The ' 096 Patent's different approach to sizing thus meant that video rate difference could be accommodated so as to avoid loss of resolution. In other words, the ' 096 Patent and the prior art disclosed systems that received video data at one rate, and displayed it at another. The prior art used that data rate difference to effect sizing, resulting in compromised resolution, while the ' 096 Patent accommodated it and sized in a different way so as not to compromise resolution. That is, in a more succinct way, what claim 21 calls for: "sizing said video image while maintaining a video signal resolution." LG is thus correct. As noted in prior sections above, sizing may result in lost pixel data. The ' 096 Patent is said to disclose a system in which pixel data may be lost during sizing without losing resolution. *See* ' 096 Patent, col. 13, lines 2326 ("[T]he electronic control system of FIG. 1 is a versatile system which may adapt to any format, and which is able to accommodate video resolutions up to at least 2048x2048 (rowsxcolumns).").

FN4. The '045 Patent, entitled "Multi-Standard Display Device With Scan Conversion Circuit," provides the following abstract:

A multi-standard display device having a liquid crystal display screen has so far only been realized by using all kinds of interpolation techniques. To make the number of rows and columns of the display screen independent of the incoming video signal and yet provide the possibility of displaying the various television standards without any disturbing errors, the incoming video signal is applied to the display screen via a scan-conversion circuit. The scan-conversion circuit reads in the video information in a first direction and subsequently reads it out in a second direction perpendicular to the first direction, for example, with storage in a memory. The video information is subsequently applied in the second direction to the row driver of the display screen, which row driver applies the video information to the display screen per column and under the control of the column driver.

The '045 Patent explains, *inter alia,* that (1) "Reading in and reading out with (possibly) different clock signals provides the freedom of enlarging, for example, a part of the picture, which will often be necessary because the number of pixels per line and the number of lines of a picture are not equal," col. 2, lines 16-20; (2) "the height of the picture can be varied by varying the frequency of the clock signal ck2 for reading out the memories and by varying the first position which is read out. For example, when a 9:16 display screen is used, a 3:4 video signal can be enlarged to a 9:16 picture, in which the upper and lower parts of the picture are lost, however," col. 4, lines 6-12; and (2) "A part of the picture can be enlarged ("zoom") by firstly increasing the frequency of the read clock ckl during reading into the memory and, secondly, by increasing the sampling frequency ck3 at the display screen." Col. 4, lines 6-12.
Thus, the Court construes the phrase "while maintaining a video signal resolution" to mean "without requiring a change in the video signal resolution received from the video source."

i) "generating first control signals for reading said video image in said memory system"

This phrase appears in claim 21 (the disputed term is in boldface):

21. A system for controlling size, position and orientation of a video image presented on a flat panel display, * * * which comprises:

timing control means receiving said video signal from said video source at a video signal data rate for generating therefrom enable, vertical synchronization, horizontal synchronization, and first clock signals for driving said flat panel display, generating column start, row start, column replicate, and row replicate control signals for sizing said video image while maintaining a video signal resolution, and **generating first control signals for reading said video image in said memory system;**

image size/position control means * * *; and

frame buffer output control means * * *.

'096 Patent, col. 31, line 59-col. 32, line 19 (emphasis added).

(1) The Parties' Positions

The parties propose the following constructions:

LG	***Hitachi***
Generating first control signals that are used	Creating column count up/down signals and row count

to read the video image from the memory system.	up/down signals for reading said video image in said memory system.

See Dkt. No. 64, at 32.

LG contends the dispute "presents a clear choice for the Court-rewrite the claim language as urged by defendants or simply construe the claims in accordance with the ordinary language, which is consistent with the specification." Dkt. No. 47, at 54. According to LG, "[i]t is clear that the microprocessor 36 generates first control signals for reading a video image out of memory (both parties agree on that)"; however, Hitachi "seek[s] to improperly limit the first control signals to the column and row count up/down control signals, to the exclusion of the other types of information provided to image size/position control unit 39 by microprocessor 36 via the first control signals." *Id*.

Hitachi urges that "[t]he specification describes only one embodiment of the invention, and Defendants' construction is consistent with this embodiment by construing the recited 'control signals' to be the disclosed column and row up/down signals."

The microprocessor 36 also issues a column count up/down control signal on line 204 to the up/down input of counter 201, and a row count up/down control signal on line 212 to the up/down input of counter 211.

Dkt. No. 48, at 20, (citing '096 Patent, col. 22, lines 38-41). Hitachi argues that LG's "brief actually identifies ***other*** signals besides the up/down count signals that it says could be the 'control signals,' " namely, the signals described at column 7, lines 40-45:

In response to the control code supplied by the module 30 on line 35, the microprocessor 36 issues a programmable control signal on a line 37 to a fourth input of generator 29, and a control signal on a line 38 to one input of an image size/position control unit 39.

Id. at 20. Hitachi argues that "none of the signals in this passage can be the 'first control signals' recited in claim 21," *i.e.*, "[t]he signal supplied on line 37 cannot be the 'first control signals' because the signal on line 37 is not input into the 'image size/position control means' and "[t]he signal supplied on line 38 cannot be the 'first control signals' because line 38 carries the column/row start/replicate control signals recited elsewhere in claim 21." Id. Hitachi notes that "Claim 21 requires that the 'first control signals' are both (i) input into the image size/position control means (which must be responsive to these signals) and (ii) 'for reading said video image in said memory system,' " and concludes that "[t]he only signals disclosed in the specification that can possibly be these signals are the 'column count up/down' and 'row count up/down' signals." Id. at 20-21. Finally Hitachi reiterates that "the same 'said video image' and 'said memory system' must satisfy all the requirements of claim 21." Id. at 21.

In response, LG urges that the specification "discloses several different control signals that correspond to 'first control signals,' and, thus, [Hitachi's] attempts to limit them to the 'column count up/down' and 'row count up/down' signals are improper." Dkt. No. 55, at 46. LG asserts that "[e]ach of these disclosed control signals are input into the image size/position control means and are used for reading the video image in the memory system." *Id*.

(2) Construction

[10] The issue here seems to be the meaning of "generating first control signals." Hitachi urges a meaning

of creating column/row count up/down signals, but this construction goes beyond what the claim requires. The claims state what the "first control signals" are for, namely, "reading said video image in said memory system." There is no dispute over that. Defining the "first control signals" as column/row count up/down signals would add limitations not found in claim 21. Claim 21 calls for a number of different signals, but count up/down signals are not among them.

Indeed, the control signals disclosed in the specification as corresponding to the "first control signals" are not limited to column/row count up/down signals.

According to the specification, "[t]he microprocessor 36 manages the entire operation of the electronic control system of Fig. 1." FN5 ' 096 Patent, col. 7, lines 49-50. The microprocessor sends control signals to a number of different elements, *e.g.:*

FN5. *See supra* Part II.A for a reproduction of Figure 1.

* "The frame buffer input control unit 27 manages the incoming video to insure correct storage into the frame buffers. As a consequence to a *control signal* received from the microprocessor 36, the control unit 27 adopts the correct writing sequence to store incoming video signals sequentially, line by line, top to bottom, as either interlaced or non-interlaced signals at the rate received." '096 Patent, col. 6, lines 41-47 (emphasis added).
* "In response to *control information* received from the microprocessor 36, the pixel clock generator 28 is line locked to each horizontal line of incoming video, and synchronizes all pixel operations for processing video data." '096 Patent, col. 6, lines 51-54 (emphasis added).

* "In response to the control code supplied by the module 30 on line 35, the microprocessor 36 issues a programmable *control signal* on a line 37 to a fourth input of generator 29, * * *." '096 Patent, col. 7, lines 41-45 (emphasis added).

* "In response to the control code supplied by the module 30 on line 35, the microprocessor 36 issues * * * a *control signal* on a line 38 to one input of an image size/position control unit 39." '096 Patent, col. 7, lines 41-45 (emphasis added).

According to the specification, "[t]he image size/position control unit 39 controls the relative size and position of the incoming video images on the display screen," and, "*[i]n response to signals received from the microprocessor 36,*" "determines the display screen size, sizes the video image up or down to accommodate the display screen, and reprograms the flat panel timing generator 29 to be compatible with the image size." '096 Patent, col. 8, lines 38-44 (emphasis added).

The specification further explains that the image size/position control unit is connected to the frame buffer output control unit 42, which also is controlled by the microprocessor as well as the image size/position control unit. *See* '096 Patent, col. 8, lines 50-62 ("The output of the control unit 39 is connected to a first input of frame buffer output control unit 42, which receives sizing, position, and orientation information from microprocessor 36 on line 43. More particularly, the microprocessor instructs the control unit 42 how to use the timing signals supplied by the image size/position control unit 39 on line 71 to supply memory address locations at third inputs of frame buffer 20, frame buffer 24, and frame buffer 25. * * * * A timing signal that controls the reading of data from the frame buffer memory is output by control unit 39 to control

unit 42 on line 65.").

According to the specification, "[t]he order in which data is read out of the frame buffers determines the form in which the image will be presented on the plat [sic] panel display screen." '096 Patent, col. 8, lines 57-60. That corresponds to the claim limitation "reading said video image in said memory system." In short, the image size/position control unit and frame buffer output control unit both work to read video data out of the frame buffers (memory). The signals that control those devices are generated by the microprocessor, and communicated to those devices via lines 38 and 43.

As seen in Figure 8,FN6 which is said to illustrate the image size/position control unit 39, some of the control signals from the microprocessor are the column and row count up/down signals. *See* ' 096 Patent, col. 22, lines 1-4 ("The binary counter 201 also receives a column count up/down signal on line 204 from the microprocessor, * * *."); ' 096 Patent, col. 22, lines 12-15 ("The counter 211 also receives a row count up/down signal at its up/down input from the microprocessor 36 by way of line 212, * * *."). But the microprocessor supplies more than just those count up/down signals to the image size/position control unit. For example, the image size/position control unit also "receives an image column start signal from the microprocessor 36 on cable 203," "receives a column replicate value on bus 209 from microprocessor 36," "receives an image row start value from the microprocessor on bus 214," and "receives a row replicate signal from the microprocessor by way of bus 216." ' 096 Patent, col. 21, lines 65-67; col. 22, lines 8-9; col. 22, lines 16-17; col. 22, lines 19-20.

FN6. *See supra* Part II.B.2(f) for a reproduction of Figure 8.

Hitachi urges that those latter four signals cannot also be the control signals because claim 21 elsewhere recites generation of those signals:

timing control means receiving said video signal from said video source at a video signal data rate for generating therefrom enable, vertical synchronization, horizontal synchronization, and first clock signals for driving said flat panel display, generating *column start, row start, column replicate,* and *row replicate* control signals for sizing said video image while maintaining a video signal resolution, and generating *first control signals* for reading said video image in said memory system

'096 Patent, col. 31, lines 64-col. 32, line 6 (emphasis added). That argument has some merit. However, as noted above, the microprocessor also communicates control signals to the frame buffer output control unit for "reading said video image in said memory system," and those control signals should be considered part of the claimed "first control signals." Further, as Figure 17 FN7 ("logic schematic form the frame buffer output control unit 42 of Fig. 1") illustrates, the frame buffer output control does not receive count up/down control signals from the microprocessor. Thus, Hitachi's proposed construction must be rejected. The "first control signals" are not limited to count up/down signals. That is believed sufficient to resolve the parties' dispute.

FN7. *See supra* Part II.B.2(f) for a reproduction of Figure 17.

Therefore, the Court concludes that in the phrase "generating first control signals for reading said video image in said memory system," the " 'first control signals' are not limited to column count

up/down signals and row count up/down signals."

j) "output column address control signals" & "output row address control signals"

This phrase appears in claim 21 (the disputed term is in boldface):

21. A system for controlling size, position and orientation of a video image presented on a flat panel display, * * * which comprises:

timing control means * * *;

image size/position control means in electrical communication with said timing control means and responsive to said column start, row start, column replicate, and row replicate control signals and said first control signals for generating **output column address control signals, output row address control signals for said memory system,** and a pixel clock signal; and

frame buffer output control means * * *.

'096 Patent, col. 31, line 59-col. 32, line 19 (emphasis added).

(1) The Parties' Positions

The parties propose the following constructions:

Phrase	***LG***	***Hitachi***
"output column address control signals"	Signals that control the column address read out of memory.	A signal that carries a column address for outputting video data from the memory.
"output row address control signals"	Signals that control the row address read out of memory.	A signal that carries a row address for outputting video data from the memory.

See Dkt. No. 64, at 34.

LG urges that its proposed constructions "flow from the plain language and the description provided in the specification," citing column 22, lines 25-28, 54-57 and 65-67, and column 8, lines 50-57. Dkt. No. 47, at 56-57. According to LG, "the output column and row address signals actually control the column and row address read out of memory, rather than merely provide for 'outputting video data from memory' as Defendants contend." Id. at 57.

Hitachi contends that "[t]he output column address and output row address signals actually carry addresses, as opposed to merely being signals involved in the addressing process." Dkt. No. 48, at 21. Hitachi argues that LG has misunderstood the "operation of frame buffer output control unit 42," which has "a single output, which is input as a 'Clock in' signal to the Output FIFO 356." *Id*. at 21-22. Hitachi urges that "[a] clock signal is ***not*** an address signal." *Id*. at 22.

In response, LG urges that its construction is supported by the specification, namely:

The image size/position control unit 39 controls the relative size and position of the incoming video images on the display screen. In response to signals received from the microprocessor 36, the unit 39 determines the

display screen size, sizes the video image up or down to accommodate the display screen, and reprograms the flat panel timing generator 29 to be compatible with the image size as is further explained below in connection with the description of FIG. 8. ***The image size/position control unit 39 also creates a set of timing clocks and control signals that are provided to a frame buffer output control unit 42, which in turn addresses memory locations in the frame buffers. The output of the control unit 39 is connected to a first input of frame buffer output control unit 42,*** which receives sizing, position, and orientation information from microprocessor 36 on line 43 * * *. Column 8, lines 38-62

In operation, the image size/position control unit 39 ***provides*** image positioning, image size, and image orientation ***by modifying*** the memory addresses that are presented to the frame buffers 20, 24, and 25. Column 22, lines 25-28.

The resulting output of the adder/subtractor 205 [of image size/position control unit 39] is a column address which ***is applied by way of bus 207 to the frame buffer output control unit 42*** by way of busses 207 and 71. In like manner, when the overflow output of counter 201 and the image row start signal at the output of latch 210 are a logic one, the counter 211 is enabled, and the counter 211 counts up or down depending upon the logic level of the line 212. The output of the counter 211 is a primary row address from which the row replicate value at the output of latch 215 is added or subtracted depending upon the sign of the replicate value. ***The resulting output*** of adder/subtractor 213 is a row address which ***is applied by way of busses 217 and 71 to the frame buffer output control unit 42.*** Column 22, lines 52-67.

Dkt. No. 55, at 49-50. LG concludes that "the image size/position control means 39 generates various control signals used [sic] modify (or control) the column and row address read out of memory; thus, [LG's] construction is supported by the specification and should be adopted by the Court." *Id*. at 50.

Hitachi urges that the passages cited by LG "demonstrate that the signals generated by the 'image size/position control means 39' are actual address signals, not merely control signals related to addressing," because the "[b]usses 207 and 217 in Figure 8 correspond to line 71 in Figure 1," which "shows that bus 71 is carried ***directly to the frame buffers 20, 24, and 25:***"

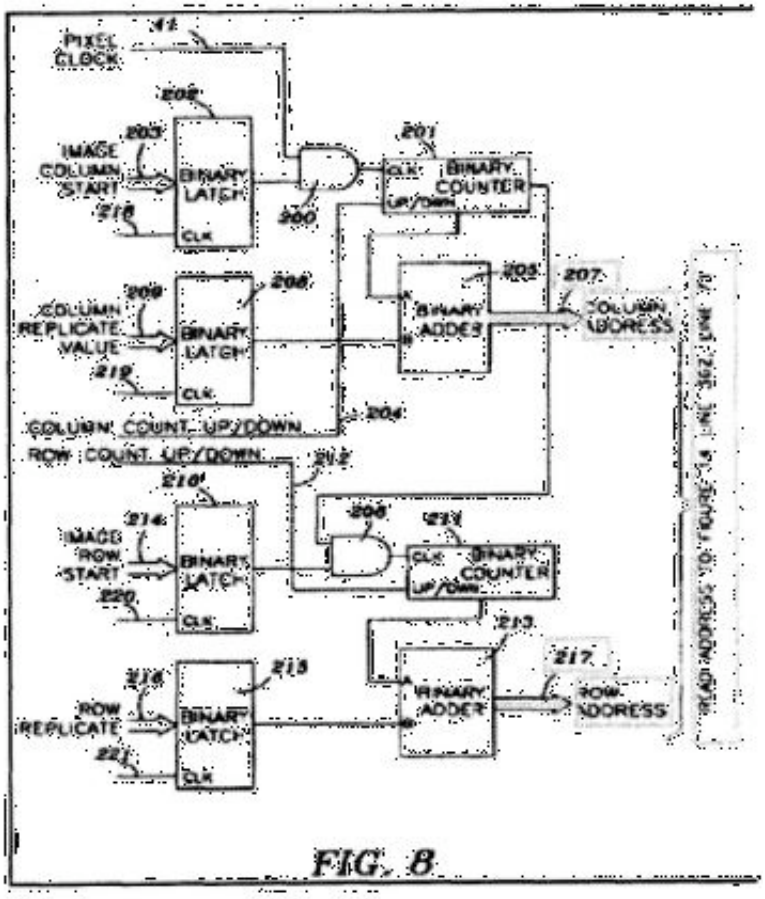

PIXEL CLOCK
41
202
203
IMAGE COLUMN START
BINARY LATCH
218
CLK
200
201
CLK
BINARY COUNTER
UP/DWN
205
207
COLUMN ADDRESS
209
206
COLUMN REPLICATE VALUE
BINARY LATCH
219
CLK
BINARY ADDER
COLUMN COUNT UP/DOWN
204
ROW COUNT UP/DOWN
212
216
214
IMAGE ROW START
BINARY LATCH
220
CLK
208
211
CLK
BINARY COUNTER
UP/DWN
213
217
ROW ADDRESS
215
216
ROW REPLICATE
BINARY LATCH
221
CLK
BINARY ADDER
TO 362 IN FIGURE 6 (COLUMN ADDRESS)

FIG. 8

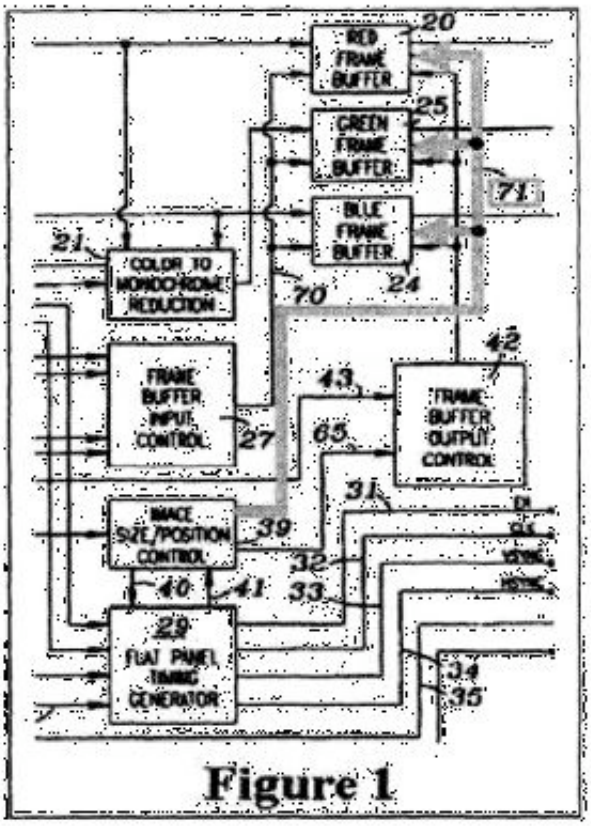


Figure 1

Dkt. No. 63, at 7. According to Hitachi, "Figure 14 further shows that buses 207 and 217 carry signals that are 'Row/Column Read Address' signals on line 362, which is input into the 'Address' input of the memory. The 'image size/position control unit 39' of the '096 patent thus generates actual address signals, not merely control signals that relate to the process of memory addressing." Id. at 7-8.

(2) Construction

[11] [12] The specification explains in connection with Figure 1 FN8 that "[t]he image size/position control unit 39 * * * creates a set of timing clocks and *control signals* that are provided to a frame buffer output control unit 42, which in turn addresses memory locations in the frame buffers." ' 096 Patent, col. 8, lines 46-49 (emphasis added). According to the specification, "[t]he output of the control unit 39 is connected to a first input of frame buffer output control unit 42, * * *. * * * [T]he microprocessor instructs the control unit 42 how to use the timing signals supplied by the image size/position control unit 39 on line 71 to supply memory address locations at third inputs of frame buffer 20, frame buffer 24, and frame buffer 25. * * * A timing signal that controls the reading of data from the frame buffer memory is output by control unit 39 to control unit 42 on line 65." ' 096 Patent, col. 8, lines 50-62.

FN8. *See supra* Part II.A.2 for a reproduction of Figure 1.

Once again, the image size/position control unit 39 is said to be depicted in Figure 8.FN9 It is apparent from Figure 8 that the image size/position control unit outputs an "output column address signal" (207) and an "output row address signal" (217). *See* ' 096 Patent, col. 22, lines 5-7 ("The output of the adder 205 is an output column address signal that is applied to bus 207."), and col. 22, lines 20-22 ("The output of the adder

213 is an output row address which is supplied to a bus 217.").

FN9. *See supra* Part II.B.2(f) for a reproduction of Figure 8.

According to the specification and Figure 8, those signals are sent to the frame buffers 20, 24 and 25 via line 71 (Figure 1) / line 362 (Figure 14). *See* '096 Patent, col. 22, lines 25-28 ("[T]he image size/position control unit 39 provides image positioning, image size, and image orientation by modifying the memory addresses that are presented to the frame buffers 20, 24, and 25."). Figure 14 FN10 illustrates one such frame buffer. Briefly, line 362 connects the "output column address signal" (207) and "output row address signal" (217) to the input of gate 358, which in turn is connected to the "address input of the memory array 355." *See* ' 096 Patent, col. 25, lines 50-60 ("The address input of the memory array 355 is connected to the outputs of AND gates 357 and 358. * * * The output of inverter 361 is connected to a first input of gate 358, the second input of which is connected to a bus on which the frame buffer output control unit 42 supplies a row/column read address signal."). According to the specification, "[d]ata is read out of * * * the memory array 355," and "the addresses of the memory locations from which data is read is controlled by gate 358." Thus, it appears that the "output column address signal" (207) and "output row address signal" (217) control the memory addresses from which video data is read. Accordingly, those signals correspond to the claimed "output column address control signals" and "output row address control signals." In other words, an "output column address signal" is a signal that controls the memory address from which column data is read, and an "output row address signal" is a signal that controls the memory address from which row data is read. Therefore, LG is correct.

FN10. *See supra* Part II.B.2(f) for a reproduction of Figure 14.

Thus, the Court construes the term "output column address signal" to mean "a signal that controls the memory address from which column data is read." An "output row address signal" is "a signal that controls the memory address from which row data is read."

k) "pixel clock signal"

This phrase appears in claim 21 (the disputed term is in boldface):

21. A system for controlling size, position and orientation of a video image presented on a flat panel display, * * * which comprises:

timing control means receiving said video signal from said video source at a video signal data rate for generating therefrom enable, vertical synchronization, horizontal synchronization, and first clock signals for driving said flat panel display * * *;

image size/position control means in electrical communication with said3 timing control means and responsive to said column start, row start, column replicate, and row replicate control signals and said first control signals for generating output column address control signals, output row address control signals for said memory system, and a **pixel clock signal;** and

frame buffer output control means in electrical communication with said timing control means, said memory

system, said image size/position control means, and said flat panel display, and responsive to said **pixel clock signal** for reading said video image from said memory system.

'096 Patent, col. 31, line 59-col. 32, line 19 (emphasis added).

(1) The Parties' Positions

The parties propose the following constructions:

LG	***Hitachi***
A clock signal used to synchronize pixel operations for driving the flat panel display.	A clock signal used to synchronize all pixel operations for processing video data.

See Dkt. No. 64, at 35.

According to LG, "[o]ne point of contention here is whether the 'pixel clock signal' as claimed synchronizes 'pixel operations for driving the flat panel display,' as LGE contends, or 'all pixel operations for processing video data' as Defendants contend." Dkt. No. 47, at 57. LG asserts that Hitachi's proposed construction "ignores the plain language of claim 21 and instead improperly attempts to import the specification into the construction by requiring the phrase 'all pixel operations' as part of the construction," whereas LG's "recognizes that the 'pixel clock signal' of claim 21 is an input used to generate output column address and output row address signals." *Id*.

Hitachi argues that "the pixel clock signal is used to synchronize "***all pixel operations for processing video data,***" citing column 6, lines 51-54, and urges that "[a]bsent any other definition or explanation of the pixel clock signal, this is the proper construction of the limitation." Dkt. No. 48, at 10. Hitachi asserts that LG's construction "confuses the pixel clock signal with a different clock signal recited earlier in claim 21." *Id*. Finally, Hitachi notes that "claim 21 also recites 'first clock signals' generated by the 'timing control means,' " but that "the 'first clock signals,' not the 'pixel clock signal,' are 'for driving the flat panel display.' " *Id*.

In response, LG contends the claim language does not "require that the 'pixel clock signal' synchronize 'all' of the relevant operations" and that "[t]he important aspect of the pixel clock is 'synchronization.' " Dkt. No. 55, at 50. Finally, LG urges that "a pixel clock is certainly part of the signaling that ultimately drives the flat panel display." *Id*.

(2) Construction

[13] In short, Hitachi is correct. The specification explains that the pixel clock generator 28 "synchronizes *all* pixel operations for processing video data." *See* '096 Patent, col. 6, lines 51-54 ("In response to control information received from the microprocessor 36, the pixel clock generator 28 is line locked to each horizontal line of incoming video, and synchronizes all pixel operations for processing video data."). *See also* '096 Patent, col. 10, lines 62-63 ("The pixel clock is used to synchronize all input timing to the electronic control system of Fig. 1."). Further, as Hitachi notes, claim 21 states that another signal, the "first control signal," is for "driving the flat panel display."

Thus, the Court construes the term "pixel clock signal" to mean "a clock signal used to synchronize all pixel operations for processing video data."

C. Means-Plus-Function Limitations

The "system" of asserted claim 21 contains three "means" elements (boldface added):

21. A system for controlling size, position and orientation of a video image presented on a flat panel display, and in electrical communication with a memory system having stored therein said video image, and receiving a video signal from a video source, which comprises:

timing control means * * * for generating therefrom enable, vertical synchronization, horizontal synchronization, and first clock signals * * *;

image size/position control means * * * for generating output column address control signals, * * *; and

frame buffer output control means * * * for reading said video image4 from said memory system.

'096 Patent, col. 31, line 59-col. 32, line 19 (emphasis added).

1. Proper Construction of Means-Plus-Function Limitations

Section 112(6) of the patent statute provides:

An element in a claim for a combination may be expressed as a means or step for performing a specified function without the recital of structure, material or acts in support thereof, and such claim shall be construed to cover the corresponding structure, material, or acts described in the specification and equivalents thereof.

35 U.S.C. s. 112 para. 6 (2006). Section 112(6) thus allows "an applicant [to] describe an element of his invention by the result accomplished or the function served, rather than describing the item or element to be used * * *." Warner-Jenkinson Co. v. Hilton Davis Chem. Co., 520 U.S. 17, 27, 117 S.Ct. 1040, 137 L.Ed.2d 146 (1997).

The general hallmarks of a means-plus-function element are three-fold. First, the element is expressed in terms using "means" or "step," which raises a presumption that there was an intent to invoke s. 112(6). *See* Elbex Video, Ltd. v. Sensormatic Elecs. Corp ., 508 F.3d 1366, 1370 (Fed.Cir.2007) ("Because this limitation uses 'means for' there is a presumption that the claim invokes 35 U.S.C. s. 112, para. 6."). Second, a specified function follows the "means" or "step" and is linked to the "means" or "step." *See* York Prods., Inc. v. Central Tractor Farm & Family Ctr., 99 F.3d 1568, 1574 (Fed.Cir.1996). Third, the claim contains insufficient structure, material or acts for achieving the specified function. *See* MIT and Elects. for Imaging, Inc. v. Abacus Soft-ware, Inc., 462 F.3d 1344, 1353 (Fed.Cir.2006); Apex v. Raritan, 325 F.3d 1364, 1372 (Fed.Cir.2003). "Means-plus-function" limitations are construed, as required by s. 112(6), to cover the corresponding structure, material or acts described in the specification and any equivalent structures. *See* In re Donaldson, 16 F.3d 1189, 1195 (Fed.Cir.1994) (*en banc*); Callicrate v. Wadsworth Mfg., Inc., 427 F.3d 1361, 1369 (Fed.Cir.2005). *See also* IMS Tech., Inc. v. Haas Automation, Inc., 206 F.3d 1422, 1436 & n. 3 (Fed.Cir.2000); Commonwealth Scientific & Indus. Research Org. v. Buffalo Tech., 542 F.3d 1363, 1385 (Fed.Cir.2008).

The Court must decide as a matter of law whether a particular term or phrase is governed by s. 112(6). *See Phillips,* 415 F.3d at 1212; Lighting World, Inc. v. Birchwood Lighting, Inc., 382 F.3d 1354, 1358

(Fed.Cir.2004) ("The task of determining whether the limitation in question should be regarded as a means-plus-function limitation, like all claim construction issues, is a question of law for the court, even though it is a question on which evidence from experts may be relevant."); Personalized Media Communications, LLC v. Int'l Trade Comm'n, 161 F.3d 696, 702 (Fed.Cir.1998). "Once a court concludes that a claim limitation is a means-plus-function limitation, two steps of claim construction remain: 1) the court must first identify the function of the limitation; and 2) the court must then look to the specification and identify the corresponding structure for that function." Biomedino, LLC v. Waters Techs. Corp., 490 F.3d 946, 950 (Fed.Cir.2007). To be a "corresponding structure," the specification or prosecution history must clearly link or associate the structure to the function recited in the claim. Medtronic, Inc. v. Advanced Cardiovascular Systems, Inc., 248 F.3d 1303, 1311 (Fed.Cir.2001) (quoting B. Braun Med., Inc. v. Abbott Labs., 124 F.3d 1419, 1424 (Fed.Cir.1997)).

2. Claim Construction

In claim 21, the three "means" elements are inter-related. In addition to the recited function, the "timing control means" receives "said video signal from said video source at a video signal data rate." '096 Patent, col. 31, line 21-col. 32, line 6.

The "image size/position control means" is "in electrical communication with said timing control means" and is, *inter alia,* "responsive" to various signals generated by the "timing control means." '096 Patent, col. 32, lines 7-13.

The "frame buffer output control means" is "in electrical communication with [1] said timing control means, [2] said memory system, [3] said image size/position control means, and [4] said flat panel display," and is further "responsive" to a "pixel clock signal" called for in connection with the "image size/position control means." '096 Patent, col. 32, lines 14-19.

a) "timing control means"

(1) The Parties' Positions

LG	***Hitachi***
This limitation is a "means-plus-function" clause under 35 U.S.C. s. 112(6).	This limitation is a "means-plus-function" clause under 35 U.S.C. s. 112(6).
Recited Function:	*Recited Function:*
(1) generating from the video signal enable, vertical synchronization, horizontal synchronization, and first clock signals for driving said flat panel display	(1) generating from the video signal enable, vertical synchronization, horizontal synchronization, and first clock signals for driving said flat panel display
(2) generating column start, row start, column replicate, and row replicate control signals for sizing said video image while maintaining a video signal resolution; and	(2) generating column start, row start, column replicate, and row replicate control signals for sizing said video image while maintaining a video signal resolution

(3) generating first control signals for reading said video image in said memory system.	(3) generating first control signals for reading said video image in said memory system.
Corresponding Structure:	*Corresponding Structure:*
Microprocessor 36, sync separator 14, and flat panel timing generator 29 (of Figures 1, and 7, including equivalents thereof)	(1) Flat panel timing generator 29 (including all the structure shown in Figure 7) and sync separator 14 (2) Microprocessor 36
	(3) Microprocessor 36

See Dkt. No. 64, at 37.

LG contends its construction reduces the number of disputed terms. Dkt. No. 47, at 60. According to LG, Hitachi "impermissibly attempt[s] to apportion the above-identified structures selectively to the recited functions contrary to the teachings of the specification." *Id*. LG contends "both the schematic of Figure 1 and the description of the invention (*see, e.g.,* Col.11:40-49) indicate the structures above are interrelated and cannot be separated in the manner attempted by the Defendants in their construction." *Id*.

Hitachi urges that "the only difference between the parties' construction of the recited functions relates to the word 'therefrom' * * * [which] refers back to 'the video signal' recited in the preamble of claim 21." Dkt. No. 48, at 4. Hitachi notes that "[i]n the joint filing, [LG] agreed with Defendants that 'therefrom' meant 'from the video signal,' " but LG's "newly-revised construction backs away from the parties' agreement." *Id*. Hitachi argues "it is vague as to whether the structure in Figure 7 is required (as opposed to non-descript, generic 'black box' shown in Figure 1)," but "if the Court were to find that the only structure clearly linked to the recited function is the 'black box' of Figure 1, the claim is invalid." *Id*. at 4 (citing Default Proof Credit Card Sys., Inc. v. Home Depot U.S.A., Inc., 389 F.Supp.2d 1325, 1353 (S.D.Fla.2004), aff'd, 412 F.3d 1291 (Fed.Cir.2005)).

Next, Hitachi argues that LG's "construction implies that there are two different or alternate embodiments of structure, the 'black box' in Figure 1 ***or*** all the circuitry of Figure 7," which will "confuse the jury." Dkt. No. 48, at 4. Hitachi urges that "[t]he proper construction should specify that all of the circuitry in Figure 7 is the structure required to perform the recited function." *Id*. at 5. Finally, Hitachi asserts that LG's construction "fails to specifically link each recited function with its corresponding structure * * * [b]y lumping all of the functions and all of the corresponding structures together." Hitachi concludes that "[t]he proper construction should be clear as to which structure is associated with each function." *Id*.

In response, LG contends that "[t]he parties largely agree on this term," but urges that the construction of "therefrom" within the context of the 'timing control means' language" means that "the requirement that the timing control means generate 'from the video signal' would be part of the claim." Dkt. No. 55, at 52. With respect to structure, LG urges that Hitachi "improperly restrict[s] the scope of the claims by demanding a one-to-one correspondence between the claim's substructures and subfunctions." *Id*. LG concludes that "[t]he circuits operate together to generate a functional output; it would be wholly improper to parse the correspondence in the manner suggested by Defendants." *Id*. Finally, LG argues that "the identity of the structures that correspond to the functions is clear to everyone." *Id*.

In its surreply, Hitachi urges that "[f]or all three of the means-plus-function limitations, LGE continues to identify a generic 'black box' from Figure 1 as corresponding structure from the specification for performing the recited function," but "generic 'black boxes' are not corresponding structure as a matter of law." Dkt. No. 63, at 1-2. According to Hitachi, "[e]ven though the claimed interconnections of claim 21 must be met in order for a circuit to be within the scope of claim, the generic 'black boxes' of Figure 1 do not show structure and thus cannot be corresponding 'means' structures from the specification." *Id*. at 2.

(2) Construction

[14] The parties agree that this phrase should be construed as a means-plus-function limitation under s. 112(6). This phrase recites the word "means" followed by a functional recitation, *i.e.,* "timing control means * * * for generating * * *," and is thus presumptively a means-plus-function limitation.

Neither the term "control," nor the other modifier "timing" connotes sufficient structure to remove this phrase from the ambit of s. 112(6). *See* Biomedino, LLC v. Waters Technologies Corp., 490 F.3d 946, 949-50 (Fed.Cir.2007).FN11 The Court thus agrees with the parties that this phrase should be construed as a means-plus-function limitation.

FN11. "As an initial matter, we address Biomedino's assertion that use of the term 'control' to describe 'means' takes the phrase 'control means' outside the realm in which s. 112, para. 6 applies. This argument is based on the premise that 'control means' recites sufficient structure on its own such that it obviates the need for s. 112, para. 6. Biomedino argues that a 'control' is a precise structure well understood by those of skill in the art, and thus, the word 'means' in claims 13 and 40 can be ignored. Additionally, Biomedino contends that 'control' is analogous to the term 'controller' and conveys, to one skilled in the art, structure for controlling the valves and other equipment. We disagree. When a claim uses the term 'means' to describe a limitation, a presumption inheres that the inventor used the term to invoke s. 112, para. 6. Altiris, Inc. v. Symantec Corp., 318 F.3d 1363, 1375 (Fed.Cir.2003). 'This presumption can be rebutted when the claim, in addition to the functional language, recites structure sufficient to perform the claimed function in its entirety.' *Id*. Claims 13 and 40 recite no such structure. As the district court noted, the 'reference to 'control' is simply an adjective describing 'means:' [sic] it is not a structure or material capable of performing the identified function.' *Biomedino,* slip op. at 12. We agree with the district court and hold that Biomedino has not rebutted the presumption that s. 112, para. 6 applies to 'control means.' " Biomedino, 490 F.3d at 949-50.

With respect to "timing control means receiving said video signal from said video source at a video signal data rate," the parties agree that the functions are three-fold, *i.e.,*

[A] generating therefrom enable, vertical synchronization, horizontal synchronization, and first clock signals for driving said flat panel display,

[B] generating column start, row start, column replicate, and row replicate control signals for sizing said video image while maintaining a video signal resolution,

and

[C] generating first control signals for reading said video image in said memory system

'096 Patent, col. 31, line 59-col. 32, line 19 (reordering, paragraphing, and numbering added). That is what the claim recites, and the Court agrees with the parties.

Turning to identifying the "corresponding structure," the Court agrees with Hitachi that each part of the recited function must find "corresponding structure" in the specification. *See* Default Proof, 412 F.3d at 1298 ("A structure disclosed in the specification qualifies as "corresponding" structure only if the specification or prosecution history clearly links or associates that structure to the function recited in the claim."); B. Braun, 124 F.3d at 1424 ("We hold that, pursuant to this provision, structure disclosed in the specification is 'corresponding' structure only if the specification or prosecution history clearly links or associates that structure to the function recited in the claim. This duty to link or associate structure to function is the quid pro quo for the convenience of employing s. 112, para. 6."). The Court thus must identify the "corresponding structure" disclosed in the specification that is "clearly linked" to the claimed function. In the context of the current limitation, though, the Court disagrees with Hitachi that a proper construction requires associating individual "structures," or "sub-structures" with each of the multiple functions performed by the "timing control means," for example, associating microprocessor 36 with the "generating column start * * * " and "generating first control signal * * * " functions.

Thus, the limitation calls for "timing control means" that collectively performs the three "generating" functions previously noted. The disclosed "corresponding structure" for the "means," of course, is not necessarily limited to a single structure. *See* Cardiac Pacemakers, Inc. v. St. Jude Med., Inc., 296 F.3d 1106, 1119 (Fed.Cir.2002) ("It remains true, of course, that corresponding structure need not include all things necessary to enable the claimed invention to work. It is equally true, however, that corresponding structure must include all structure that actually performs the recited function."). Accordingly, several structures or sub-structures as a group may be "clearly linked" to the overall claimed function by being clearly linked to one or more of the "generating" functions that together are performed by the claimed "timing control means."

In short, when a claim recites a "means" for performing multiple functions, the "corresponding structure" may be a single device or circuit, or may be multiple devices and circuits that together cooperate to perform the recited functions. In the latter instance, although proper construction of a means-plus-function limitation requires the Court to review the specification and determine which devices and circuits are "clearly linked" to the several functions, the ultimately identified "corresponding structure" is the group of devices and circuits that cooperate to perform the claimed multiple functions.

A patent drafter can, of course, provide otherwise. For example, here the drafter could have called for "timing control means" that included separate "means" for each of the three generating functions. But that was not what the patent drafter did in this claim. Thus, while the Court agrees with Hitachi that the specification must disclose "corresponding structure" for each of the multiple functions of the "timing control means," the Court disagrees that the claim language requires parsing the ultimately determined "corresponding structure" into "sub-structures," keyed individually to each of the several generating functions.

According to function [A], four types of signals are generated from the video signal, namely, (i) "enable" signals, (ii) "vertical synchronization" signals, (iii) "horizontal synchronization" signals and (iv) "first clock signals." From the grammar and structure of the recited function, all four signals appear to be for "driving" a flat panel display. Figure 1 FN12 shows the "flat panel timing generator 29" as ultimately sending those four

signals (on lines "en" 31, "clk" 32, "vsync" 33 & "hsync" 34) to the flat panel display. *See* ' 096 Patent, col. 6, line 63-col. 7, line 2 ("The [plug-in flat panel interface] module 30 * * * receives four inputs from generator 29, including a display enable signal on line 31, a clock signal on line 32, a vertical sync signal on line 33, and a horizontal sync signal on line 34.").

FN12. *See supra* Part II.A.2 for a reproduction of Figure 1.

Figure 4 is said to graphically illustrate these generated signals:

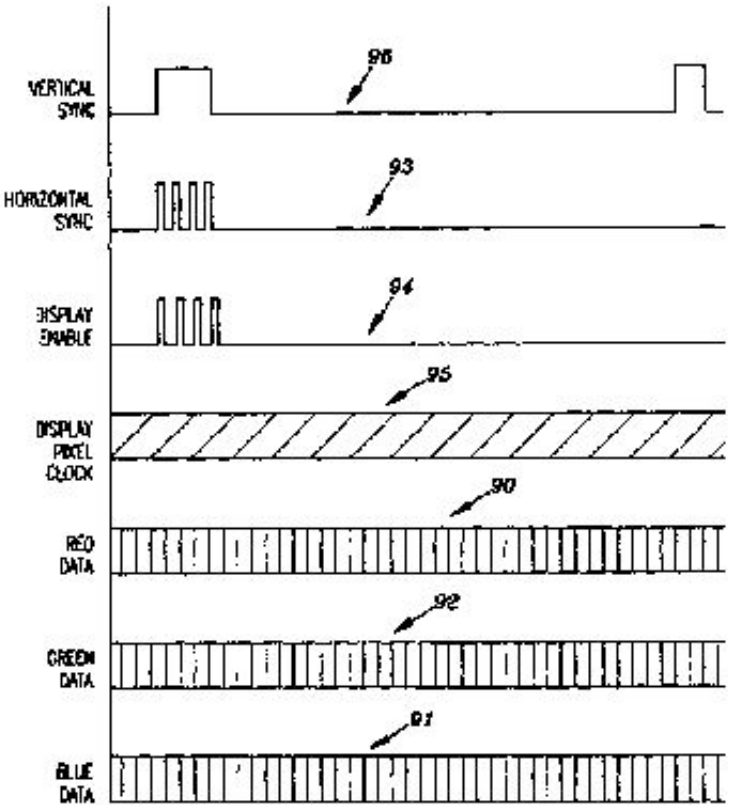


FIG. 4

See '096 Patent, col. 14, lines 50-57 ("Fig. 4 illustrates graphically the electronic signals which are applied by the electronics control system of Fig. 1 to the Plug-In Flat Panel Interface Module 30. More particularly, the digital signals 90, 91 and 92 respectively are supplied by buffers 20, 24 and 25 of Fig. 1. Further, the waveforms 93, 94, 95 and 96 of FIG. 4 are supplied by the flat panel timing generator 29 respectively to lines 34, 31, 32 and 33 of FIG. 1 leading to inputs of the module 30.").

The vertical synchronization and horizontal synchronization signals in Figure 1 appear to originate from the "synch separator 14." According to the specification, "[t]he sync separator 14 separates out the video vertical and horizontal sync signals from the composite video sync signal received from the connector 10." FN13 ' 096 Patent, col. 6, lines 8-10. *See also* id. at col. 14, lines 5-8 ("As before stated, the sync separator 14

extracts the horizontal sync and vertical sync signals from the video signal, and provides the sync signals at voltage levels compatible with the electronic control system of Fig. 1."). The specification explains that the sync separator "receive[s] the composite video signal from the plug-in video input connector 10" along with the "sync detector 13," which "detects sync signal parameters such as sync voltage level, sync width, number of serrations, and pulse width to lock onto a video sync signal." The sync separator apparently interacts with the sync detector as follows:

FN13. Specifically, "the sync separator 14 removes the negative polarity synchronization component of the video signal of waveform 70, and produces separated sync signals." '096 patent, col. 14, lines 24-26.

The sync detector 13 also receives information such as sync voltage level, sync width, and number and width of serrations from the sync separator 14, which in turn has received all sync separation/detection information from the system microprocessor 36. When the detector 13 is locked onto a sync signal, the detector informs the sync separator 14 by way of line 26. *The video input connector 10 then routes the synchronization signals (whether composite or separate) to the separator 14, which separates the vertical and horizontal sync signals from the incoming video signal*. Further, the connector routes a digital code by way of line 10a to the microprocessor 36 to identify the type of the video signal being received. In response thereto, the microprocessor supplies the separator 14 with timing parameters such as horizontal and vertical sync timing, polarities, and pulse widths. *The separator 14 thereupon extracts the horizontal and vertical sync signals from the video signal*
'096 Patent, col. 6, lines 11-27 (emphasis added). The specification then describes the path of the horizontal and vertical sync signals from the sync separator to the flat panel timing generator:
A vertical sync signal at a first output of the separator 14 is applied to a first input of a frame buffer input control unit 27, to a first input of a pixel clock generator 28, and to a first input of a flat panel timing generator 29. A horizontal synchronization signal at a second output of the sync separator 14 is applied to a second input of the generator 28, to a second input of the generator 29, and to a second input of the control unit 27. The output of the generator 28 in turn is connected to a third input of the control unit 27, and to a third input of the generator 29.

'096 Patent, col. 6, lines 27-37. *See also* id., at col. 15, lines 55-63 ("The microprocessor steps are as follows in the order given: first energize the power control circuits 53 to power up the flat panel display by way of line 55, then *apply the synchronization signal outputs of sync separator 14 by way of the flat panel timing generator 29 to the flat panel interface module 30,* next apply the outputs of frame buffers 20, 24, and 25 to the flat panel interface module 30, then cause the power control circuits 53 to energize the backlight inverter power supply 58.") (emphasis added).
With respect to the enable and clock signals, the specification describes those as originating from the flat panel timing generator. *See* '096 Patent, col. 6, lines 55-61 ("The flat panel timing generator 29 comprises counters and timers necessary to generate control *timing signals to drive the flat panel display*. The generator 29 also creates correct timing signals for fitting an image on the display screen being used, and enables and disables timing signals as the power to the electronic control unit of Fig. 1 is turned on and off.") (emphasis added). Figure 7 is said to "illustrate[ ] the logic circuit of the flat panel timing generator 29:"

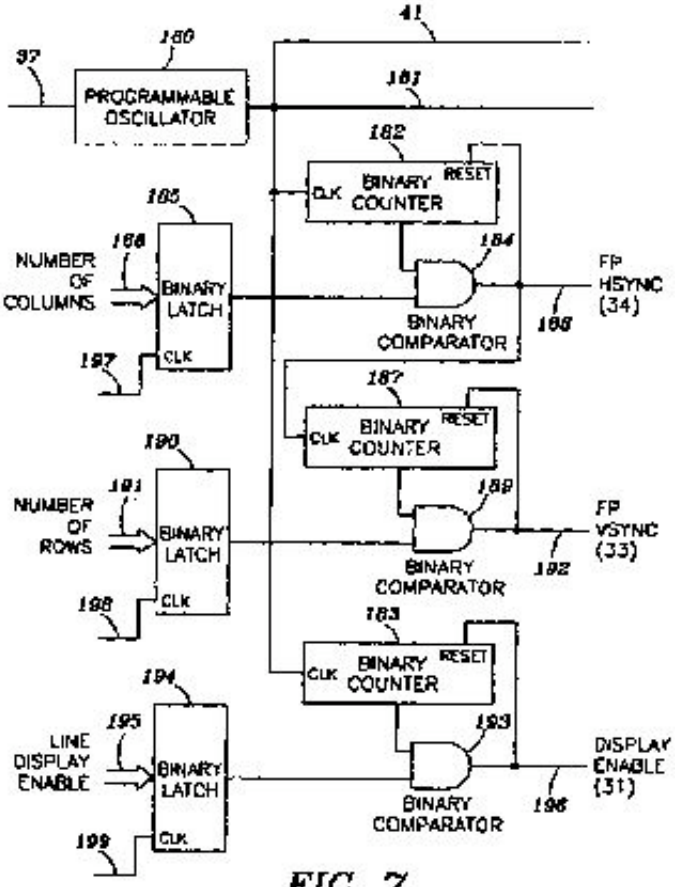


FIG. 7

The specification explains that the "programmable oscillator 180" of the flat panel timing generator generates the "clock signals:"

[A] programmable oscillator 180 receives a programming code from microprocessor 36[FN14] by way of line 37 of FIG. 1. In response thereto, *the oscillator generates a flat panel pixel clock on line 181 of FIG. 7 which is supplied by way of line 32 to one input of the flat panel interface module 30, and by way of line 41 to one input of the image size/position control unit 39. This clock signal is the same clock signal as that used to create the flat panel timing,* and also is used to create frame buffer memory addresses of output video data. In this manner, data is presented to the flat panel interface module 30 at the precise time that the input timing signals require.

FN14. The specification explains that the code comes from the flat panel interface module (30):
The module 30 provides a unique code on line 35 to the microprocessor 36 to establish the specific timing needed for the flat panel display that is being used. The microprocessor has stored therein a complete set of flat panel data and timing parameters for each flat panel interface module plug-in that may be used.

'096 Patent, col. 13, lines 2-7. "Upon reading the flat panel interface module 30 code on line 35 to determine flat panel type, size and resolution, the microprocessor controls the timing generator 29 * * *." ' 096 Patent, col. 13, lines 12-16.
'096 Patent, col. 20, lines 55-66 (emphasis added). The specification explains how that works "in operation," and how the enable signal is generated:

In operation, the programmable oscillator 180 receives a programming code from the microprocessor 36 on line 37, and in response thereto the oscillator generates a flat panel pixel clock signal on lines 41 and 181. * * * * The programmable oscillator 180 also can accommodate flat panel displays with pixel clock rates up to 230 MHz.

The clock input to the counter 183 is supplied by the oscillator 180, and when the output of the counter 183 is equal to the output of latch 194, *the binary comparator 193* resets counter 183 and *issues a display enable signal on line 196*. The display enable signal is required by a number of flat panel displays to provide correct horizontal positioning on the display screen.

'096 Patent, col. 21, lines 28-58 (emphasis added). Thus, as the parties agree, the sync separator (14) and flat panel timing generator (29) appear to be structure "clearly linked" to the recited function of "receiving said video signal from said video source at a video signal data rate for generating therefrom enable, vertical synchronization, horizontal synchronization, and first clock signals for driving said flat panel display."

With respect to function [B], namely, "generating column start, row start, column replicate, and row replicate control signals for sizing said video image while maintaining a video signal resolution," the specification explains, in connection with Figure 8, that the "microprocessor 36" (*see* Figure 1) generates those signals. Figure 8 FN15 is said to illustrate "[t]he logic schematic diagram of the image size/position control unit 39." According to the specification, the image size/position control unit 39 receives from the microprocessor 36:(i) an "image column start signal," (ii) an "image row start signal," (iii) a "column replicate value" signal, and (iv) a "row replicate value" signal. *See* ' 096 Patent, col. 21, lines 64-67 ("A second input of the gate 200 is connected to the output of a binary latch 202, which receives an image column start signal from the microprocessor 36 on cable 203."); id. at col. 22, lines 16-20 ("The binary latch 210 receives an image row start value from the microprocessor on bus 214 * * *."); id. at col. 22, lines 7-9 ("A second data input of the adder 205 is connected to the output of a binary latch 208, which receives a column replicate value on bus 209 from microprocessor 36."); id. at col. 22, lines 17-20. ("[A] second input of the adder 213 is connected to the output of a binary latch 215, the data input of which receives a row replicate signal from the microprocessor by way of bus 216."). "In operation," the specification explains, "the image size/position control unit 39 provides image positioning, image size, and image orientation by modifying the memory addresses that are presented to the frame buffers 20, 24, and 25. The *microprocessor 36 writes a column starting position* into latch 202, the output of which enables the counter 201. The *microprocessor also writes a column replicate value on bus 209* into latch 208, an *image row start value into latch 210* by way of bus 214, and a *row replicate value into latch 215* by way of bus 216. The information stored in the latches 202, 208, 210 and 215 are clocked to the latch outputs by clock signals issued by the microprocessor 36 respectively on lines 218, 219, 220 and 221." ' 096 Patent, col. 22, lines 25-37 (emphasis added). Thus, the microprocessor 36, as the parties agree, is structure "clearly linked" to the function of "generating column start, row start, column replicate, and row replicate control signals for sizing said video image while maintaining a video signal resolution."

FN15. *See supra* Part II.B.2(f) for a reproduction of Figure 8.

With respect to function [C], namely, "generating first control signals for reading said video image in said memory system," that phrase was construed above. As discussed there, the "first control signals" are generated by microprocessor 36.

Thus, the Court agrees with the parties that the structure "corresponding" to these functions is microprocessor 36, sync separator 14, and flat panel timing generator 29 (as shown in Figs. 1, and 7.

Finally, Hitachi makes a "black box" argument with respect to Figure 1. Certainly, "failure to disclose adequate structure corresponding to the recited function in accordance with 35 U.S.C. s. 112, paragraph 1, results in the claim being of indefinite scope, and thus invalid, under 35 U.S.C. s. 112, paragraph 2." Budde v. Harley-Davidson, Inc., 250 F.3d 1369, 1376 (Fed.Cir.2001). In *Biomedino,* the Federal Circuit construed the phrase "control means for automatically operating said valving" as a means-plus-function limitation, and held that the "black box" labeled "control" in a drawing figure and a statement in the written description "that the regeneration process may be 'controlled automatically by known differential pressure, valving and control equipment,' " failed to disclose structure corresponding to the recited function of "automatically operating said valving." *See* Biomedino, 490 F.3d at 950, 953. But here the specification provides, in some cases, additional figures that disclose significantly more detail (Figure 7), than what is shown in Figure 1. The point is that although the boxes illustrated in Figure 1 may be insufficient *per se* to constitute "structure," they represent the structure described in more detail elsewhere in the specification and they also illustrate interconnections between the boxes.

The Court concludes that the limitation "timing control means receiving said video signal from said video source at a video signal data rate for generating therefrom enable, vertical synchronization, horizontal synchronization, and first clock signals for driving said flat panel display, generating column start, row start, column replicate, and row replicate control signals for sizing said video image while maintaining a video signal resolution, and generating first control signals for reading said video image in said memory system" should be construed as a means-plus-function limitation under s. 112**(6)**.

The recited function is "generating therefrom enable, vertical synchronization, horizontal synchronization, and first clock signals for driving said flat panel display, generating column start, row start, column replicate, and row replicate control signals for sizing said video image while maintaining a video signal resolution, and generating first control signals for reading said video image in said memory system."

The "corresponding structure" disclosed in the specification for performing that function is microprocessor (36), sync separator (14) and the flat panel timing generator (29), as illustrated in Figure 7. Under the terms of s. 112**(6), therefore, the limitation should be construed to cover this corresponding structure and any equivalent structures.**

b) "image size/position control means"

(1) The Parties' Positions

LG	***Hitachi***
This limitation is a "means-plus-function" clause under 35 U.S.C. s. 112(6).	This limitation is a "means-plus-function" clause under 35 U.S.C. s. 112(6).
Recited Function:	*Recited Function:*

generating output column address and output row address control signals.	(1) generating output column address control signals for said memory system (2) generating output row address control signals for said memory system (3) generating a pixel clock signals.
Corresponding Structure: the circuitry described as the image size/position control unit 39 of Figs. 1 and 8 and any equivalents thereof.	*Corresponding Structure:* (1) image/size position control unit 39 (including all the structure shown in Figure 8). (2) imagine/size position control unit 39 (including all structure shown in Figure 8).
	(3) no corresponding structure that performs this function and satisfies the remainder of this limitation.

See Dkt. No. 64, at 33.

According to LG, "[t]he dispute here revolves around whether the last clause of this element-'generating a pixel clock signal'-is a signal that is received or generated by the claimed 'image size/position control means.' " Dkt. No. 47, at 55. In LG's view, Hitachi "simply seek[s] to bootstrap the latter claim construction into an argument that the claim is somehow not supported by the specification." *Id*.

LG urges that "image size/position control unit 39, as disclosed in Figure 8, does not generate a pixel clock signal, but rather receives a pixel clock signal that is used to perform its proper functions of generating output column address control signals and output row address control signals." Dkt. No. 47, at 55-56. Alternatively, LG contends, "if the generation of a pixel clock signal is a function as urged by defendants, then it is completely clear what structure in the specification corresponds to that function," *i.e*., pixel clock generator 28. *Id*. at 56. Either way, LG asserts, "the claim language is completely supported." *Id*.

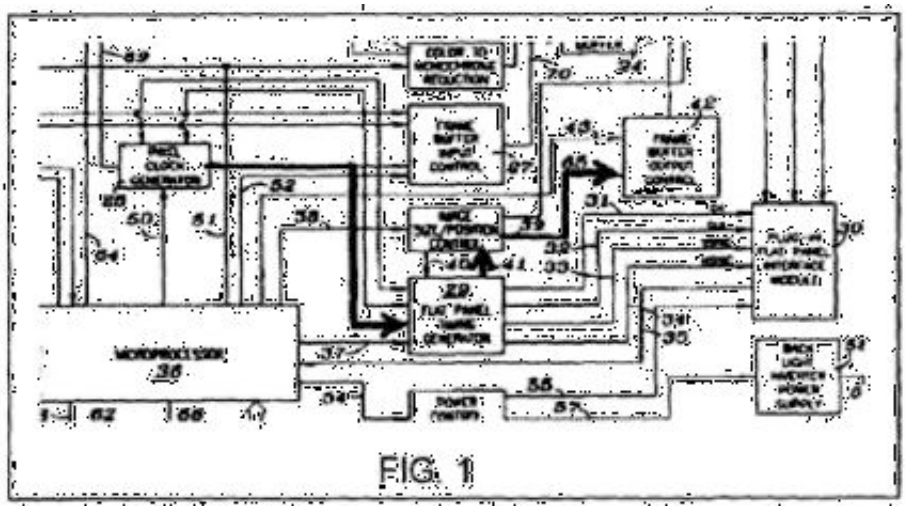
Hitachi argues that "[n]o structure is disclosed in the specification that performs the function of 'generating a pixel clock signal,' rendering claim 21 invalid." Dkt. No. 48, at 6. Hitachi also accuses LG of attempting "to first identify structure that is disclosed in the specification, and then rewrit[ing] the claimed function consistent with the structure it identified," which is clear error. *Id*. at 6 (citing Omega Eng'g, Inc. v. Raytek Corp., 334 F.3d 1314, 1330 (Fed.Cir.2003)).

Hitachi also contends that LG "reorganizes the language of claim 21 in an effort to read the 'generating a pixel clock signal' function out of the 'image size/position control means' means-plus-function clause," and urges that "the clause itself, as it exists in claim 21 of the patent, clearly includes the 'generating a pixel clock signal' function within the 'image size/position control means' limitation," because, as is "common

practice in patent claim drafting, distinct clauses within claim 21 are separated by a semicolon, not a comma." Dkt. No. 48, at 6-7. Hitachi urges that "[t]he use of the comma before 'and a pixel clock signal' (as before each of the other signals in the limitation) and a semicolon after that same phrase, is clear indication that the 'pixel clock signal' is the last item in the list of three signals that are generated by the 'image size/position control means': output column address control signals, output row address control signals, and a pixel clock signal." *Id*. at 7.

In response, LG argues that its construction is supported by Figure 8, which "shows the same six groups of inputs * * *." Dkt. No. 55, at 47. LG also urges that "Defendants 'identification of the comma before' and a pixel clock signal 'and semicolon after, also supports [LG's] contention that the limitation is the last item in the list of six inputs to which the image size/position control means is responsive." *Id*. at 47-48.

LG suggests that "[i]f the Court agrees with Defendants that this term would be invalid if construed to require generation of a pixel clock signal, the Court should adopt the equally supportable construction set forth above by LGE to avoid invalidating the claim, * * * [though] if the Court determines that generation of a pixel clock signal is a function of this claim term, it is clear that there is structure in the specification to support it. LG asserts that" [t]here are several structural examples in the specification that are clearly linked to the recited pixel clock signal generation. "Dkt. No. 55, at 48. For example," [a]s seen in the annotated figure below, control unit 42 receives a pixel clock signal from the image size/position control unit 39 via line 65, "which" is used by the frame buffer output control unit 42 for reading the video image from the memory, and used by the image size/position control unit 39 to generate output column and row address control signals:



Id. at 48-49. LG notes that "[t]he pixel clock signal arrives at image size/position control unit 39 via line 41 from the flat panel timing generator 29, which is in turn connected with pixel clock generator 28." *Id*. at 48.

In its surreply, Hitachi contends that "LGE provides the new argument that the 'image size/position control means' is responsive to six signals, number (5) of which is 'said first control signals for generating output column address control signals, output row address signals for said memory system.' Thus, LGE simultaneously contends that the 'means' structure of this limitation (a) generates output column and row

address signals (LGE's recited function), and (b) is responsive to the same output column and row address signals. The circuitry in Figure 8 cannot be generating these address signals and also [sic] responsive to the same address signals." According to Hitachi, "LGE itself cannot reconcile the structure disclosed in the specification to the requirements of this means-plus-function limitation of claim 21, implicitly conceding that the claim fails the requirements of Section 112." Dkt. No. 63, at 3. Hitachi urges that "if the 'image size/position control means' is *not* generating the 'pixel clock signal,' then claim 21 is invalid because it fails to recite any structure that does so." *Id*. In Hitachi's view, "LGE's argument is also inconsistent with the format and sequence found in the other means-plus-function clauses of claim 21, both of which follow the same format: they first recite the signals to which the 'means' is responsive; then they finish with a recitation of the signals generated by the 'means .' " *Id*. at 4.

Hitachi further contends that LG's annotated figure and its explanation are "not correct." Dkt. No. 63, at 5. According to Hitachi, the "signal on line 41 in Figure 1 * * * is not generated by the 'pixel clock generator,' " but rather is "generated by a 'programmable oscillator' 180 based on the input on line 37." *Id* . Hitachi urges that the "input on line 37 does not come from the 'pixel clock generator'; instead it comes from microprocessor 36, as shown in Figure 1," which Hitachi has annotated:

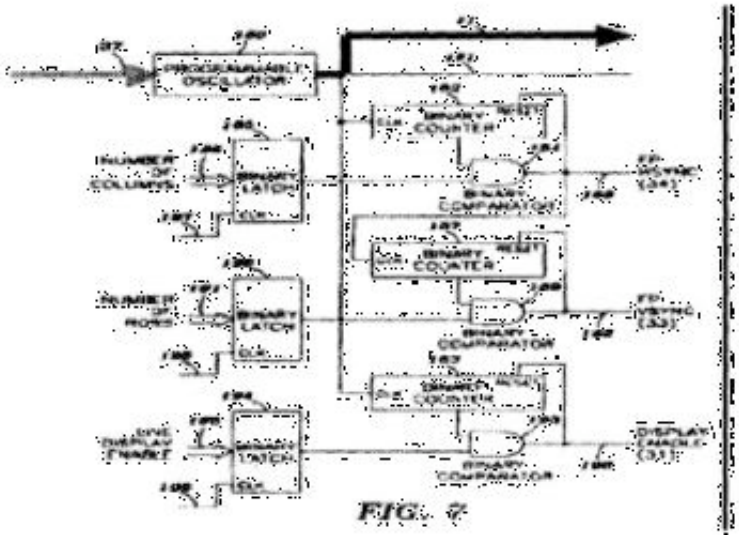


FIG. 8

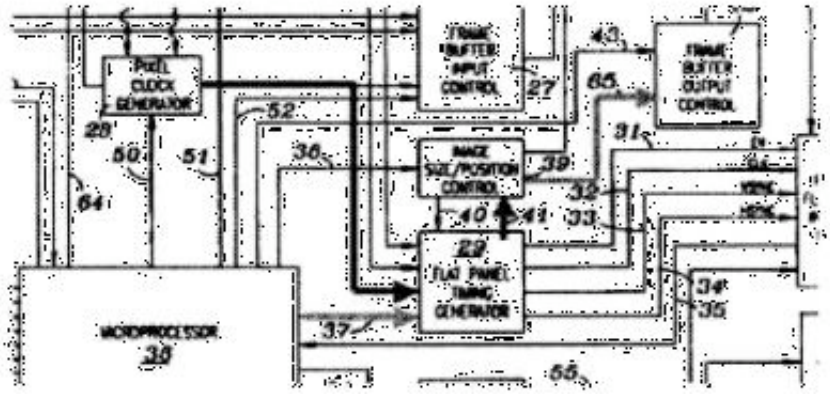


Figure 1

Id. at 5-6. Hitachi argues:

According to claim 21, the "image size/position control means" must generate a "pixel clock signal." LGE points to the "pixel clock signal" shown in red in the corrected version of Figure 1 above, but that signal is generated by the "pixel clock generator," not by the "image size/position control means." Contrary to LGE's reply brief, the red signal shown above does not get passed through the "flat panel timing generator" to the "image size/position control" and then to the "frame buffer output control." The signal on line 41 (blue in the above Figures) is generated by a programmable oscillator based on the green signal on line 37, which comes from the microprocessor, not the "pixel clock generator." Nor is the "frame buffer output control means" responsive to the red signal from the "pixel clock generator," as required by claim 21. Instead, the "frame buffer output control means" receives the orange signal in the annotated figure above, which is substantively different than the output of "pixel clock generator 28."

Id. at 6. According to Hitachi, "[c]laim 21 simply fails to specifically and unambiguously link any structure in the specification to the function of 'generating a pixel clock signal' that also satisfies the rest of claim 21, which requires such structure (1) to be part of the 'image size/position control means,' (2) to be responsive to certain other specified signals, and (3) to which the 'frame buffer output control means' is responsive." *Id* . at 6-7. Thus, Hitachi contends claim 21 is invalid, and the "Court can and should reach that conclusion within the context of claim construction." *Id*. at 7.

After the *Markman* hearing, LG submitted a supplemental claim construction brief, arguing that Hitachi "gave short shrift in their briefing to the supposed invalidity issue," and "have urged this Court to invalidate claim 21-not in a trial setting or even on summary judgment (with the proper evidentiary burdens in place) but simply in the *Markman* process-in an invalidity 'free for all' with no regard for the presumption that the Patent Office performed its duties correctly and without any consideration for the proper construction of the claims, which sinks their indefiniteness challenge." Dkt. No. 74-3, at 5. According to LG, Hitachi's "sole argument here is that there is purportedly no structure disclosed in the specification that corresponds to the functional language 'generating a pixel clock signal' with respect to the 'image size/position control means.' " *Id*. LG urges that "[t]here is ample structure disclosed for performing this function, including but not limited to timing signal generators described in the 'flat panel timing generator 29' and the interconnected 'pixel clock generator 28' shown in Figure 1. *Id*. For example, as seen in LGE's slides and the '096 patent specification, the 'image size/position control unit 39' directly provides the 'frame buffer output control unit

42' with a pixel clock signal on line 65, from a structure such as oscillator 180 of the flat panel timing generator 29. The pixel clock signal may be used to drive the flat panel timing and to create the memory addresses for reading the video image from the frame buffer memory system." Id. at 5-6. LG further urges that "the patent even goes so far as to specifically identify an exemplary structure for the 'pixel clock generator 28' in Table IX of the patent at Column 13, lines 30-60, wherein the device is identified as being manufactured by Integrated Circuit systems, Inc. with the specific part number." Id. at 6.

Also, LG contends that Hitachi's reliance on PureChoice, Inc. v. Honeywell Int'l Inc., No. 2:06-CV-244, 2008 WL 190317 (E.D.Tex. Jan. 22, 2008) is misplaced because:

contrary to the rationale of *PureChoice,* the claim term at issue is well supported in the patent as shown above; thus, the result there is wholly irrelevant. Beyond that, the procedural history of the terms at issue in *PureChoice* is notably distinct from the terms at issue in claim 21 of the ' 096 patent. The claim terms at issue in *PureChoice* were the result of a lengthy prosecution and, then, a reexamination that was merged with a reissue proceeding.

Dkt. No. 74-3, at 6. According to LG, "even one of the inventors [in *PureChoice*] could not explain the meaning of the term at issue." *Id*. at 7. Here, LG argues, "the intrinsic record clearly provides guidance on how to properly construe the claim terms at issue, and any request to invalidate claim 21 now should be resoundingly rejected." *Id*.

Hitachi replies that "[t]he question is whether the '096 patent specification discloses structure that corresponds to the function of 'generating a pixel clock signal' **and** whether such structure meets the rest of the claim." Dkt. No. 77, at 3-4. Hitachi urges that "the 'frame buffer output control means' must be responsive to the pixel clock signal, and that same pixel clock signal must be generated by the 'image size/position control means.' " *Id*. at 4. Hitachi contends that "LGE has now advanced three different, mutually-inconsistent theories for where that structure is located," and that "[a]ll three theories are wrong." *Id*. at 3.

According to Hitachi, "LGE's first argument that the 'image size/position control means' of claim 21 is responsive to the 'pixel clock signal' is wrong," because claim 21 requires that the 'image size position control means' generate [ ] the pixel clock signal," and thus LG has "admitted that 'image size position control unit 39' of the '096 patent ***does not*** generate a pixel clock signal." Id. at 4-5.

As for "LGE's second argument that 'pixel clock generator 28' is the corresponding structure for 'generating a pixel clock signal,' " Hitachi urges that " 'pixel clock generator 28' cannot be the corresponding structure because it is not part of the 'image size/position control means' of claim 21," and "the signal generated by 'pixel clock generator 28' is not input into the 'frame buffer output control means' which claim 21 clearly requires must be 'responsive to' the pixel clock signal." Id. 5. According to Hitachi, LG "implies that the signal generated by 'pixel clock generator 28' is input into 'flat panel timing generator 29,' and that this same signal is fed out of 'flat panel timing generator 29' on line 41," but that "cannot be correct, because no signal generated by or derived from 'pixel clock generator 28' is passed through to the 'frame buffer output control means.' " Id. In Hitachi's view, "[l]ine 41 has nothing to do with 'pixel clock generator 28'-it is output from 'programmable oscillator 180,' which has a single input on line 37 from Microprocessor 36." Id. at 6.

Hitachi finally urges that LG's "third argument, that 'oscillator 180' is the corresponding structure for 'generating a pixel clock signal,' is also wrong" for two reasons. First, "everyone agrees that 'flat panel

timing generator 29' (including oscillator 180) corresponds to the 'timing control means,' not the 'image size/position control means." Id. at 6. Because "[d]ifferent claim terms in the same claim should not be construed to have the same meaning" and "[b]ecause claim 21 requires that the 'image size/position control means' generates this signal-not the 'timing control means'-oscillator 180 of 'flat panel timing generator 29' cannot be the structure corresponding to the 'generating a pixel clock signal' function." Id. Second, "the signal generated by oscillator 180 of 'flat panel timing generator 29' [and carried on lines 41 and 32] is already identified by claim 21 as a 'first clock signal for driving said flat panel display,' " i.e., [t]he 'first clock signal' cannot be the same signal as the 'pixel clock signal,' and the signal generated by oscillator 180 of 'flat panel timing generator 29' therefore cannot be structure for 'generating a pixel clock signal.' " Id. at 7.

(2) Construction

[15] The parties agree that this phrase should be construed as a means-plus-function limitation under s. 112(6). This phrase recites the word "means" followed by a functional recitation, *i.e.,* "image size/position control means * * * for generating * * *," and is thus presumptively a means-plus-function limitation.

Neither the term "control," nor the other modifier "image size/position" connotes sufficient structure to remove this phrase from the ambit of s. 112(6). *See* Biomedino, 490 F.3d at 949-50. The Court thus agrees with the parties that this phrase should be construed as a means-plus-function limitation.

Turning to identification of the recited function, this limitation may be parsed as follows:

[A] image size/position control means

[B] in electrical communication with said timing control means and

[C] responsive to said column start, row start, column replicate, and row replicate control signals and said first control signals

[D] for generating output column address control signals, output row address control signals for said memory system, and

[E] a pixel clock signal;

'096 Patent, col. 32, lines 7-13 (paragraphing and numbering added). The parties agree that at least the limitations of [D] are recited function, but dispute whether the last phrase, *i.e.,* "and a pixel clock signal," should be part of [C], or part of [D]. In other words, the parties dispute whether the "image size/position control means" receives or generates the "pixel clock signal."

Of course, "[i]n identifying the function of a means-plus-function claim, a claimed function may not be improperly narrowed or limited beyond the scope of the claim language. Conversely, neither may the function be improperly broadened by ignoring the clear limitations contained in the claim language." Micro Chem., Inc. v. Great Plains Chem. Co., Inc., 194 F.3d 1250, 1258 (Fed.Cir.1999).

Typically, the phrase following the word "for" is the recitation of function. *See* Lockheed Martin v. Space Sys./Loral, Inc., 324 F.3d 1308, 1319 (Fed.Cir.2003) ("The phrase 'means for' generally invokes 35 U.S.C. s.

112 para. 6, and is typically followed by the recited *function and claim limitations*"). Here, the words following "for" are "generating output column address control signals, output row address control signals for said memory system, and a pixel clock signal."

However, both LG and Hitachi urge something different. LG's proposed function-"generating output column address and output row address control signals"-replaces the first comma with an "and," and drops both "for said memory system" and "and a pixel clock signal." Hitachi's proposed construction-(1) generating output column address control signals for said memory system; (2) generating output row address control signals for said memory system; and (3) generating a pixel clock signals-also essentially replaces the first comma with an "and" in assuming that the "for said memory system" language applies to both "output row address control signals" and "output row address control signals." LG does not appear to disagree with that part of Hitachi's proposed function.

There seems to be implicit recognition, therefore, that the punctuation of the phrase raises some ambiguity. The parties do not explain why the phrase "for said memory system" should append "output column address control signals." The specification, though, supports that, as discussed above in connection with the terms "output column address control signals" and "output row address control signals."

Thus, the parties have essentially construed the recited "generating output column address control signals, output row address control signals for said memory system" to mean: "generating output column address control signals *and* output row address control signals for said memory system."

That, of course, makes it difficult to view the ", and" that sets off the "pixel clock signal" as Hitachi urges. Nevertheless, grammatically, the "pixel clock signal" is more reasonably read as part of the list of address control signals generated by the "image size/position control means," as noted above. That is also consistent with the grammar structure of the other "means" phrases.

Thus, the function recited in the claim is "generating output column address control signals, output row address control signals for said memory system, and a pixel clock signal." *See* Micro Chem., 194 F.3d at 1258 (Section 112(6) "does not permit limitation of a means-plus-function claim by adopting a function different from that explicitly recited in the claim.").

The focus then turns to identifying the "corresponding structure," starting with the undisputed function "generating output column address control signals and output row address control signals for said memory system." As is clear from Figure 8 and the specification, and as discussed above in connection with construction of the terms "output column address control signals" and "output row address control signals," the image size/position control unit (39) is "clearly linked" to those functions-that is not in dispute. According to the specification (with reference to Figure 8), "[t]he output of the adder 205 is an output column address signal that is applied to bus 207," and "[t]he output of the adder 213 is an output row address which is supplied to a bus 217." ' 096 Patent, col. 22, lines 5-7; id. at col. 22, lines 20-22.

To confirm that construction, consider the non-functional limitations to the "image size/position control means." Claim 21 requires that the "image size/position control means" be "in electrical communication with said timing control means." The Court has, as discussed above, identified the microprocessor (36) as part of that "timing control means." In Figure 1, the image size/position control unit is shown to be "in electrical communication with" the microprocessor via line 38. The specification explains that "[i]n response to the control code supplied by the module 30 on line 35, the microprocessor 36 issues a programmable control

signal on a line 37 to a fourth input of generator 29, and *a control signal on a line 38 to one input of an image size/position control unit 39*." '096 Patent, col. 7, lines 41-45 (emphasis added). That is, the image size/position control unit receives a control signal from the microprocessor, thus meeting the "in electrical communication" limitation.

Claim 21 also requires the "image size/position control means" to be "responsive to said column start, row start, column replicate, and row replicate control signals and said first control signals." The first three signals are, as discussed above, generated by the "timing control means" to which the microprocessor 36 corresponds. As previously noted, the microprocessor sends a control signal on line 38 to the image size/position control unit. As discussed above in connection with the construction of the phrase "generating first control signals for reading said video image in said memory system," those "column start, row start, column replicate, and row replicate control signals" are carried on the control signal from the microprocessor. That is, the image size/position control unit is controlled by those four signals from the microprocessor and flat panel timing generator, thus meeting the "responsive to" limitation.

That leaves the final issue-identifying the structure corresponding to "generating * * * a "pixel clock signal." Hitachi urges that the specification does not disclose such structure, and LG urges that the structure is either the flat panel timing generator or the pixel clock generator.

The flat panel timing generator generates a pixel clock signal, albeit a flat panel clock signal. *See* '096 Patent, col. 20, lines 54-66 ("Fig. 7 illustrates the logic circuit of the flat panel timing generator 29, where a programmable oscillator 180 receives a programming code from microprocessor 36 by way of line 37 of FIG. 1. In response thereto, the oscillator generates a flat panel pixel clock on line 181 of Fig. 7 which is supplied by way of line 32 to one input of the flat panel interface module 30 * * *."). But, as discussed above, in connection with "timing control means," the pixel clock signals generated by the flat panel generator appear to refer to the "first clock signals" to which the image size/position control unit responds. Thus, that particular pixel clock signal does not appear to correspond to the claimed "pixel clock signal." In other words, the pixel clock signal from the flat panel timing generator appears to correspond to the claimed "first clock signals for driving said flat panel display" generated by the "timing control means," rather than to the "pixel clock signal" generated by the "image size/position control means."

That is consistent with Figures 7 (flat panel timing generator) and 8 (image size/position control unit), which were previously discussed.FN16 As can be seen from those figures, the pixel clock signal is provided on line 41 (top of both figures) from the flat panel timing generator to the image size/position control unit. *See* ' 096 Patent, col. 21, lines 59-64 ("The logic schematic diagram of the image size/position control unit 39 is illustrated in FIG. 8, where a flat panel pixel clock from the flat panel timing generator 29 is supplied on line 41 to one input of an AND gate 200, * * *.").

FN16. *See supra* Part II.C.2(a)(2).

However, the claim also requires that the "frame buffer output control means" (construed in a separate section below) be "responsive" to the pixel clock signal generated by the "image size/position control means." As construed below, the structure disclosed as corresponding to the function recited for the "frame buffer output control means" is the frame buffer output control unit (17) and FIFO (365). According to the specification, the pixel clock signal passes from the flat panel timing generator via image size/position control unit to the frame buffer output control unit, shown in Figure 17. FN17 *See* ' 096 Patent, col. 27, lines

45-49 ("Fig. 17 illustrates in logic schematic form the frame buffer output control unit 42 of Fig. 1. More particularly, a logic AND gate 500 receives a pixel clock signal on line 501 from the flat panel timing generator 29 by way of line 41, the image size/position control unit 39 and line 65 of Fig. 1."). But the image size/position control unit of Figure 8 does not appear to show a pixel clock signal output. Thus, there appear to be some discrepancies between the figures and the description of the flat panel timing generator, image size/position control unit and the frame buffer output control unit. Although construction of the phrase "timing control means * * * " appears to foreclose identification of the flat panel timing generator as part of the structure "corresponding" to the function recited for the "image size/position control means," the specification appears to leave open that possibility.

FN17. *See supra* Part II.B.2(f) for a reproduction of Figure 17.

Another structure disclosed in the specification that generates a pixel clock signal is pixel clock generator 28, as seen in Figure 1.FN18 That pixel clock generator provides input directly to the frame buffer input control unit 27 and the flat panel timing generator 29, but not, apparently, to the image size/position control unit 39. *See* ' 096 Patent, col. 12, line 60-col. 13, line 1 ("The synchronization signals supplied by the sync separator 14 are used by the pixel clock generator 28 to generate a synchronous pixel clock signal * * * The pixel clock and the synchronization signals also are used by the frame buffer input control unit 27 * * *.")

FN18. *See supra* Part II.A for the reproduction of Figure 1.

The specification also, as LG urges, provides exemplary products to serve as the pixel clock generator, *i.e.,* the "ICS1522" or "AV9173" disclosed in Table IX. '096 Patent, col. 13, lines 30-59. That is clearly structure that "generates * * * a pixel clock signal."

As for whether identifying the pixel clock generator as "corresponding structure" meets the other limitations of the claim, the pixel clock generator appears to be "in electrical communication" with the "timing control means" structure, *i.e.,* the sync separator (14), microprocessor (36) and flat panel timing generator (29). But it is not readily apparent from Figure 1 whether the "frame buffer output control means" structure, *i.e.,* the frame buffer output control (as discussed below), is responsive to a signal from a pixel clock generator, as claim 21 requires:

frame buffer output control means in electrical communication with said timing control means, said memory system, said image size/position control means, and said flat panel display, and *responsive to said pixel clock signal* for reading said video image from said memory system.

'096 Patent, col. 32, lines 14-19 (emphasis added). Figure 1 illustrates a signal passing from the pixel clock generator 28 to the flat panel timing generator via an unmarked line. Figure 7, which illustrates the flat panel timing generator (above), does not appear to show that signal. Rather, the oscillator 180 of the flat panel timing generator generates an apparently different pixel signal that is passed to the image size/position control unit via line 41. That signal and line appear in Figures 7 and 8. Thus, it is not clear how, or if, the flat panel timing generator actually uses the signal from the pixel clock generator. In any event, as noted above, the specification (including Figure 17) explains that the frame buffer output control unit receives some sort of pixel clock signal from the flat panel timing generator via the image size/position control unit. *See* '096 Patent, col. 27, lines 46-49 ("More particularly, a logic AND gate 500 receives a pixel clock signal

on line 501 from the flat panel timing generator 29 by way of line 41, the image size/position control unit 39 and line 65 of Fig. 1."). However, Figure 8 (the image size/position control unit) does not illustrate line 41, or any pixel clock signal, passing to the frame buffer output control from the image size/position control unit.

Obviously, a "line" may carry more than one signal. *See, e.g .,* '096 Patent, col. 4, lines 26-27 ("Line: As referred to herein, a line is an electrical conductor."); id. at col. 21, lines 28-34 (Referring to Figure 7: "In operation, the programmable oscillator 180 receives a programming code from the microprocessor 36 on line 37, and in response thereto the oscillator generates a flat panel pixel clock signal on lines 41 and 181. The microprocessor also loads the number of image columns and rows respectively in the latches 185 and 190, and a line display enable value into the latch 194."). The specification thus does not foreclose multiple pixel clock signals traveling on lines 41 and 65. Nevertheless, it is not readily apparent where the pixel clock signal into the frame buffer output control unit comes from, i.e., it is not readily apparent that a signal from the pixel clock generator is sent to the frame buffer output control (or FIFO 356).

The focus thus returns to the specification's disclosure of the image size/position control unit 39. The parties appear to agree-without discussion-that the image size/position control unit does not generate a "pixel clock signal." However, according to the specification, "[t]he *image size/position control unit 39 also creates a set of timing clocks* and control signals that are provided to a frame buffer output control unit 42, which in turn addresses memory locations in the frame buffers. * * * * The order in which data is read out of the frame buffers determines the form in which the image will be presented on the plat panel display screen. A *timing signal that controls the reading of data from the frame buffer memory* is output by control unit 39 to control unit 42 on line 65." '096 Patent, col. 8, lines 46-62 (emphasis added). That timing signal, though, does not appear to be illustrated in Figure 8 (image size/position control unit, above), nor does it appear to be discussed in connection with Figure 8. Nevertheless, that "timing signal" is disclosed as "create[d]," or generated, by the image size/position control unit, and, from the foregoing passage, appears to correspond to the "pixel clock signal" that the "frame buffer output control means" responds to in claim 21.

Also, it is worth noting that the specification sometimes refers to "pixel clock signals" as "timing signals." *Compare* '096 Patent, col. 6, lines 55-57 ("The flat panel timing generator 29 comprises counters and timers necessary to generate control *timing signals to drive the flat panel display*.") *with* id. at col. 20, lines 57-64 ("In response thereto, the oscillator generates a flat panel *pixel clock* on line 181 of FIG. 7 which is supplied by way of line 32 to one input of the flat panel interface module 30, and by way of line 41 to one input of the image size/position control unit 39. *This clock signal* is the *same clock signal as that used to create the flat panel timing,* and also is used to create frame buffer memory addresses of output video data.") (emphasis added). The specification thus supports viewing that "timing signal" or "clock" as the "pixel clock signal" generated by the "image size/position control means"-at least based on that part of the specification. Again, though, the specification describes the frame buffer output control unit as receiving a pixel clock signal from the flat panel timing generator, which appears to be inconsistent with the foregoing. *See* '096 Patent, col. 27, lines 46-49 ("More particularly, a logic AND gate 500 receives a pixel clock signal on line 501 from the flat panel timing generator 29 by way of line 41, the image size/position control unit 39 and line 65 of Fig. 1."). The parties do not, however, address that issue.

In any event, there is no dispute that the image size/position control unit corresponds to at least part of the recited function of "generating output column address control signals and output row address control signals for said memory system." The foregoing also provides some basis for tentatively identifying the pixel clock generator (28) as part of the structure corresponding to that function. The Court reserves any ruling on claim

definiteness upon further invalidity briefing. Finally, the Court notes that the "timing control means * * *," "image size/position control means * * * " and "frame buffer output control means * * * " elements are inter-related. Further briefing with respect to the "image size/position control means * * *," if any, should thoroughly address those relationships and their impact, if any, on the claim constructions discussed in this Order.

Thus, the Court, pending further briefing, concludes the term "image size/position control means in electrical communication with said timing control means and responsive to said column start, row start, column replicate, and row replicate control signals and said first control signals for generating output column address control signals, output row address control signals for said memory system, and a pixel clock signal" should be construed as a means-plus-function limitation under s. 112**(6). The recited function is "generating output column address control signals, output row address control signals for said memory system, and a pixel clock signal." The "corresponding structure" disclosed in the specification for performing that function is image size/position control unit (39), as illustrated in Fig. 8, and pixel clock generator (28). Under the terms of** s. 112**(6), the limitation should therefore be construed to cover this corresponding structure and any equivalent structures.**

3. "frame buffer output control means"

(1) The Parties' Positions

LG	***Hitachi***
This limitation is a "means-plus-function" clause under 35 U.S.C. s. 112(6).	This limitation is a "means-plus-function" clause under 35 U.S.C. s. 112(6).
Recited Function: reading the video image from the memory system	*Recited Function:* reading said video image from said memory system
Corresponding Structure: the circuitry described as the frame buffer output control unit 42 of Figs. 1 and 17 and any equivalents thereof, and Output FIFO 356 and any equivalents thereof.	*Corresponding Structure:* frame buffer output control unit 42 (including all the structure shown in Figure 17); and Output FIFO 356.

See Dkt. No. 64, at 36.

LG urges that "frame buffer output control unit 42 receives output column and row address control signals from image size/position control unit 39" using "the control signals to supply memory address locations at the inputs of frame buffers 20, 24, and 25," but "is not itself in direct communication with the flat panel display." Dkt. No. 47, at 58. According to LG, "[f]rame buffer output control unit 42 is connected to frame buffers 20, 24, and 25, which includes Output FIFO 356 which is directly connected to plug-in flat panel interface module 30." *Id*. at 58-59.

LG further urges that "[f]rame buffer output control unit 42[1] uses the outputs of image size/position control unit 42 to control the column and row addresses read out of memory by providing address information to frame buffers 20, 24, and 25," which receive the "address information" "as row/column read address on line 362." *Id*. at 59. "The row/column read address information on line 362 through gate 358 [which 'gate 358 controls the addresses of the memory locations from which data (e.g., a stored video image) is to be read'] to memory array 355," which "is the portion of the frame buffers that actually includes

the stored information, i.e., the video image." According to LG, "[t]he read information is then provided to output FIFO 356 and sent to plug-in flat panel interface module 30 for presentation of the video image on a flat panel display." *Id*. Thus, LG argues, "the frame buffer output control unit 42, in connection with output FIFO 356 are in electrical communication with the flat panel display, among other elements, and reads a video image from the memory system, as claimed ." *Id*.

Hitachi urges that "[t]he function recited in this means-plus-function limitation is 'reading ***said*** video image from ***said*** memory system' [and][t]he 'said video image' is the same video image referred to throughout claim 21, and the 'said memory system' is the same memory system throughout the claim." Dkt. No. 48, at 9. Hitachi further asserts that LG's construction is "vague as to whether there are two different or alternate embodiments of structure, or whether the 'black box' in Figure 1 is the same as (and includes all the circuitry of) Figure 17." *Id*. Hitachi warns that LG's construction "would render the claim invalid because any 'black box' structure (and thus no specific structure at all) would be all that was required for this means-plus-function limitation. *Id*. at 10.

In response, LG notes that "Defendants changed their construction to remove the gate 358 from the 'corresponding structure' of its proposal" and states that LG is "willing to substitute the definite article 'the' in place of the word 'a' in its claim construction." Dkt. No. 55, at 51. LG concludes that "it appears that the conflict between the parties has been greatly diminished or eliminated." *Id*.

(2) Construction

[16] The parties agree that this phrase should be construed as a means-plus-function limitation under s. 112(6). This phrase recites the word "means" followed by a functional recitation, *i.e.,* "frame buffer output control means * * * for reading * * *," and is thus presumptively a means-plus-function limitation.

Neither the term "control" nor the other modifier "frame buffer output" connote sufficient structure to remove this phrase from the ambit of s. 112(6). *See* Biomedino, LLC, 490 F.3d at 949-50. The Court thus agrees with the parties that this phrase should be construed as a means-plus-function limitation.

The parties agree that the recited function is "reading said video image from said memory system." That is what the claim recites, and the Court agrees with the parties.

With respect to the "corresponding structure," the specification explains that the frame buffers store the video image, *i.e.,* "store video data at one video rate, and simultaneously read video data out of the frame buffer at a different video rate." '096 Patent, col. 26, lines 1-3. xxx

Figure 14 is said to illustrate "the structure of frame buffers 20, 24 and 25." FN19 ' 096 Patent, col. 25, lines 66. The specification explains that "[w]ith the frame buffers operating in a fully asynchronous manner, video data may be read out of the frame buffers and through the output FIFO 356 to the flat panel display." ' 096 Patent, col. 27, lines 55-57. In the frame buffers, the "video data" is read out of the memory array (355) into FIFO (356) and from there out to the flat panel display:

FN19. According to the specification, "[e]ach of the frame buffers 20, 24, and 25 of Fig. 1 has the architecture illustrated in Fig. 14 ." ' 096 patent, col. 25, lines 66-67. *See supra* Part II.A for a reproduction of Figure 1 and Part II.B.2(f) for reproductions of Figures 14 & 17.

In operation, *digital video data* is received by the input FIFO 350 at the video rate appearing on line 352. Simultaneously, video data is read out of the FIFO and into the memory array 355 at the video rate determined by the clock signal from the frame buffer input control unit 27 on line 354.
Data is read out of or written into the memory array 355 as controlled by the logic voltage on line 360 from the input control unit 27. Further, the addresses of the memory locations into which data is written is controlled by gate 357, and the addresses of the memory locations from which data is read is controlled by gate 358. *From the memory array 355, the video data is read into the FIFO 356* at the video rate of the flat panel display as determined by the *clock signal appearing on line 363 from the frame buffer output control unit 42,* and read out of the FIFO at a different clock rate *received from the frame buffer output control unit 42 on line 364. The video image data for the flat panel display appears at the output of FIFO 356. The output FIFO allows video data to continue to be supplied to the flat panel display* when the memory array 355 is unavailable during write cycles.

'096 patent, col. 26, lines 6-25 (emphasis added). The memory array appears, in the context of claim 21, to correspond to the "memory system." In any event, "[t]he clock-in input to the FIFO 356 receives a write output clock signal on line 363 from [frame buffer output] control unit 42 on line 65, and a clock out signal from the [frame buffer output] control unit 42 on a line 364. The data output of the FIFO 356 is connected to a bus 365 leading to the flat panel interface module 30." '096 Patent, col. 25, lines 61-65. Essentially, then, the frame buffer output control unit 42 controls the FIFO 356 to read out the video image from the memory array.
As noted above, "[t]he image size/position control unit 39 also creates a set of timing clocks and control signals that are provided to a frame buffer output control unit 42, which in turn addresses memory locations in the frame buffers." '096 Patent, col. 8, lines 46-49. Specifically, "[a] timing signal that controls the reading of data from the frame buffer memory is output by control unit 39 to control unit 42 on line 65." '096 Patent, col. 8, lines 60-62. According to the specification, "[t]he order in which data is read out of the frame buffers determines the form in which the image will be presented on the plat [sic] panel display screen. * * * * By way of example, if the control unit 42 reads the frame buffer video data beginning at the last line and then proceeding to the first, the video image will be displayed upside down on the display screen." '096 Patent, col. 8, line 57-col. 9, line 1.

Figure 17 is a "logic schematic diagram of the frame buffer output control unit 42 of FIG. 1." '096 Patent, col. 4, lines 12-13.FN20 The specification explains that "a logic AND gate 500 receives a pixel clock signal on line 501 from the flat panel timing generator 29 by way of line 41, the image size/position control unit 39 and line 65 of FIG. 1. Further, a write to frame buffer signal is received on line 504 from line 414 of Fig. 15. The valid address signal 502 is received by the microprocessor 36 on line 43. This signal is set by the microprocessor to allow video data to be read from the frame buffers 20, 25 and 24 of Fig. 1." ' 096 Patent, col. 27, lines 46-54.

FN20. *See supra* Part II.A.2 for a reproduction of Figure 1 and Part II.B.2(f) for a reproduction of Figure 17.

Claim 21 also calls for the "frame buffer output control means" to be "in electrical communication with [A] said timing control means, [B] said memory system, [C] said image size/position control means, and [D] said flat panel display, and [E] responsive to said pixel clock signal." '096 Patent, col. 32, lines 14-19 (lettering added). The frame buffer output control unit 42 and FIFO 356 appear to meet those limitations, although that is, once again, unclear with respect to [E].

With respect to "in electrical communication with [A] said timing control means, * * * and [C] said image size/position control means," the "logic AND gate 500" of the frame buffer output control unit, as noted above, "receives a pixel clock signal on line 501 from the flat panel timing generator 29 by way of line 41, the image size/position control unit 39 and line 65 of FIG. 1." ' 096 Patent, col. 27, lines 47-49. Also, "[t]he valid address signal 502 is received by the microprocessor 36 on line 43 [into the frame buffer output control unit]." '096 Patent, col. 27, lines 51-52. Thus, the frame buffer output control unit (42) meets those limitations.

With respect to "in electrical communication with * * * [D] said flat panel display," from the foregoing, it is clear that the frame buffer output control unit (42) through the FIFO 356 meets those limitations.

Finally, with respect to "in electrical communication with * * * [B] said memory system," as discussed above, the FIFO (356) meets that limitation, and the frame buffer output control unit (42) indirectly.

Thus, it seems reasonably clear that the frame buffer output control unit (42) and FIFO (356) together perform the function of "reading said video image from said memory system." Accordingly, the Court agrees with the parties.

The Court concludes the limitation "frame buffer output control means in electrical communication with said timing control means, said memory system, said image size/position control means, and said flat panel display, and responsive to said pixel clock signal for reading said video image from said memory system" should be construed as a means-plus-function limitation under s. 112**(6). The recited function is "reading said video image from said memory system." The "corresponding structure" disclosed in the specification for performing this function is frame buffer output control unit (42), as illustrated in Fig. 17, and FIFO (356), as illustrated in Figure 14. Under the terms of** s. 112**(6), this limitation should therefore be construed to cover the stated corresponding structure and any equivalent structures.**

III. Conclusion

According to the previous discussion, the Court **ORDERS** the claim terms for the '096 Patent construed as indicated herein.