United States District Court,
N.D. California, San Jose Division.

RAMBUS INC,
Plaintiff.
v.
HYNIX SEMICONDUCTOR INC., Hynix Semiconductor America Inc., Hynix Semiconductor Manufacturing America Inc., Samsung Electronics Co., Ltd., Samsung Electronics America, Inc., Samsung Semiconductor, Inc., Samsung Austin Semiconductor, L.P., Nanya Technology Corporation, Nanya Technology Corporation U.S.A,
Defendants.
Rambus Inc,
Plaintiff.
v.
Samsung Electronics Co., Ltd., Samsung Electronics America, Inc., Samsung Semiconductor, Inc., Samsung Austin Semiconductor, L.P,
Defendants.
Rambus Inc,
Plaintiff.
v.
Micron Technology, Inc., and Micron Semiconductor Products, Inc,
Defendants.

Nos. C-05-00334 RMW, C-05-02298 RMW, C-06-00244 RMW

Aug. 27, 2008.

Andrea Jill Weiss Jeffries, David C. Yang, Donald Ward, Gregory P. Stone, Jeffrey Y. Wu, Jennifer Lynn Polse, Keith Rhoderic Dhu Hamilton, II, Steven Mccall Perry, Munger Tolles & Olson LLP, Andrew Winston Song, Rollin Andrew Ransom, Sidley Austin LLP, Los Angeles, CA, Burton Alexander Gross, Esq., Carolyn Hoecker Luedtke, Erin C. Dougherty, Miriam Kim, Peter A. Detre, Rosemarie Theresa Ring, Esq., Sean Eskovitz, Munger Tolles & Olson LLP, Matthew Thomas Powers, Sidley Austin LLP, San Francisco, CA, Craig N. Tolliver, Douglas C. Edwards, Kevin L. Burgess, Pierre J. Hubert, Ramzi R. Khazen, Seth R. Hasenour, McKool Smith, Kevin S. Kudlac, Weil,Gotshal & Manges LLP, Austin, TX, for Plaintiff.

Matthew Douglas Powers, Weil Gotshal & Manges, Redwood Shores, CA, Brian C. Riopelle, McGuire Woods, LLP, Riochmond, VA, Carmen E. Bremer, Weil Gotshal & Manges LLP, Dallas, TX, Claire Elise Goldstein, Dana K. Powers, John D. Beynon, Steven S. Cherensky, Weil, Gotshal & Manges, LLP, Redwood Shores, CA, David C. Radulescu, Matthew J. Antonelli, Robert S. Berezin, Weil Gotshal & Manges LLP, New York, NY, Edward Robert Reines, Jared Bobrow, Weil Gotshal & Manges LLP, Redwood Shores, CA, Jason Sheffield Angell, Kristin Sarah Cornuelle, Stacy Beth Margolies, Theresa E. Norton, Vickie L. Feeman, Orrick, Herrington & Sutcliffe, LLP, Menlo Park, CA, Julie Jinsook Han, Townsend and Townsend and Crew LLP, Palo Alto, CA, Rene A. Trevino, Weil Gotshal & Manges LLP, Austin, TX, for Defendants.

SUPPLEMENTAL CLAIM CONSTRUCTION ORDER FOR THE WARE PATENTS AND ORDER DENYING THE MANUFACTURERS' MOTION FOR SUMMARY JUDGMENT

RONALD M. WHYTE**, District Judge.**

Rambus has accused the Manufacturers of infringing various patents. On July 25, 2008, the court issued its claim construction order interpreting most of the disputed terms in U.S. Patent Nos. 6,496,897 and 6,493,789, referred to as the "Ware patents." *See* Rambus Inc. v. Hynix Semiconductor Inc., 2008 WL 2955125 (N.D.Cal. Jul.25, 2008) ("Ware Order"). FN1 The court requested further briefing from the parties regarding the phrase "during a first/second half of a clock cycle of an external clock signal." *Id*. at *11-*12.

FN1. The court previously construed the claims of the other fifteen patents-in-suit in a separate order. *See* Rambus Inc. v. Hynix Semiconductor Inc., 2008 WL 2754805 (N.D.Cal.2008). That order contains additional background on DRAM technology and the present dispute between Rambus and the Manufacturers.

The parties have since filed the requested briefs. The court has reviewed these additional papers, as well as the original briefing and the court has considered the arguments of counsel. The court now sets forth its claim construction and ruling on the summary judgment motion dealing with this phrase in the Ware patents' claims.

I. THE CLAIM CONSTRUCTION DISPUTE

Rambus has asserted that the Manufacturers infringe claim 13 of the '789 patent and claims 2 and 16 of the '897 patent. The claims all recite limitations that require the memory device (or method of operating a memory device) to receive certain information "during the first half of the clock cycle of the external clock signal" or "during the second half of the clock cycle of the external clock signal." *See* Ware Order, 2008 WL 2955125 at *5 (reciting the full text of the claims).

The parties disagree about what it means for information to be received "during a first/second half of the clock cycle of the external clock signal." Generally, Rambus argues that the claims impose no restriction on where a clock cycle begins. The Manufacturers argue that a person of ordinary skill in the art would have understood a "first half of the clock cycle" and "second half of the clock cycle" to begin at a specific point. Their proposed constructions appear below:

Claim term:	**Rambus's construction:**	**The Manufacturers' Construction:**
"during a first/second half of a clock cycle of an external clock signal"	Phrase does not require separate construction, but is construed in view of the terms therein (see "clock cycle," "external clock signal"), plus plain meaning.	Only between two adjacent clock edges beginning with a rising edge of the clock signal and ending at the next falling edge of the clock signal or beginning with a falling edge of the clock signal and ending at the next rising edge.

As discussed in the court's prior order, the Ware specification says very little about clocking. *See id*. at *11-

*12. The only statement in the Ware specification regarding clocking is that "[f]or the embodiments of the invention, a single clock cycle has two phases, allowing two transfer operations within a single clock cycle" and that "[f]or alternative embodiments, other clocking schemes may be used." '789 Patent at col. 7, ll. 21-24. Because the specifications sheds so little light on how a person of ordinary skill would understand the claims, the court turns to the extrinsic evidence supplied by the parties. Helmsderfer v. Bobrick Washroom Equipment, Inc., 527 F.3d 1379, 1381-83 (Fed.Cir.2008).

The excerpt from a Nanya technical specification shown in Figure 1 at right provides some context for discussing how a clock signal functions. The figure actually shows two clock signals, one solid and one dashed and labeled CK and /CK respectively. The figure shows the clock signals being combined to form a differential clock signal. Each clock signal has a rising edge and a falling edge during which the signal's voltage increases or decreases. This is significant because a device can detect these changes in voltage. *See* Decl. of Joseph McAlexander, Docket No. 2010, C-05-00334 para.para. 9, 11 (N.D.Cal. Aug. 1, 2008). But between these changes in voltage, the ideal clock signal maintains a constant voltage and is not measured. *See id*. para. 10.

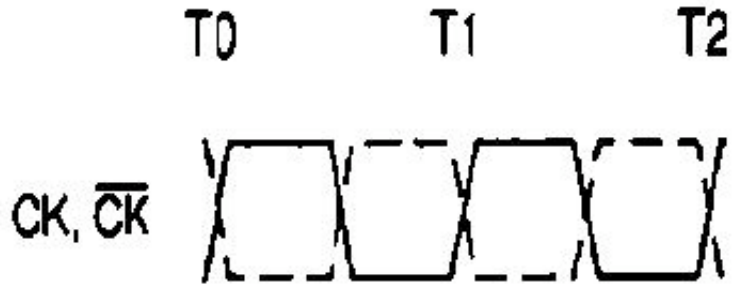


Figure 1: Excerpt from a Nanya timing diagram.

The figure also demonstrates that a clock signal is periodic, that is, the signal repeats itself. Where a period "starts" can be arbitrarily defined. For example, the court previously expressed concern that if it construed a "clock cycle" as beginning with, for example, the rising edge of a clock signal, the next question would be whether the rising edge begins when the signal's voltage begins to increase, when it passes a midpoint, or when it passes some other point. *See* Ware Order, 2008 WL 2955125 at *12. This dilemma is also illustrated by Figure 1. The labels "T0," "T1," and "T2" correspond to the beginning of three clock cycles. In the illustrated device, a clock signal (CK) and its inverse (/CK) are combined to form a differential clock signal, and a cycle is then defined as beginning when the two signals intersect. Nevertheless, a cycle could have been defined using only a single clock signal, and that cycle could have begun at any point in time.

The Manufacturers' supplemental briefing clarifies their position that a person of ordinary skill would have understood that a clock cycle may begin at various arbitrary points along the clock signal's edge. Mr. McAlexander states that:

For example, if the clock signal swings between 0 volts and 3 volts (i.e., the low state of the clock is 0 volts and the high state of the clock is 3 volts), the circuits can be designed to detect a value between the two voltages, such as 1 V, 1.5V or another voltage point along the transition. The designer may select such a value, as a reference level for the system, which will then be used to provide a single point of reference to

reliably trigger events to synchronize with the clock. The selection of one of a number of reference voltage values along the transition is simply a matter of design choice. Such well-known edge triggering techniques are used not only internal to integrated circuits but also when using test measurement equipment such as oscilloscopes.

McAlexander Decl. para. 11. What is significant, from the Manufacturers' point of view, is that a person of ordinary skill in the art would understand that as a practical matter a clock cycle must begin at some point along the edge of a clock signal, as opposed to a point at which the clock signal's voltage is not changing, because it is only along the clock's signal's edge that a clock can be measured.

This concept finds confirmation in contemporaneous dictionaries. For example, the *1996 IEEE Dictionary* defines "clock cycle" as "one period of the [clock] signal, beginning with the rising edge of the signal and ending on the following rising edge of the signal." Rambus submits a more general definition from the *Oxford Dictionary of Computing* (4th ed.1997) that states that "A clock cycle is considered to be one complete cycle of the clock signal and will always contain one active transition of the clock." Though the definition does not state that a clock cycle "begins" with the clock signal's transition, the definition's emphasis on the signal's transition demonstrates the importance of the transition to the function of the signal and to the understanding of a person of skill in the art.

Contemporaneous patents further establish that a person of ordinary skill would understand that a clock cycle begins where it can be measured, i.e., on its edges. For example, a patent issued to Atsushi Takasugi discusses at length how various signals within a DRAM respond to low-to-high and high-to-low transitions of the clock signals. U.S. Patent No. 5,420,688, col. 4, ll. 16-55. FN2 Another synchronous DRAM patent from 1996 discusses prior art implementations of CAS latency. It continuously demonstrates an understanding that a clock cycle begins on the edge of the clock signal, as shown by the three exemplary figures below. U.S. Patent No. 5,550,784; *see, e.g.*, id. at col. 1, ll. 12-59 (discussing Figures 1A-1C). No figure in the ' 784 patent shows a clock cycle starting at any point other than at the edge of the clock signal.

FN2. Rambus argues that the Takasugi patent undermines the Manufacturers' argument, focusing on a signal labeled S90. The patent states that its output control circuit is designed to "drive the output control signal S90 to the active state for one clock cycle, starting a certain number of clocks after /RAS becomes active." U.S. Patent No. 5,420,688, col. 6, ll. 1-4. Rambus points out that in Figure 8 "S90 clearly does not coincide with rising or falling edges of the clock." Rambus appears to be incorrect. Figure 8 shows S90 increasing shortly after a rising edge and falling slightly after the next rising edge (t13 and t14 respectively). As the specification describes, "S90 may be active during an interval from substantially the third rising edge of CLK after /RAS becomes active until substantially the fourth rising edge." Id., col. 6, ll. 4-7. While S90, which is not a clock signal, lags the actual clock signal by a small amount of time, it clearly is driven by transitions in the clock signal. This discussion reinforces that a person of ordinary skill in the art would measure a cycle from a point along the edge of the clock.

FIG. 1A
PRIOR ART CLOCK

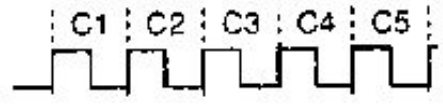


FIG. 3A
PRIOR ART

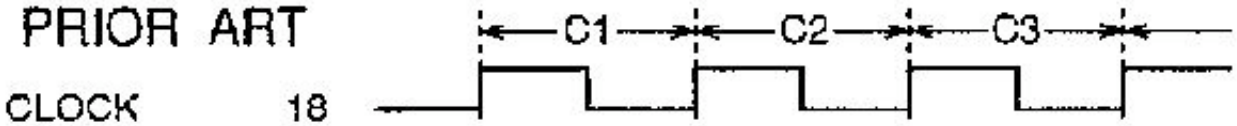


FIG. 5B

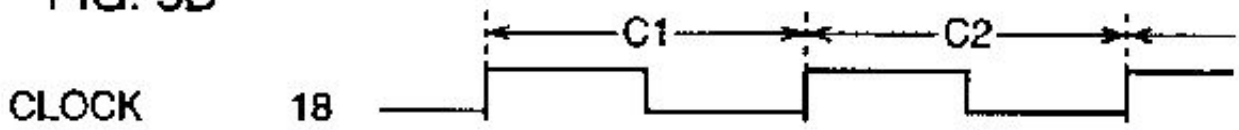
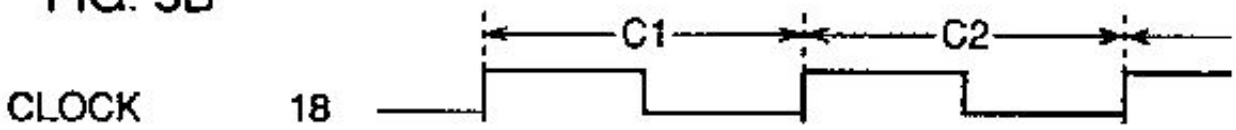


FIG. 5B



In its original briefing, Rambus argued that a clock cycle "need not lie between rising and falling edges of a clock signal" and that "a rough analogy can be found in the periodic nature of the hours in the day-while the time between 12:00 AM and 12:00 PM can be said to be one half of a day, so too is any other twelve-hour period, such as the time between 23:00 AM and 3:00 PM." The court rejects Rambus's "rough analogy." Time can be measured at any point, but the uncontradicted testimony of Mr. McAlexander is that a clock signal is ordinarily measured on its edges, not at any arbitrary point along the signal. Moreover, even if extrinsic evidence like other patents or dictionaries merits less weight than intrinsic evidence in construing claim language, *see* Phillips v. AWH Corp., 415 F.3d 1303, 1324 (Fed.Cir.2005) (en banc), the extrinsic evidence introduced by the Manufacturers is more helpful in discerning the meaning of language to a person or ordinary skill in the art than Rambus's "rough analogy."

The foregoing discussion does not mean that the Manufacturers' proposed construction is completely free of difficulty. Rambus points out that all of the discussion to this point has focused on clock signals with a 50/50 duty cycle, i.e., clock signals that spend equal amounts of time high and low. By contrast, other duty cycles are possible, creating clock signals with asymmetric lengths of time between a rising edge and a falling edge and between a falling edge and a rising edge. For example, Figure 2 below compares a clock signal with a 50/50 duty cycle and a 90/10 duty cycle.

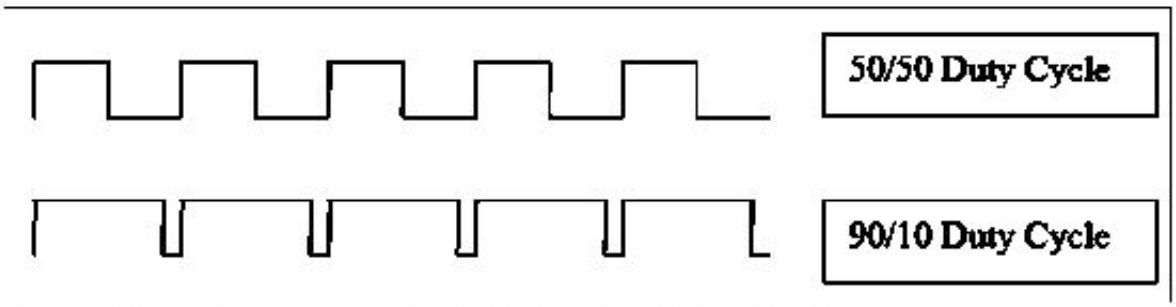


Figure 2: Duty cycle comparison from the Declaration of Robert Murphy.

The Manufacturers' proposed construction is that "during a first/second half of a clock cycle" means "only between two adjacent clock edges beginning with a rising edge of the clock signal and ending at the next falling edge of the clock signal or beginning with a falling edge of the clock signal and ending at the next rising edge." As Rambus's 90/10 duty cycle hypothetical shows, this construction would lead to the first portion of a clock cycle being of a different length than the second portion. Obviously, this result cannot be reconciled with the claim language explicitly reciting that information arrive "during the first half of the clock signal" and "during the second half of the clock signal."

The Manufacturers' construction also transmutes the phrase "during a half of a clock cycle" to mean "*only* during a half of a clock cycle." In other words, the parties disagree about whether an event that occurs "during" a period of time must occur exclusively within that time period and not outside of it. As discussed below, this appears to be the true dispute between the parties.

Neither side's briefing addressed the meaning of the word "during." The parties do not suggest that the word "during" has a technical meaning in this context. Hence, the court turns to its ordinary meaning. The *Merriam-Webster's Dictionary* offers two definitions for "during:" "1: throughout the duration of <swims every day *during* the summer>" and "2: at a point in the course of < was offered a job *during* a visit to the capital>." Neither definition supports the Manufacturers' contention that an event that occurs "during" a time period cannot also occur outside the time period. The word "during" implies only that an event occurs within a time period; it imposes no limitation on what occurs outside that time period.

The difficulties discussed above are most easily resolved by limiting the court's construction to the technical term in dispute, namely "clock cycle." A "clock cycle" is a period of the clock signal, beginning at an edge of the clock signal where the clock signal can be measured. With this definition of "clock cycle," the phrase "during the first/second half of the clock cycle of the external clock signal" is readily understood using its ordinary meaning without additional construction.

II. THE MANUFACTURERS' NON-INFRINGEMENT ARGUMENT

The Manufacturers move for summary judgment of non-infringement of the three claims in the Ware patents, arguing that their devices do not "receive a first/second mask bit during the first/second half of the clock cycle of the external clock signal." The evidence suggests that the data mask signals at issue in the accused devices go high or low slightly before the beginning of a transition of the external clock signal, but the signals remain high or low for a substantial portion of the half-cycle of the external clock signal. For example, the Manufacturers submitted the timing diagram from a representative Nanya device shown below in Figure 3:

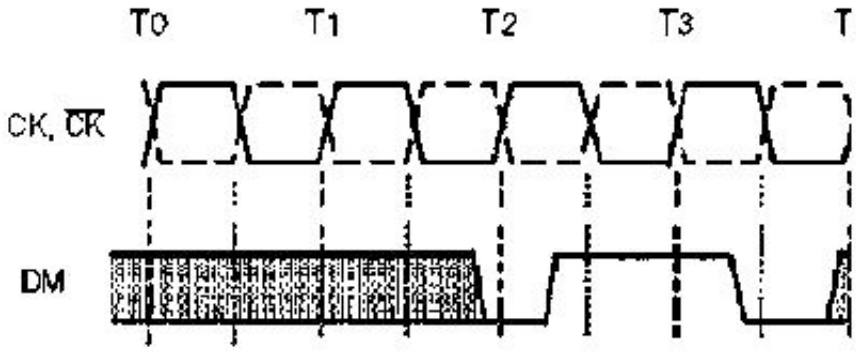


Figure 3: Excerpts from a Nanya timing diagram.

The Manufacturers' argument turns on the court accepting their proposed claim construction. While the court largely adopted the Manufacturers' construction, it did not adopt that the straightjacketing "only" limitation from the Manufacturers' proposed construction. According to the Manufacturers, the mask bits conveyed by the DM signal shown above are not received "during" a half of a clock cycle because the DM signal goes high or low slightly before the transition of the external clock signal. Under the Manufacturer's construction, the mask bit signal could "only" arrive between a rising edge and a falling edge of the external clock signal. The court has rejected this construction, and therefore denies the motion for summary judgment.

Furthermore, Rambus's claims require the DRAM to receive a mask bit "during the first half of the clock cycle." As shown in the timing diagram above, it appears that the Manufacturers' devices do receive the mask bit information during a "first half of a clock cycle." That the DM signal arrives slightly before the beginning of the external clock signal's "first half" is not relevant because the data mask signal remains available for the DRAM to receive "during the first half." The court therefore also denies the motion because Rambus has shown that the accused products appear to meet the limitation concerning the receipt of a first/second mask bit.

III. MEMORANDUM REGARDING THE SCOPE OF PRIOR ART EVIDENCE

In its statement regarding the proposed case management schedule, Rambus noted that "The Manufacturers have served invalidity contentions and supplemental invalidity contentions citing well-over 200 alleged prior art references and attaching multiple boxes worth of purported claim charts." In the court's case management order, the court provided only 21 days for Rambus to file rebuttal expert reports. *See, e.g.*, Docket No. 968, C-05-02298, at 2 (N.D.Cal. Jul. 9, 2008). In providing Rambus with less time to file its rebuttal reports than it requested, the court noted that it "expects that the Manufacturers will have significantly narrowed the number of prior art references supporting their invalidity contentions." *Id.* at 2 fn. 1. In its supplemental briefing, Rambus mentioned that the Manufacturers have now disclosed "nearly three-hundred (300) separate purported references" and had added 10 references to their contentions as late as July 28.

The court cautions that the parties must focus the issues both in fairness to each other and to the jury which

will face the daunting task of understanding complex technology and applying its factual findings to the applicable patent law. The court in its June 25, 2007 ordered Rambus to narrow its asserted claims from the 22 patents in suit to no more than 25 claims. The court did not mean to imply by that reduction that 25 claims from 22 different patents would be an appropriate number of claims for trial. The court expects Rambus to further reduce its asserted claims after it reviews the Manufacturers' asserted prior art.

The court did not anticipate that the Manufacturers would assert "nearly three-hundred (300) separate purported references," if they have, in fact, done so in response to Rambus's assertion of infringement of 25 claims. It is hard for the court to imagine a legitimate basis for asserting more than two allegedly anticipating references and two or three obviousness combinations per claim. In the event that Rambus does not voluntarily reduce the number of asserted claims and the Manufacturers do not greatly reduce their prior art references, the court will require the parties to do so as it deems appropriate.

IV. ORDER

For the reasons set forth above, the court construes the disputed phrase as described. The Manufacturers' motion for summary judgment of non-infringement with respect to the "during a first/second half of a clock cycle" limitation is denied.

N.D.Cal.,2008.
Rambus Inc. v. Hynix Semiconductor Inc.