United States District Court,
E.D. Texas, Tyler Division.

SAMSUNG ELECTRONICS CO., LTD,
Plaintiff.
v.
MATSUSHITA ELECTRIC INDUSTRIAL CO., LTD,
Defendant.

No. 6:06CV 154

Nov. 14, 2007.

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MEMORANDUM OPINION

LEONARD DAVIS**, District Judge.**

This Claim Construction Opinion construes terms in Samsung's asserted patents: U.S. Patent Nos. 5,091,339 ("the '339 patent") and 5,173,442 ("the '442 patent") (collectively, "the Carey patents") and RE 36,490 ("the '490 patent"). This Opinion also construes terms in Matshusita Electronic Industrial's ("MEI") asserted patents: U.S. Reissue Patent Nos. 35,921 ("the '921 patent") and 35,680 ("the '680 patent") and U.S. Patent Nos. 5,189,588 ("the '588 patent") and 6,677,195 ("the '195 patent").

BACKGROUND

The Samsung patents relate generally to semiconductors. the '442 patent is a continuation of a continuation-in-part of the '339 patent. The Carey patents describe a process for forming electrical wiring in multilayer interconnect structures such as modern integrated circuits. In this process-known generally as a "dual damascene"-channels and vias are formed and then filled with metal to form the wiring. Samsung's '490 patent describes a power and signal line bussing method for memory devices located on semiconductor

chips. The described power, ground, and signal wiring arrangement is designed to protect the electrical circuitry from interference and decrease overall chip size.

The MEI's '921 and '680 patents relate generally to synchronous random access memory ("SDRAM"). Both patents describe using a clock signal to increase overall operational speed. The '921 patent claims a SDRAM, and the '680 patent claims a system incorporating the SDRAM claimed in the '921 patent.

MEI's '588 and '195 patents relate generally to semiconductor chip design. The '588 patent relates to an electro-static discharge protection device and claims a surge protection apparatus utilizing multiple transistors to discharge or drain excess static. MEI's '195 patent claims a semiconductor integrated circuit device and method of producing such a circuit. The '195 patent discloses a semiconductor fuse structure that allows defective areas of a chip to be disabled by disconnecting selected fuses, thereby increasing chip manufacture production yields.

APPLICABLE LAW

"It is a 'bedrock principle' of patent law that 'the claims of a patent define the invention to which the patentee is entitled the right to exclude.' " Phillips v. AWH Corp., 415 F.3d 1303, 1312 (Fed.Cir.2005) (en banc) (quoting Innova/Pure Water Inc. v. Safari Water Filtration Sys., Inc., 381 F.3d 1111, 1115 (Fed.Cir.2004)). In claim construction, courts examine the patent's intrinsic evidence to define the patented invention's scope. *See id.;* C.R. Bard, Inc. v. U.S. Surgical Corp., 388 F.3d 858, 861 (Fed.Cir.2004); Bell Atl. Network Servs., Inc. v. Covad Commc'ns Group, Inc., 262 F.3d 1258, 1267 (Fed.Cir.2001). This intrinsic evidence includes the claims themselves, the specification, and the prosecution history. *See* Phillips, 415 F.3d at 1314; C.R. Bard, Inc., 388 F.3d at 861. Courts give claim terms their ordinary and accustomed meaning as understood by one of ordinary skill in the art at the time of the invention in the context of the entire patent. Phillips, 415 F.3d at 1312-13; Alloc, Inc. v. Int'l Trade Comm'n, 342 F.3d 1361, 1368 (Fed.Cir.2003).

The claims themselves provide substantial guidance in determining the meaning of particular claim terms. Phillips, 415 F.3d at 1314. First, a term's context in the asserted claim can be very instructive. *Id*. Other asserted or unasserted claims can also aid in determining the claim's meaning because claim terms are typically used consistently throughout the patent. *Id*. Differences among the claim terms can also assist in understanding a term's meaning. *Id*. For example, when a dependent claim adds a limitation to an independent claim, it is presumed that the independent claim does not include the limitation. *Id*. at 1314-15.

"[C]laims 'must be read in view of the specification, of which they are a part.' " *Id*. (quoting Markman v. Westview Instruments, Inc., 52 F.3d 967, 979 (Fed.Cir.1995) (en banc)). "[T]he specification 'is always highly relevant to the claim construction analysis. Usually, it is dispositive; it is the single best guide to the meaning of a disputed term.' " *Id*. (quoting Vitronics Corp. v. Conceptronic, Inc., 90 F.3d 1576, 1582 (Fed.Cir.1996)); Teleflex, Inc. v. Ficosa N. Am. Corp., 299 F.3d 1313, 1325 (Fed.Cir.2002). This is true because a patentee may define his own terms, give a claim term a different meaning than the term would otherwise possess, or disclaim or disavow the claim scope. Phillips, 415 F.3d at 1316. In these situations, the patentee's lexicography governs. *Id*. Also, the specification may resolve ambiguous claim terms "where the ordinary and accustomed meaning of the words used in the claims lack sufficient clarity to permit the scope of the claim to be ascertained from the words alone." Teleflex, Inc., 299 F.3d at 1325. But, " '[a]lthough the specification may aid the court in interpreting the meaning of disputed claim language, particular embodiments and examples appearing in the specification will not generally be read into the

claims.' " Comark Commc'ns, Inc. v. Harris Corp., 156 F.3d 1182, 1187 (Fed.Cir.1998) (quoting Constant v. Advanced Micro-Devices, Inc., 848 F.2d 1560, 1571 (Fed.Cir.1988)); *see also* Phillips, 415 F.3d at 1323. The prosecution history is another tool to supply the proper context for claim construction because a patent applicant may also define a term in prosecuting the patent. Home Diagnostics, Inc., v. Lifescan, Inc., 381 F.3d 1352, 1356 (Fed.Cir.2004) ("As in the case of the specification, a patent applicant may define a term in prosecuting a patent.").

Although extrinsic evidence can be useful, it is " 'less significant than the intrinsic record in determining the legally operative meaning of claim language.' " Phillips, 415 F.3d at 1317 (quoting C.R. Bard, Inc., 388 F.3d at 862). Technical dictionaries and treatises may help a court understand the underlying technology and the manner in which one skilled in the art might use claim terms, but technical dictionaries and treatises may provide definitions that are too broad or may not be indicative of how the term is used in the patent. *Id.* at 1318. Similarly, expert testimony may aid a court in understanding the underlying technology and determining the particular meaning of a term in the pertinent field, but an expert's conclusory, unsupported assertions as to a term's definition is entirely unhelpful to a court. *Id.* Generally, extrinsic evidence is "less reliable than the patent and its prosecution history in determining how to read claim terms." *Id.*

The patents in suit also contain means-plus-function limitations that require construction. Where a claim limitation is expressed in "means plus function" language and does not recite definite structure in support of its function, the limitation is subject to 35 U.S.C. s. 112, para. 6. Braun Med., Inc. v. Abbott Labs., 124 F.3d 1419, 1424 (Fed.Cir.1997). In relevant part, 35 U.S.C. s. 112, para. 6 mandates that "such a claim limitation 'be construed to cover the corresponding structure ... described in the specification and equivalents thereof.' " *Id.* (citing 35 U.S.C. s. 112, para. 6). Accordingly, when faced with means-plus-function limitations, courts "must turn to the written description of the patent to find the structure that corresponds to the means recited in the [limitations]." *Id.*

Construing a means-plus-function limitation involves multiple inquiries. "The first step in construing [a means-plus-function] limitation is a determination of the function of the means-plus-function limitation." Medtronic, Inc. v. Advanced Cardiovascular Sys., Inc., 248 F.3d 1303, 1311 (Fed.Cir.2001). Once a court has determined the limitation's function, "the next step is to determine the corresponding structure disclosed in the specification and equivalents thereof." *Id.* A "structure disclosed in the specification is 'corresponding' structure only if the specification or prosecution history clearly links or associates that structure to the function recited in the claim." *Id.* Moreover, the focus of the "corresponding structure" inquiry is not merely whether a structure is capable of performing the recited function, but rather whether the corresponding structure is "clearly linked or associated with the [recited] function." *Id.*

THE '339 and '442 PATENTS FN1

FN1. Appendix A contains the patent claims containing the disputed terms.

Insulating layer

The Court agrees with Samsung and construes the term "insulating layer" in claim 11 of the '339 patent and claim 3 of the '442 patent as "a layer made of one or more materials that are poor conductors of electricity." MEI argues that the construction should be "a layer of one material that is a poor conductor of electricity." MEI's construction is overly narrow-the patent clearly encompasses an insulating layer composed of more than one material or sublayer. *See* '339 Patent Figs. 7d-7f (disclosing an insulating layer composed of two

sublayers); col. 3:39-41 (disclosing an insulating layer made of two materials).

Base

The Court agrees with Samsung and construes the term "base" in claim 11 of the '339 patent as "a structure on which a multilayer electrical interconnect is fabricated." MEI's proposed construction-"a bottom layer of electrically conductive material"-adds limitations requiring that the base be "electrically conductive" and a "bottom" layer. The specification discloses that the base may be "an organic or inorganic *insulator,* a conductor, an integrated circuit, or a preceding layer ...." '339 Pat. col. 3:24-28 (emphasis added). MEI's narrow construction is controverted by the specification.

Via

The Court agrees with Samsung and construes the term "via" in claim 11 of the '339 patent and claim 3 of the '442 patent as "a hole that vertically extends through an insulating layer." MEI's proposed construction-"a hole that vertically extends through an insulating layer to an underlying electrical conductor"-adds the limitation that via must be connected to a conductor. Neither the claims-at-issue nor the specification support this additional limitation. Via is given its ordinary meaning-it is simply a vertical hole in an insulating layer. The claims-at-issue describe how a via is formed in an insulating layer. *See* '339 Pat. col. 12:33-64; '442 Pat. col. 11:50-65. Vias are not described in terms of what materials-electrically conductive or otherwise-are deposited in them.

Etch

The Court agrees with Samsung and construes the term "etch" in claim 11 of the '339 patent and claim 3 of the '442 patent as "a process or processes for removing one or more materials using chemical and/or physical means." MEI's proposed construction-"a chemical or plasma used to remove material from the claimed insulating layer and the claimed first soft mask or second soft mask in one step"-adds the limitations that an etch must be done in one step, includes only a chemical or plasma mechanism, and is used to remove material from an insulating layer. MEI's proposed construction is overly narrow. The specification discloses that an "etch" step may be done with various chemical and physical processes, may combine more than one process as part of a single etch "step," and may be used to remove soft masks and insulating materials. *See* '339 Pat. col. 4:36-50 (disclosing chemical and physical etch methods); col. 4:30-32; col. 8:9-21 (disclosing multiple etch processes used as part of a single etch step).

Soft mask

The Court construes the term "soft mask" in claim 11 of the '339 patent and claim 3 of the '442 patent as "a mask is an erodable layer of material used to cover selected areas of a surface during etch. A soft mask erodes more rapidly than a hard mask, which erodes slowly or not at all." The patents-at-issue use "soft mask" as a relative term to "hard" mask, which is described as a mask which "erodes slowly or not at all." *See* '339 Patent col. 3:54-55. These terms lack lack an ordinary and accustomed meaning in the relevant art, and no other definition of "soft mask" or "hard mask" is provided in the patent.

Samsung's proposed construction-"an erodible layer of material used to cover selected areas of a surface during etch"-improperly reads "soft" out of the term. MEI's construction-"a rapidly erodible layer of material used to cover selected areas of surface during the claimed step of applying a first etch or applying a second etch"-reflects the relative erosion of hard and soft masks, but adds a limitation of "rapid" erosion

that is not supported by the claims or specification and would itself likely require construction. Furthermore, MEI's proposed limitation that a mask be used in an etch is an improper and redundant inclusion of other limitations from the claims.

An opening to expose the channel and via

The Court construes the phrase "an opening to expose the channel and via" in claim 11 of the '339 patent and claim 3 of the '442 patent as "an opening in the second soft mask where the channel and via are to be formed." Samsung argues that no construction is necessary because "via" and "channel" are described elsewhere in the patent and the remainder of the phrase is clear. However, the claims describe how the second soft mask covers the insulating layer and exposes the areas where the channel and via *will be* after the second etch is applied. This construction clarifies that the phrase refers to the area that is eroded by the second etch to form the channel and via.

MEI's construction-"an open portion of the second soft mask that is aligned with the region to form the channel and via such that substantially no portion of the second soft mask is in that region"-requires a high degree of precision that is not specified in the patent. Furthermore, this construction would likely require further construction to define what "substantially no portion" means.

THE '490 PATENT

Memory cell array

The Court adopts the construction of "memory cell array" that the parties agreed to at the claim construction hearing: "a coordinated group or matrix of memory cells." Although MEI argued that the construction of the terms should specify that "bit lines" are included, MEI essentially conceded at the hearing that memory cells are understood to have bit lines and that a jury would understand this fact from testimony. *See* Claim Const. Hr'g Tr. at 62. It is therefore unnecessary to include "bit lines" in the construction.

Single memory cell array

Since the parties agreed to the meaning of "memory cell array," "single memory cell array" in claims 1 and 3 of the '490 patent does not require further construction. Samsung's proposed construction merely substitutes "individual" for "single." MEI's arguments for this term are addressed above in the construction of "memory cell array."

Power lines

The Court agrees with Samsung and construes "power lines" in claims 1 and 3 of the '490 patent as "conducting paths that provide electric power." The parties agree that both power lines are conducting paths. *See* Claim Const. Hr'g Tr. at 62. MEI's proposed construction-"conducting paths, each independently providing electric power"-requires that each and every power line be independently coupled to each circuit. MEI's construction improperly imports limits from the preferred embodiment; while noise reduction is optimized by independent power lines, the patent does not require such independence for each power line.

Ground lines

The Court agrees with Samsung and construes "ground lines" in claims 1 and 3 of the '490 patent as

"conducting paths that provide a connection to the ground." The parties agree that both ground lines are conducting paths. *See* Claim Const. Hr'g Tr. at 62. As discussed above for "power lines," MEI's construction of "ground lines"-"conducting paths, each independently providing a connection to ground"-improperly imports limitations from the preferred embodiment.

THE '921 and '680 PATENTS

External clock signal

The Court construes "external clock signal" as "a single timing signal from outside of a device." MEI argues that the term should be construed as "a clock signal from outside of a device." Samsung argues that the construction should be "a single external timing signal provided to a single input pin." MEI acknowledged in its brief that a clock signal provides timing information. MEI Claim Const. Br. at 7 (Docket No. 112). Samsung's argument that the external clock signal is limited to a single input pin is presumably based only on an amendment to claim 1. *See* Response to Examiner at 113-14 (Exh. 5, Docket No. 120). This statement is not sufficient to establish a waiver of claim scope.

Samsung also argues that the term is limited to a single clock signal. The Court agrees. The specification of the patents-at-issue consistently emphasize and disclose the use of a single clock signal on the random port. *See* '921 Patent col. 2:17-19 (distinguishing the invention on the basis that it uses a single clock signal); col. 2:25-29 ("Under the teachings of the present invention, a *single* clock pulse drives an internal state machine to provide the control pulses thereby minimizing the number of signal paths to and from the chip ....") (emphasis added); col. 3:31-34 (stating that a single clock pulse is used); col. 7:36-40; col. 8:13-15; col. 9:57-58; col. 14:14-18; col. 15:38-40. Furthermore, the patentees responded to the examiner's rejection by distinguishing their claimed invention from the Target Specification because the Target Specification did not operate on a single random port clock input: "the Target Specification does not operate in response to *a single* clock as claimed in claim 1.... The Target Spec [sic] ... requires more than one clock to perform this function." Response to Examiner at 115 (Exh. 5, Docket No. 120). A construction limiting clock signal to a single timing signal is consistent with the express purpose of the invention, the specification, and the prosecution history.

Clock signal

For the reasons discussed above in the construction of "external clock signal," the Court construes "clock signal" as "a single timing signal."

Dynamic random state machine

The Court adopts the construction of "dynamic random state machine" that the parties agreed to at the claim construction hearing: "a dynamic sequential-logic system whose outputs depend on previous and present inputs on the random port, as opposed to processes that are functions of present inputs alone." FN2 Hr'g Tr. at 73.

FN2. According to the transcript, the Court misstated the parties' agreed upon construction as "a dynamic sequential-logic system whose outputs depend on previous and present inputs on the random *board* as opposed to processes that are functions of present inputs alone." Hr'g Tr. at 73. From the context of the patent, the hearing, the briefing, and the parties' Joint Third Supplemental Claim Construction Chart (Docket No. 141), it is clear the construction stated above is the parties' agreed construction.

Random state machine

The Court adopts the construction of "random state machine" that the parties agreed to at the claim construction hearing: "a sequential-logic system whose outputs depend on previous and present inputs on the random port, as opposed to processes that are functions of present inputs alone." FN3 Hr'g Tr. at 73-74.

FN3. According to the transcript, the Court misstated the parties' agreed upon construction as "a sequential-logic system whose outputs depend on previous and present inputs on the random *board* as opposed to processes that are functions of present inputs alone." Hr'g Tr. at 73-74. From the context of the patent, the hearing, the briefing, and the parties' Joint Third Supplemental Claim Construction Chart (Docket No. 141), it is clear the construction stated above is the parties' agreed construction.

Access information

The Court agrees with MEI and construes "access information" as "information that specifies a memory access." To access memory, the memory address of the information and the operation to be performed at that location are needed. *See* '921 Patent col. 11:30-40, Figs. 12 & 13. Samsung's proposed construction-"drawing rules (DR), start/stop bits, and H/V bit"-improperly imports limitations from a preferred embodiment. *See* Turbocare Div. v. Gen. Elec. Co., 264 F.3d 1111, 1123 (Fed.Cir.2001) (citing Laitram Corp. v. Cambridge Wire Cloth Co., 863 F.2d 855, 865 (Fed.Cir.1988) ("References to a preferred embodiment, such as those often present in a specification, are not claim limitations.")).

Access information defining a specification of said operation mode

The Court agrees with MEI and construes the phrase as "information defining a specification for an operation mode." As discussed above, Samsung's proposed construction-"drawing rules (DR), start/stop bits, and H/V bits provide further details of the operation mode, as defined in Table II"-improperly imports limitations from a preferred embodiment.

Access information defining a specification of said operation mode in combination with said external control input defining said operation mode

The Court construes the phrase as "information defining a specification for an operation mode, which, together with external control input, defines the specifics of the operation mode." Samsung's proposed construction-"drawing rules (DR), start/stop bits, and H/V bits provide further details of the operation mode, as defined in Table II"-improperly imports limitations from a preferred embodiment.

Output means

The parties agree this term is subject to 35 U.S.C. s. 112, para. 6 and agree to the corresponding function in each disputed claim.FN4 The corresponding structure for claim 66 of the ' 921 patent and claim 47 of the ' 680 patent is "dynamic latch 1304, serial data port 1306, and output control 1338." MEI argues that the corresponding structure is "output control 1338," and Samsung argues it is "dynamic latch 1304 and serial data port 1306." MEI's identified structure is on the random port side of the chip, and Samsung's identified structure is on the serial side of the chip. The parties have agreed that the corresponding structure for "output

means" is "output control 1338" for every claim except claim 66 of the ' 921 patent and claim 47 of the ' 680 patent. The output means sequentially outputs data in these two claims but not the other claims that include an "output means." Samsung argues that the "sequentially" limitation requires the data to be output over the sequential port because the serial port is specifically designed to output serial data and the specification uses the term "sequentially" in reference to the serial port side. ' 921 Patent col. 9:25-10:34; Hr'g Tr. at 101-02.

FN4. The parties agree that the function for each disputed means-plus-function term is what each claim specifies. Because the agreed functions often vary between the claims-at-issue for the same means-plus-function term, this opinion addresses only structure. The parties' agreed functions are identified for each claim in Appendix B.

MEI argues that output control 1338 is the corresponding structure because that is consistent with the agreed corresponding structure of "output means" in other claims. However, the claims-at-issue are different from those to which the parties agreed that output control 1338 is the corresponding structure. First, there is the additional "sequentially" limitation between the language of the claims-at-issue and the agree-to claims. Second-and importantly-claims 5 and 8 of the '921 patent are clearly restricted to "random port," and output control 1338 is thus the obvious structural choice. None of the other claims using the agreed-upon structure of output means are so restricted. Thus it could be readily argued that these other claims are broad enough to include the serial port. However, other limitations in those claims preclude a serial port structure for output means. Third, in claims 11, 17, 29 and 59 of the ' 921 patent the "access means comprises output means ... in response to a third edge of said external clock signal." Both parties agree that output control 1338 is a part of the structure for access means, and thus it is must be at least a part of the structure for the output means in these claims. Fourth, the "in response to a third edge ..." language (also found in claims 31 and 35) distinguishes these claims from the two at issue. Finally, MEI did not demonstrate that the limitations of the claims-at-issue are essentially the same as the limitations in the claims where the parties agreed that output means corresponds to output control 1338. In short, the corresponding structure of "output means" varies between claims.

Samsung conceded at the claim construction hearing that the random port side could sequentially output data. The claims-at-issue are directed to a random access memory, and nothing in the specification or claims prevents the output means from using the random port side. *See* '680 Patent col. 24:16-24; '921 Patent col. 28:48-68. MEI did not dispute that the serial port side structure could also perform the recited function. Accordingly, the corresponding structure is both "output control 1338" on the random port side and "dynamic latch 1304 and serial data port 1306" on the serial port side.

Access means

The parties agree this term is subject to 35 U.S.C. s. 112, para. 6. The Court agrees with Samsung that the corresponding structure is "output control 1338, write mask 1336, and drawing rule 1354." MEI argues that drawing rule 1354 should not be included. The only structure identified in the '921 and '680 patent specification includes the drawing rule. See '921 Patent Fig. 13; ' 680 Patent Fig. 13. The only way for 'NEW' data to access the memory block is through the drawing rule 1354. MEI argues that one of ordinary skill would understand that data could go through the write mask in an unmodified form and therefore it is unnecessary to disclose that structure. However, the write mask is not clearly linked to the recited function and is therefore not corresponding structure. *See* Medtronic, Inc., 248 F.3d at 1311 (stating that corresponding structure must be "clearly linked or associated with the [recited] function").

Writing means/write means/means for writing

The parties agree this term is subject to 35 U.S.C. s. 112, para. 6. The Court agrees with Samsung that the corresponding structure is "write mask 1336 and drawing rule 1354." MEI argues that "drawing rule 1354" should not be included. As discussed above for "access means," the only corresponding structure identified that clearly links reading/writing to memory includes the drawing rule 1354. Accordingly, drawing rule 1354 is corresponding structure.

Access information input means

The parties agree this term is subject to 35 U.S.C. s. 112, para. 6. At the claim construction hearing, Samsung did not object to MEI's identified structure. The Court has no objection to MEI's proposal. Accordingly, the corresponding structure is "address register 1320 and data register 1340."

Decoding means

The parties agree this term is subject to 35 U.S.C. s. 112, para. 6. The Court agrees with MEI that the corresponding structure is "state machine 1366." Samsung argues that the corresponding structure is "decoding circuitry in random state machine 1366, Table V and Table VI." However, the specification expressly states that the approach set forth in the tables is a preferred embodiment and "that other configurations of control signals and states can be defined under the teachings of the present invention." '921 Patent. col. 15:52-56. The patent identifies the corresponding structure as "state machine 1366." Importing limitations from a preferred embodiment of a state machine is improper.

Address providing means

The parties agree this term is subject to 35 U.S.C. s. 112, para. 6. The Court agrees with MEI that the corresponding structure is "a processor (CPU), a bus 170, and an interface circuit 160." Samsung argues that the corresponding structure is "graphics hardware 110." Samsung argues that the graphics hardware 110 is the only structure identified that provides the address. *See* '680 Patent Fig. 1. However, the intrinsic record shows that it is the CPU, not shown in Figure 1, that generates the address information. *See* '680 patent col. 4:53-65.

Graphics hardware 110 is part of a preferred embodiment directed at video applications-it is not a necessary structure. The graphics hardware passes on information generated by the CPU and sent over bus 170 and interface circuit 160. In non-video applications, the graphics hardware 110 is not present and is not needed to pass along the address information. Including graphics hardware 110 would effectively limit the patent to a preferred embodiment and scale back the patent to its original state, before the PTO granted a reissue broadening the patent's scope.

Data providing means

The parties agree this term is subject to 35 U.S.C. s. 112, para. 6. The Court agrees with MEI that the corresponding structure is "a processor (CPU), a bus 170, and an interface circuit 160." Samsung argues that the corresponding structure is "graphics hardware 110." As discussed above for "address providing means," graphics hardware 110 is part of a preferred embodiment and is not required corresponding structure.

Control input providing means

The parties agree this term is subject to 35 U.S.C. s. 112, para. 6. The Court agrees with MEI that the corresponding structure is "a processor (CPU), a bus 170, and an interface circuit 160." Samsung argues that the corresponding structure is "circuitry of random port control 120." As for "data providing means" and "address providing means," the CPU provides the information, using the bus 170 and an interface circuit 160. Samsung's proposed structure imports limitations from a specific embodiment in the patent directed at video applications.

Access information providing means

The parties agree this term is subject to 35 U.S.C. s. 112, para. 6. The Court agrees with MEI that the corresponding structure is "a processor (CPU), a bus 170, and an interface circuit 160." As with "address providing means" discussed above, Samsung's proposed corresponding structure-"circuitry of graphics hardware 110 and Figures 14 and 15"-attempts to read in limitations from a preferred embodiment directed at video applications.

THE '588 PATENT

Protective MOS transistor

The Court agrees with MEI and construes the term as "a MOS transistor that provides a discharge path for current to flow from the first power supply terminal to the second power supply terminal when activated by a voltage on the drain that exceeds a predetermined level." Samsung argues that the term should be construed as "a MOS transistor that shunts the surge/ESD event by the breakdown of the MOS transistor due to the punch-through effect."

Both parties agree that the protective MOS transistor provides a discharge path or shunts current. Samsung's proposed construction limits the claim to "punch-thru effect" MOS breakdowns. Samsung argues that the patentees disclaimed breakdown of the MOS by avalanche effect in statements made during patent prosecution. *See* '588 Pros. Hist., June 3, 1992 Amendment at 9 (Docket No. 120, Exh. 9). The applicants' discussion of punch-through effect in the prosecution history is not a clear disclaimer of claim scope for numerous reasons. First, the patent specification shows a MOS transistor configured to operate in an avalanche mode. *See* '588 Patent Fig. 5. Second, the applicants' statements that the MOS transistor could operate in "punch-through" mode were not critical to distinguishing the claimed invention over the prior art, and the applicants never limited the MOS transistor to operating in the punch-through mode. *See* Pros. Hist., June 3, 1992 Amendment at 9-10 (distinguishing Armstrong prior art reference as capable of operating in avalanche mode *only,* whereas applicants' invention was capable of operating in punch-through mode).

Peripheral region of the semiconductor chip

The Court agrees withe MEI and construes the term as the "region outside the area of the semiconductor chip in which the internal circuit is formed." Samsung's proposed construction-"the outermost region of the semiconductor chip"-merely substitutes "outermost" for "peripheral." The claim language recites "a surge protection apparatus for protecting an *internal* circuit." ' 588 Patent col. 9:3-8 (emphasis added). The surge protection apparatus is formed outside of the internal circuit. "Peripheral" in this context connotes an area outside of the internal circuit. Furthermore, there is no basis to require this surge protection apparatus be built on the "outermost" area of a chip.

Plural protective transistors

The Court modifies MEI's proposal and construes the term as "multiple transistors which provide a discharge path for current to flow between the first power supply wire and the second power supply wire when activated." MEI's argument that "plural" in this claim has a special meaning-i.e., "three or more"-is unsupported. Also, "plural" is used in a means-plus-function term in claim 2. MEI agreed to a construction of that term that does not include a special "three or more" construction of "plural." *See* Third Amended Joint Supp. Claim Const. Chart at 55 (Docket No. 141); Fin Control Sys. Pty, Ltd. v. OAM, Inc., 265 F.3d 1311, 1318 (Fed.Cir.2001) ("[T]he same terms appearing in different portions of the claims should be given the same meaning unless it is clear from the specification and prosecution history that the terms have different meanings at different portions of the claims.").

Protective transistor

The Court agrees with MEI and construes the term as "a transistor which provides a discharge path for current to flow between the first power supply wire and the second power supply wire when activated." FN5 This term simply refers to a single one of the "plural protective transistors" of claim 2. *See* '588 col. 9:3-14; col. 10:10-13.

FN5. In the parties' Joint Claim Construction Charts, MEI's proposed construction is listed as "a transistor which provides a discharge path for current to *follow* between the first power supply wire and the second power supply wire when activated." However, MEI's brief and its construction of "plural protective transistors" use the word "flow" rather than "follow." Accordingly, the Court construes the term as stated above using the word "flow."

Internal circuit

The Court modifies MEI's proposed construction and construes the term as "the internal circuit which is protected by the surge protection apparatus." Samsung's proposed construction-"a circuit that is protected by the surge protection apparatus and is internal to the semiconductor integrated circuit"-imports limitations from claim 2 that do not appear in claim 1. There is no basis for importing a "semiconductor integrated circuit" limitation into the term. *See* '588 Patent Figs. 1, 2, 3, 5, 6, 10-12 (illustrating circuit diagrams that are not limited to semiconductor integrated circuits).

THE '195 PATENT

Plug electrode

The Court combines the parties' proposals and construes the term as "a metal conductor formed in a contact hole, which connects two layers." Samsung's proposed construction-"a conductor formed in a contact hole"-is consistent with the specification, the claims, and the agreed-upon construction of "contact hole"-"a vertical hole that allows electrical contact." *See* '195 Patent col. 5:63-67. However, the Court agrees with MEI that the specification discloses only a metal plug. *See* '195 Patent col. 14:49; col. 15:6; col. 19:29-34, 49; col. 20:6, 9, 23; and all figures referenced therein. MEI's proposed construction-"a metal which connects two metal layers"-is too narrow because it improperly includes what the electrode is connected to. MEI's definition is also too broad because it encompasses all metal regardless of conductivity.

Formed on said layer insulating film

This phrase does not require construction. Samsung's proposed construction-"formed on a thin layer of material that is a poor conductor of electricity"-adds additional limitations that are not supported by the claims and may themselves require construction (i.e., "thin," and "poor conductor"). MEI argues that the phrase should be construed as "arranged on the uppermost surface of the layer insulating film." However, MEI does not explain how "arranged on the uppermost layer" is more helpful to a jury than "formed on." Accordingly, the Court does not construe the term.

Formed in a plural number

The Court agrees with MEI and construes the term as "two or more plug electrodes are formed." Samsung argues that the phrase cannot be understood or construed. The claim language is awkward: "wherein said plug electrode is formed in a plural manner and said plug electrodes are connected respectively to both sides ...." '195 Patent col. 22:47-48. The grammatical error in the claim-at-issue does not cast its meaning into doubt so as to render it indefinite. The inventor's intent here is clear-plural means more than one. The intrinsic evidence shows multiple plug electrodes connected to a fuse portion. *See* '195 Patent Figs. 9g, 11e. Samsung fails to demonstrate that a person of ordinary skill in the art would not understand the claim as written.

Plug electrodes are connected respectively to both sides which are positioned across a part of said fuse portion where cutting off is to be performed

The Court agrees with MEI and construes the term as "at least one plug electrode connected to the fuse portion on each side of the region where the fuse may be cut." Samsung argues that the phrase cannot be understood or construed because this phrase appears in a claim 2, which depends from claim 1, and claim 1 is ambiguous because a plug electrode cannot be "formed in a plural number." Samsung's argument that "connected respectively to both sides" cannot be understood fails in light of the intrinsic evidence, which describes plug electrodes connected across either side of a fuse portion. *See* '195 Patent Figs. 9g, 11e; col. 19:15-35.

CONCLUSION

For the foregoing reasons, the Court interprets the claim language in this case in the manner set forth above. For ease of reference, the Court's claim interpretations are set forth in a table as Appendix B. The claims with the disputed terms are set forth in Appendix A.

So ORDERED.

APPENDIX A

U.S. Patent No. 5,091,339

11. A method for fabricating a multilayer electrical interconnect, comprising the following steps in the sequence set forth:

(a) providing an insulating layer on a base;

(b) forming a channel in the top surface and partially through the thickness of the insulating layer;

(c) forming a via in the top surface and completely through the thickness of the insulating layer adjacent the channel;

wherein forming the channel and via in steps (b) and (c) comprises:

covering the insulating layer with a first soft mask having an opening to expose the via but covering the channel, wherein the first soft mask is erodible by a first etch;

applying a first etch to remove material from the insulating layer where the via is exposed and to either partially or completely erode the first soft mask;

covering the insulating layer with a second soft mask having an opening to expose the channel and via, wherein the second soft mask is erodible by a second etch; and

applying a second etch to remove material from the insulating layer where the channel is exposed and material from the insulating layer remaining where the via is exposed until the second soft mask is either partially or completely eroded and the channel and via are etched, thereby forming the channel and via;

(d) depositing an electrical conductor into the channel and via; and

(e) planarizing the interconnect top surface so that the electrically conductive layer remains only in the channel and via and is otherwise removed from the top surface of the insulating layer, and the interconnect top surface is substantially smooth, thereby forming an electrically conducting channel interconnect to an electrically conducting via.

U.S. Patent No. 5,173,442

3. A method of forming a channel and a via in an insulating layer, said channel being a horizontally disposed in the top surface of and partially through the thickness of the insulating layer and said via being adjacent to the channel and vertically disposed and completely through the thickness of the insulating layer, said method comprising the steps of:

covering the insulating layer with a first soft mask having an opening to expose the via but covering the channel wherein the first soft mask is erodible by a first etch;

applying the first etch to at least partially remove the insulating layer where the vis is exposed;

covering the insulating layer with a second soft mask having an opening to expose the channel and the via wherein the second soft mask is erodible by a second etch; and

applying the second etch to remove the insulating layer where the channel is exposed and to remove any of the insulating layer remaining where the via is exposed so that the channel and the via are formed.

U.S. Patent RE 36,490

1. A memory device formed on a semiconductor substrate having *peripheral* circuitry positioned adjacent a single memory cell array, said memory device comprising:

a plurality of power lines formed above said single memory cell array for supplying power to said *peripheral* circuitry, each power line being substantially parallel to and spaced apart from every other power line; and

a plurality of ground lines formed above said single memory cell array for supplying ground potential to said *peripheral* circuitry, each ground line being substantially parallel to and spaced apart from every other ground line.

3. A method of forming power and signal lines on a memory device, said memory device being formed on a semiconductor substrate and having a single memory cell array and *peripheral circuitry adjacent said memory cell array,* comprising the steps of:

forming a plurality of substantially parallel power lines above said single memory cell array *for supplying power to said peripheral circuitry;*

forming a plurality of substantially parallel ground lines above said single memory cell array *for supplying ground potential to said peripheral circuitry;* and

forming a plurality of signal lines above said single memory cell array *for supplying signals to said peripheral circuitry*.

U.S. Patent RE 35,921

5. An improved random port for a dynamic random access memory which includes a plurality of memory cells for storing information, said random port and said dynamic random access memory being on a single integrated circuit chip, said random port being connectable to an address bus, a data bus, and a control bus including an external clock signal, said improved random port comprising:

address means connected to said address bus for holding a first address of information stored in said dynamic random access memory in response to a first edge of said external clock signal, and for holding a second address of said information stored in said dynamic random access memory in response to a second edge of said external clock signal, said first edge of said external clock signal being different from said second edge said external clock signal;

output means connected to said dynamic random access memory for delivering said stored information at said first and second addresses from said memory to said data bus; and

control means connected to said control bus for receiving said external clock signal from said control bus and being further connected to said address means, said output means and said dynamic random access memory, said control means being responsive to the receipt of said external clock signal for controlling the operation of said address means, said output means, and said dynamic random access memory.

6. The improved random port of claim 5, wherein said control means is a dynamic random state machine responsive to a control input provided on said control bus for producing predetermined sequences of

internal control pulses in synchronization with said external clock signal.

7. The improved random port of claim 5, further comprising:

data input means connected to said data bus for receiving data and for holding said data in response to an edge of said external clock signal; and

writing means for writing said held data to said memory.

8. A synchronous dynamic random access memory, comprising:

a memory block residing on an integrated circuit chip and including a plurality of memory cells for storing information; and

a random port residing on said integrated circuit chip and connectable to an address bus, a data bus, and a control bus including an external clock signal, said random port including:

address means connected to said address bus for holding a first address of information stored in said dynamic random access memory in response to a first edge of said external clock signal and for holding a second address of said information stored in said dynamic random access memory in response to a second edge of said external clock signal, said first edge of said external clock sign b different from said second edge of said external clock signal;

output means connected to said dynamic random access memory for delivering said stored information at said first and second addresses from said memory block to said data bus; and

control means connected to said control bus for receiving said external clock signal from said control bus and being further connected to said address means, said output means and said dynamic random access memory, said control means being responsive to the receipt of said external clock signal for controlling the operation of said address means, said output means, and said memory block.

9. The memory of claim 8, wherein said control means is a dynamic random state machine responsive to a control input provided on said control bus for producing predetermined sequences of internal control pulses in synchronization with said external clock signal.

10. A synchronous dynamic random access memory integrated circuit comprising:

a memory block including a plurality of memory cells for storing information;

an input for receiving an external clock signal;

address input means for receiving a first address and a second address defining a location of information stored in said memory block, said address input means providing said first address as an output in response to a first edge of said external clock signal, said address input means providing said second address as an output in response to a second edge of said external clock signal, said first edge of said external clock signal being different from said second edge of said external clock signal; and

access means for accessing a location in said memory block corresponding to said first address and said second address provided by said address input means.

11. The memory of claim 10, wherein said access means comprises output means for outputting information stored at said location of said memory block in response to a third edge of said external clock signal.

12. The memory of claim 10, further comprising:

mask information input means for receiving mask information, said mask information input means providing said mask information as an output in response to a third edge of said external clock signal, and

wherein said access means comprises:

write mask means for generating a write prohibition signal for prohibiting writing information to at least one bit location in said memory block based on said mask information; and

write means for writing said information to said memory block in accordance with said write prohibition signal within a region in said memory block corresponding to said first address and said second address provided by said address input means.

16. The memory of claim 12, wherein said write means writes said information to said memory block in response to a fourth edge of said external clock signal.

17. The memory of claim 11, further comprising:

control means for supplying a first enable signal and a second enable signal to said address input means in response to an external control input on an edge of said external clock signal, and for supplying an output enable signal to said output means in response to said external control input on an edge of said external clock signal, each of said first enable signal, said second enable signal and said output enable signal being synchronous with an edge of said external clock signal,

wherein said address input means provides said first address in response to said first enable signal, said address input means provides said second address in response to said second enable signal, and said output means outputs said information in response to said output enable signal.

18. The memory of claim 10, wherein said access means comprising:

data input means for receiving data, said data input means providing said data as an output in response to an edge of said external clock signal; and

write means for writing said data to said memory block at a location addressed by said first address and said second address in response to an edge of said external clock signal.

19. The memory of claim 18, further comprising:

control means for supplying a data enable signal to said data input means in response to an external control input on an edge of said external clock signal, and for supplying a write enable signal to said write means in

response to said external control input on an edge of said external clock signal, each of said data enable signal and said write enable signal being synchronous with an edge of said external clock signal,

wherein said data input means provides said data in response to said data enable signal, and said write means writes said data in response to said write enable signal.

20. The memory of claim 10, wherein said external clock signal has a frequency of about 16.7 MHz.

23. A synchronous dynamic random access memory integrated circuit comprising:

a memory block including a plurality of memory cells for storing information;

can input for receiving an external clock signal;

address input means for receiving a first address and a second address defining a location of information stored in said memory block, said address input means providing said first address as an output in response to a first enable signal, and said address input means providing said second address as an output in response to a second enable signal;

access means for accessing a location in said memory block corresponding to said first address and said second address provided by said address input means;

control means for supplying said first enable signal and said second enable signal to said address input means in response to an external control input on an edge of said external clock signal, and for supplying said output enable signal to said output means in response to said external control input on an edge of said external clock signal, each of said first enable signal, said second enable signal and said output enable signal being synchronous with an edge of said external clock signal.

24. The memory of claim 23, wherein said access means comprises:

data input means for receiving data, said data input means providing said data as an output in response to a data enable signal,

write means for writing said data to said memory block at a location addressed by said first address and said second address in response to a write enable signal,

wherein said control means supplies said data enable signal to said data input means in response to said external control input on an edge of said external clock signal, and supplies said write enable signal to said write means in response to said external control input on an edge of said external clock signal, each of said data enable signal and said write enable signal being synchronous with an edge of said external clock signal.

26. The memory of claim 24, wherein

said control means comprises:

means for determining a next state in response to a current state and said external control input on an edge

of said external clock signal; and

means for producing said first enable signal, said second enable signal, said output enable signal, said data enable signal and said write enable signal as a function of said next state.

28. The memory of claim 23, wherein said external clock signal has a frequency of about 16.7 MHz.

31. In a synchronous memory integrated circuit including a memory block having a plurality of memory cells for storing information; address input means for receiving a first address and a second address defining a location of information stored in said memory block: output means for outputting information from said memory block; and an input for receiving an external clock signal,

a method for reading information from said memory block, comprising the steps of:

a) providing said first address as an output of said address input means in response to a first edge of said external clock signal;

b) providing said second address as an output of said address input means in response to a second edge of said external clock signal, said first edge of said external clock signal being different from said second edge of said external clock signal; and

c) outputting information stored at a location of said memory block addressed by said first address and said second address on a third edge of said external clock signal.

33. In a synchronous memory integrated circuit including a memory block having a plurality of memory cells for storing information; address input means for receiving a first address and a second address defining a location of information stored in said memory block; data input means for receiving data; write means for writing said data into said memory block; and an input for receiving an external clock signal,

a method for writing data into said memory block, comprising the steps of:

a) providing said first address as an output of said address input means in response to a first edge of said external clock signal;

b) providing said second address as an output of said address input means in response to a second edge of said external clock signal, said first edge of said external clock signal being different from said second edge of said external clock signal;

c) providing said data as an output of said data input means in response to an edge of said external clock signal; and

d) writing said data into said memory block at a location addressed by said first address and said second address on an edge of said external clock signal.

35. In a synchronous memory integrated circuit including a memory block having a plurality of memory cells for storing information; address input means for receiving a first address and a second address defining a location of information stored in said memory block; output means for outputting information

from said memory block; data input means for receiving data: write means for writing said data into said memory block; and an input for receiving an external clock signal,

a method for reading and writing information from said memory block, comprising the steps of:

a) providing said first address as an output of said address input means to response to a first edge of said external clock signal;

b) providing said second address as an output of said address input means in response to a second edge of said external clock signal, said first edge of said external clock signal being different from said second edge of said external clock signal;

c) outputting information stored at a location of said memory block addressed by said first address and said second address on a third edge of said external clock signal;

d) providing said data as an output of said data input means in response to an edge of said external clock signal; and

e) writing said data into said memory block at said location addressed by said first address and said second address on an edge of said external clock signal.

36. A synchronous dynamic random access memory integrated circuit, comprising:

an input for receiving an external clock signal;

a memory block;

an address buffer in which an address from a first address and a second address bus are loaded in response to a first load enable signal and a second load enable signal, respectively, said first address and said second address representing an addressable memory location in said memory block;

means for reading information stored at said addressable memory location;

means for outputting said information read from said memory to a data bus in response to an output enable signal; and

a digital control circuit for controlling said address buffer and said means for outputting, said control circuit comprising logic clocked by said external clock signal during a read operation to generate said first and second load enable signals in response to an edge of respective clock cycles in said external clock signal, and to generate said output enable signal in response to a subsequent edge of a clock cycle in said external clock signal.

38. The memory of claim 36, further comprising:

a data buffer in which data from a data bus is loaded in response to a data load enable signal;

means for writing said data loaded in said data buffer to said addressable memory location represented by

said address loaded in said address buffer; and

wherein said control circuit logic during a write operation generates said first and second load enable signals in response to an edge of respective clock cycles in said external clock signal, and generates said data load enable signal in response to an edge of a clock cycle in said external clock signal.

40. A synchronous dynamic random access memory integrated circuit connected to a first bus for specifying a location in said memory block and for inputting/outputting data, and a second bus for inputting an external control input defining an operation mode, comprising:

a memory block including a plurality of memory cells for storing information;

an input for receiving an external clock signal;

address input means for receiving a first address and a second address through said first bus, said address input means providing said first address as an output in response to a first edge of said external clock signal, said address input means providing said second address as an output in response to a second edge of said external clock signal, said first edge of said external clock signal being different from said second edge of said external clock signal;

access information input means for receiving access information through said first bus, said access information defining a specification of said operation mcomdeb ination with said external control input defining said operation mode, said access information input means providing said access information as an output in response to a third edge of said external clock signal;

access means for accessing a location in said memory block corresponding to said first address and said second address provided by said address input means in accordance with said operation mode and;

control means for receiving said external control input defining said operation mode through said second bus, and for controlling operations of said address input means, said access information input means and said access means in response to said external control input on an edge of said external clock signal.

41. The memory of claim 40, wherein said access means comprises:

write means for writing information to said memory block at a location corresponding to said first and said second address in response to a fourth edge of said external clock signal.

42. The memory of claim 41,

wherein said control means supplies a first enable signal and a second enable signal to said address input means in response to an external control input on an edge of said external clock signal, supplies an access information enable signal to said access information input means in response to said external control input on an edge of said external clock signal, and supplies a write enable signal to said write means in response to said external control input on an edge of said external clock signal, each of said first enable signal, said second enable signal, said access information enable signal and said write enable signal being synchronous with an edge of said external clock signal, and

wherein said address input means provides said first address in response to said first enable signal, said address input means provides said second address in response to said second enable signal, said access information input means provides said access information in response to said access information enable signal, and said write means writes said information in response to said write enable signal.

48. The memory of claim 47,

wherein said control means supplies a first enable signal and a second enable signal to said address input means in response to said external control input on an edge of said external clock signal, and supplies an output enable signal to said output means in response to said external control input on an edge of said external clock signal, each of said first enable signal, said second enable signal and said output enable signal being synchronous with an edge of said external clock signal, and

wherein said address input means provides said first address in response to said first enable signal, said address input means provides said second address in response to said second enable signal, and said output means outputs said information in response to said output enable signal.

50. The memory of claim 49,

wherein said control means supplies a data enable signal to said data input means in response to said external control input on an edge of said external clock signal, and supplies a write enable signal to said write means in response to said external control input on an edge of said external clock signal, each of said data enable signal and said write enable signal being synchronous with an edge of said external clock signal,

wherein said data input means provides said data in response to said data enable signal, and said write means writes said data in response to said write enable signal.

53. A synchronous semiconductor memory integrated circuit comprising:

a memory block including a plurality of memory cells for storing information;

an input for receiving an external clock signal;

address input means for receiving a first address and a second address, said address input means providing said first address as an output in response to an edge of said external clock signal, said address input means providing said second address as an output in response to an edge of said external clock signal;

access means for accessing a location in said memory block corresponding to said first address and said second address provided by said address input means and;

control means for outputting an internal control signal defining a timing of an internal operation of said synchronous semiconductor memory in response to an external control input on an edge of said external clock signal;

wherein said control means generates new state information in accordance with an external control input and state information output in response to a first edge of said external clock signal, and outputs a new

internal control signal based on said new state information in response to a second edge of said external clock signal, said first edge of said external clock signal being different from said second edge of said external clock signal.

54. The memory of claim 53, wherein said external control input is on said second edge of said external clock signal.

55. The memory of claim 54, wherein said control means generates further new state information in accordance with an external control input on a third edge of said external clock signal and said new state information, and outputs a further new internal control signal based on said further new state information in response to said third edge of said external, clock signal, said second edge of said external clock signal being different from said third edge of said external clock signal.

59. The memory of claim 53, wherein said access means comprises:

output means for outputting information stored at said location of said memory block in response to a third edge of said external clock signal.

61. The memory of claim 53, wherein said access means comprises:

data input means for receiving data, said data input means providing said data as an output in response to a third edge of said external clock signal; and

write means for writing said data to said memory block at a location corresponding to said first and said second address in response to a fourth edge of said external clock signal.

65. The memory of claim 53, wherein said state information may be any one of a first state information indicating an initial state and a plurality of second state information indicating respective states other than said initial state, and with respect to at least one of the plurality of second state information when said state information output in response to said first edge of said external clock signal is said at least one second state information, said new state information may be any one of a predefined plurality of second state information from among said plurality of second state information, each of said predefined plurality of second state information indicating respective states other than said initial state.

66. A synchronous dynamic random access memory integrated circuit a plurality of memory blocks including a plurality of memory cells for storing information;

an input for receiving an external clock input;

address input means for receiving a first address and a second address, said address input means providing said first address as an output in response to a first edge of said external clock input, said address input means providing said second address as an output in response to a second edge of said external clock input, said first edge of said external clock input being different from said second edge of said external clock input; and

output means for sequentially outputting a plurality of data which belong to separately addressable locations in said memory blocks at substantially a same interval, said plurality of data including data stored

at a location in said memory blocks corresponding to said first address and said second address provided by said address input means.

68. A synchronous dynamic random access memory integrated circuit comprising:

a memory block including a plurality of memory cells for storing information;

an input for receiving an external clock signal;

address input means for receiving a first address and a second address, said address input means providing said first address as an output in response to a first enable signal, said address input means providing said second address as an output in response to a second enable signal;

access means for accessing a location in said memory block corresponding to said first address and said second address provided by said address input means in response to a third enable signal; and

control means for receiving a first external control input indicating one of a read mode and a write mode and a second external control input which is different from said first external control input, for generating said third enable signal based on said first external control input and generating at least one of said first enable signal and said second enable signal based on said second external control input, and for supplying said third enable signal to said access means in response to an edge of said external clock signal and supplying at least one of said first enable signal and said second enable signal to said address input means in response to an edge of said external clock signal.

69. A synchronous dynamic random access memory integrated circuit which operates by use of edges of an external clock signal, said memory comprising:

a memory block including a plurality of memory cells for storing information;

an input for receiving an external clock signal;

address input means for receiving a first address and a second address, said address input means providing said first address as an output in response to a first edge of said external clock signal, said address input means providing said second address as an output in response to a second edge of said external clock signal, said first edge of said external clock signal being different from said second edge of said external clock signal;

access means for accessing a location in said memory block corresponding to said first address and said second address provided by said address input means;

control means for receiving an external control input indicating whether or not a precharge operation is performed, and for changing whether said precharge operation is performed based on a difference of level of said external control input at two successive edges of said edges of said external clock signal.

71. A synchronous semiconductor memory integrated circuit comprising:

a memory block including a plurality of memory cells for storing information;

an input for receiving an external clock signal;

address input means for receiving a first address and a second address, said address input means providing said first address as an output in response to an edge of said external clock signal, said address input means providing said second address as an output in response to an edge of said external clock signal;

access means for accessing a location in said memory block corresponding to said first address and said second address provided by said address input means; and

control means for outputting an internal control signal defining a timing of an internal operation of said synchronous semiconductor memory in response to an external control input on an edge of said external clock signal;

wherein said control means comprises a random state machine.

72. The memory of claim 71, wherein said random state machine determines a new state based on said external control input and a current state, and outputs said internal control signal based on said new state in response to an edge of said external clock signal.

73. The memory of claim 72, wherein said random state machine comprises:

decoding means for decoding said new state so as to output said internal control signal.

75. A synchronous dynamic random access memory integrated circuit comprising:

a memory block including a plurality of memory cells for storing information;

an input for receiving an external clock signal;

an address input means for receiving a first address and a second address, said address input means providing said first address as an output in response to a first edge of said external clock signal, said address input means providing said second address as an output in response to a second edge of said external clock signal, said first edge of said external clock signal being different from said second edge of said external clock signal;

access means for accessing a location in said memory block corresponding to said first address and said second address provided by said address input means; and

control means for receiving a predetermined set of control signals provided from outside of said synchronous dynamic random access memory, for making a transition from a state to a next state in accordance with said predetermined set of control signals on respective edges of said external clock signal, and for outputting an internal control signal defining a timing of an internal operation of said synchronous dynamic random access memory based on the said next state;

wherein said predetermined set of control signals include a first control signal and a second control signal, said internal operation represents a write operation when said first control signal is in a first logic level and

said second control signal is in a second logic level, and said internal operation represents a read operation when said first control signal is in a third logic level which is different from the first logic level and said second control signal in said second logic level.

U.S. Patent RE 35,680

35. A system comprising a memory, a circuit for accessing said memory, and a bus connecting said circuit to said memory,

said circuit comprising means for providing a first address and a second address on said bus, said first address being valid on said bus on a first edge of a clock signal and said second address being valid on said bus on a second edge of said clock signal, said first edge of said clock signal being different from said second edge of said clock signal; and

said memory being a synchronous dynamic random access memory integrated circuit comprising:

a memory block including a plurality of memory cells for storing information;

an input for receiving said clock signal;

address input means for receiving and holding said first address from said bus in response to said first edge of said clock signal, and for receiving and holding said second address from said bus in response to said second edge of said clock signal; and

access means for accessing a location in said memory block corresponding to said first address and said second address held by said address input means.

36. The system of claim 35, wherein said access means comprises:

output means for outputting, to said bus, information stored at said location of said memory block in response to a third edge of said clock signal.

37. The system of claim 36,

said circuit for accessing further comprising:

means for providing on said bus a control input, said control input being valid on an edge of said clock signal,

said memory further comprising:

control means for supplying a first enable signal and a second enable signal to said address input means in response to said control input on an edge of said clock signal, and for supplying an output enable signal to said output means in response to said control input on an edge of said clock signal, each of said first enable signal, said second enable signal and said output enable signal being synchronous with an edge of said clock signal, and

wherein said address input means holds said first address based on said first enable signal, said address input means holds said second address based on said second enable signal, and said output means outputs said information based on said output enable signal.

38. The system of claim 35,

said circuit for accessing further comprising:

means for providing data on said bus which is valid on a third edge of said clock signal,

wherein said access means comprises:

data input means for receiving said data from said bus, said data input means holding said data in response to said third edge of said clock signal; and

write means for writing said data to said memory block at said location corresponding to said first address and said second address in response to a fourth edge of said clock signal.

39. The system of claim 38,

said circuit for accessing further comprising:

means for providing on said bus a control input, said control input being valid on an edge of said clock signal;

said memory further comprising:

control means for supplying a data enable signal to said data input means in response to said control input on an edge of said clock signal, and for supplying a write enable signal to said write means in response to said control input on an edge of said clock signal, each of said data enable signal and said write enable signal being synchronous with an edge of said clock signal, and

wherein said data input means provides said data to said write means in response to said data enable signal.

42. The system of claim 35, wherein:

said bus comprises a first bus on which said first address and said second address are provided and which also conveys data between said circuit and said memory, and a second bus connecting said circuit to said memory for conveying a control input defining an operation mode;

said circuit further comprises means for providing said control input on said second bus, and means for providing access information defining a specification of said operation mode on said first bus, said access information being valid on said first bus on a third edge of said clock signal, and said control input being valid on said second bus on an edge of said clock signal; and

said memory further comprises:

access information input means for receiving said access information through said first bus, said access information input means providing said access information as an output in response to said third edge of said clock signal; and

control means for receiving said control input through said second bus, and for controlling operations of said address input means, said access information input means and said access means in response to said control input on an edge of said clock signal.

45. The system of claim 35, wherein:

said circuit further comprises means for providing a control input on said bus, said control input being valid on said bus on an edge of said clock signal;

and said memory further comprising control means for outputting an internal control signal defining a timing of an internal operation of said synchronous dynamic random access memory based on a control input on an edge of said clock signal;

wherein said control means generates new state information in accordance with a control input and state information output in response to a third edge of said clock signal, and outputs a new internal control signal based on said new state information in response to a fourth edge of said clock signal, said third edge of said clock signal being different from said fourth edge of said clock signal.

47. The system of claim 35, wherein:

said memory block comprises a plurality of individual memory blocks and said access means further comprises output means for sequentially outputting a plurality of data which belong to separately addressable locations in said individual memory blocks at substantially a same interval, said plurality of data including data stored at a location in said memory block corresponding to said first address and said second address.

48. The system of claim 35, wherein:

said circuit further comprises means for providing a control input on said bus, said control input being valid on said bus on an edge of said clock signal; and

said memory comprises a random state machine.

49. The system of claim 48, wherein:

said random state machine determines a new state based on said control input and a current state, and outputs an internal control signal based on said new state in response to an edge of said clock signal, said internal control signal defining a timing of an internal operation of said memory.

50. The system of claim 49, wherein:

said random state machine comprises decoding means for decoding said new state so as to output said

internal control signal.

51. The system of claim 35, said memory further comprising:

control means for receiving a predetermined set of control signals provided from outside of said memory, for transition ing from one state to at least one next state in accordance with said predetermined set of control signals on respective edges of said clock signal, and for outputting internal control signals defining timings of internal operations of said memory based on the at least one next state;

wherein said predetermined set of control signals include a first control signal and a second control signal, said internal operations represent a write operation when said first control signal is active and said second control signal is active, and said internal operations represent a read operation when said first control signal is inactive and said second control signal is active.

U.S. Patent No. 5,189,588

1. A surge protection apparatus for protecting an internal circuit composed of MOS semiconductor elements comprising:

a signal terminal, a first power supply terminal and second power supply terminal connected to the internal circuit;

a first diode having an anode which is connected to said signal terminal and having a cathode which is connected to said first power supply terminal;

a second diode having a cathode which is connected to said signal terminal and having an anode which is connected to said second power supply terminal; and

a protective MOS transistor having a drain electrode which is connected to said first power supply terminal, and having a source electrode which is connected to said second power supply terminal and having a gate electrode which is connected to said source electrode.

2. A surge protection apparatus for protecting an internal circuit formed in a semiconductor chip comprising:

plural signal input/output pads and power supply pads formed in a peripheral region of the semiconductor chip;

first and second power supply wires connected to said power supply pads and disposed mutually adjacent to each other on the semiconductor chip;

a means for respectively connecting said plural signal input/output pads and said first and second power supply wires to the internal circuit;

plural first and second diodes, each of said first and second diodes respectively connected between said signal input/output pads and said first and second power supply wires; and

plural protective transistors connected between said first and second power supply wires and disposed

sporadically at plural positions along a longitudinal direction of said first and second power supply wires.

3. A surge protection apparatus as recited in claim 2, wherein said protective transistor is formed in the semiconductor substrate beneath said first or second power supply wire.

U.S. Patent No. 6,677,195

1. A semiconductor integrated circuit device having a plurality of wiring layers, said device comprising:

a layer insulating film formed over a semiconductor substrate,

a plug electrode which is formed in a contact hole that is disposed in said layer insulating film; and

a fuse portion which is configured by a metal wiring layer that is formed on said layer insulating film, said plug electrode being connected to a bottom portion of said fuse portion.

2. A semiconductor integrated circuit device according to claim 1, wherein said plug electrode is formed in a plural number and said plug electrodes are connected respectively to both sides which are positioned across a part of said fuse portion where cutting off is to be performed.

5. A semiconductor integrated circuit device according to claim 1, wherein said metal wiring layer contains an aluminum metal or an aluminum alloy which serves at least as a main conducting metal layer.

6. A semiconductor integrated circuit device according to claim 5, wherein in said fuse portion, a barrier metal layer is formed in at least a part of a layer below said main conducting metal layer.

7. A semiconductor integrated circuit device according to claim 5, wherein said plug electrode is made of tungsten, and a barrier metal layer is formed below said plug electrode.

8. A semiconductor integrated circuit device according to claim 2, wherein said metal wiring layer contains an aluminum metal or an aluminum alloy which serves at least as a main conducting metal layer.

9. A semiconductor integrated circuit device according to claim 2, wherein in said fuse portion, a barrier metal layer is formed in at least a part of a layer below said main conducting metal layer.

10. A semiconductor integrated circuit device according to claim 8, wherein said plug electrode are made of tungsten, and barrier metal layers are formed respectively below said plug electrode.

17. A semiconductor integrated circuit device according to claim 1, wherein an inorganic insulating protective film is formed on said metal wiring layer and said layer insulating film.

18. A semiconductor integrated circuit device according to claim 17, wherein said inorganic insulating protective film on said fuse portion has a thickness which is not smaller than 0.1 m and not larger than 0.8 m.

19. A semiconductor integrated circuit device according to claim 2, wherein an inorganic insulating protective film is formed on said metal wiring layer and said layer insulating film.

20. A semiconductor integrated circuit device according to claim 19, wherein said inorganic insulating protective film on said fuse portion has a thickness which not smaller than 0.1 m and than 0.8 m.

21. A semiconductor integrated circuit device according to claim 1, wherein a wiring width of said part of said fuse portion where cutting off is to be performed is not smaller than 0.1 m and not larger than 1.0 m.

APPENDIX B

Samsung's U.S. Patent No. 5,091,339 & U.S. Patent No. 5,173,442 AGREED CONSTRUCTIONS		
Claim(s)	Term	Agreed Construction
'339-Claim 11	depositing	A process for adding material to a semiconductor device.
'339-Claim 11	channel	A horizontal groove or trench that extends partially through the thickness of an insulating layer.
'442-Claim 3		
'339-Claim 11	covering the insulating layer with a second soft mask	This term requires no express construction because it can be understood from its plain and ordinary meaning.
'442-Claim 3		
'339-Claim 11	remove material from the insulating layer	This term requires no express construction because it can be understood from its plain and ordinary meaning.
'442-Claim 3	applying a second etch ... so that the channel and the via are formed	This term requires no express construction because it can be understood from its plain and ordinary meaning.
'339-Claim 11	applying a second etch ... until the second soft mask is either partially or completely eroded and the channel and via are etched, thereby forming the channel and via	This term requires no express construction because it can be understood from its plain and ordinary meaning.

Samsung's U.S. Patent No. 5,091,339 & U.S. Patent No. 5,173,442 DISPUTED CONSTRUCTIONS		
Claim(s)	Term	Court's Construction
'339-Claim 11	insulating layer	A layer made of one or more materials that are poor conductors of electricity.
'442-		

Claim 3		
'339-Claim 11	base	A structure on which a multilayer electrical interconnect is fabricated.
'339-Claim 11	via	A hole that vertically extends through an insulating layer.
'442-Claim 3		
'339-Claim 11	etch	A process or processes for removing one or more materials using chemical and/or physical means.
'442-Claim 3		
'339-Claim 11	soft mask	A mask is a n erodible layer of material used to cover selected areas of a surface during etch. A soft mask erodes more slowly than a hard mask, which erodes slowly or not at all.
'442-Claim 3		
'339-Claim 11	an opening to expose the channel and via	An opening in the second soft mask where the channel and via are to be formed.

'442-Claim 3

Samsung's U.S. Reissue Patent No. 36,490 AGREED CONSTRUCTIONS		
Claim(s)	Term	Agreed Construction
3	signal lines	Conducting paths that supply signals other than power and ground lines.
1 and 3	above said single memory cell array for supplying power to said peripheral circuitry	Over the single memory cell array to supply power to the peripheral circuitry and not directly to the single memory cell array.
1 and 3	above said single memory cell array for supplying ground potential to said peripheral circuitry	Over the single memory cell array to supply ground potential to the peripheral circuitry and not directly to the single memory cell array.
3	above said single memory cell array for supplying signals to said peripheral circuitry	Over the single memory cell array for supplying signals to the peripheral circuitry and not directly to the single memory cell array.
1	peripheral circuitry positioned adjacent a single memory cell array	Circuitry connected to the plurality of power lines and plurality of ground lines positioned next to and outside of the single memory cell array.

3	peripheral circuitry adjacent a said memory cell array	Circuitry connected to the plurality of power lines and plurality of ground lines next to and outside of said memory cell array.
1	each power line being substantially parallel to and spaced apart from every other power line	This term requires no express construction because it can be understood from its plain and ordinary meaning.
1	each ground line being substantially parallel to and spaced apart from every other ground line	This term requires no express construction because it can be understood from its plain and ordinary meaning.
3	substantially parallel power lines	This term requires no express construction because it can be understood from its plain and ordinary meaning.
3	substantially parallel ground lines	This term requires no express construction because it can be understood from its plain and ordinary meaning.

Samsung's U.S. Reissue Patent No. 36,490 DISPUTED CONSTRUCTIONS		
Claim(s)	Term Court's	Construction
3	memory cell array	A coordinated group or matrix of memory cells.
		[Agreed to at the hearing.]
1 and 3	single memory cell array	No construction necessary.
1 and 3	power lines	Conducting paths that provide electric power.
1 and 3	ground lines	Conducting paths that provide a connection to the ground.

MEI's U.S. Reissue Patent No. 35,921 & U.S. Reissue Patent No. 35,680 AGREED CONSTRUCTIONS		
Claim(s)	Term	Agreed Construction
'921-Claim 40	first bus	A first set of signal lines over which information is transmitted to or from a device.
'680-Claim 42		
'921-Claim 40	second bus	A second set of signal lines over which information is transmitted to or from a device.
'680-Claim 42		
'921-Claim 40	operation mode	A manner in which a device operates.
'680-		

Claim 42		
'921-Claim 36	digital control circuit	This term requires no express construction because it can be understood from its plain and ordinary meaning.
'921-Claims 6 and 9	dynamic random state machine	A dynamic sequential-logic system whose outputs depend on previous and present inputs on the random port, as opposed to processes that are functions of present inputs alone.
'921-Claims 71-73	random state machine	A sequential-logic system whose outputs depend on previous and present inputs on the random port, as opposed to processes that are functions of present inputs alone.

'680-Claims 48-50		
'921-Claim 5	address means	Function: For holding a first address of information stored in said dynamic random access memory in response to a first edge of said external clock signal, and for holding a second address of said information stored in said dynamic random access memory in response to a second edge of said external clock signal.
	Governed by 35 U.S.C. s. 112 para. 6.	Corresponding structure: address register (1320) and equivalents thereof.
'921-Claim 8	address means	Function: for holding a first address of information stored in said dynamic random access memory in response to a first edge of said external clock signal and for holding a second address of said information stored in said dynamic random access memory in response to a second edge of said external clock signal, said first edge of said external clock sign b[sic] different from said second edge of said external clock signal.
	Governed by 35 U.S.C. s. 112 para. 6.	Corresponding structure: address register (1320) and equivalents thereof.
'921-Claim 10	address input means	Function: for receiving a first address and a second address defining a location of information stored in said memory block, said address input means providing said first address as an output in response to a first edge of said external clock signal, said address input means providing said second address as an output in response to a second edge of said external clock signal, said first edge of said external clock signal being different from said second edge of said external clock signal.
	Governed by 35 U.S.C. s. 112 para. 6.	Corresponding structure: address register (1320) and equivalents thereof.
'921-Claim 17	address input means	Function: provides said first address in response to said first enable signal, said address input means provides said second address in response to said second enable signal.

	Governed by 35 U.S.C. s. 112 para. 6.	Corresponding structure: address register (1320) and equivalents thereof.
'921-Claim 23	address input means	Function: for receiving a first address and a second address defining a location of information stored in said memory block, said address input means providing said first address as an output in response to a first enable signal, and said address input means providing said second address as an output in response to a second enable signal.
	Governed by 35 U.S.C. s. 112 para. 6.	Corresponding structure: address register (1320) and equivalents thereof.
'921-Claim 31	address input means	Function: for receiving a first address and a second address defining a location of information stored in said memory block.
	Governed by 35 U.S.C. s. 112 para. 6.	Corresponding structure: address register (1320) and equivalents thereof.
'921-Claim 33	address input means	Function: for receiving a first address and a second address defining a location of information stored in said memory block.
	Governed by 35 U.S.C. s. 112 para. 6.	Corresponding structure: address register (1320) and equivalents thereof.
'921-Claim 35	address input means	Function: for receiving a first address and a second address defining a location of information stored in said memory block.
	Governed by 35 U.S.C. s. 112 para. 6.	Corresponding structure: address register (1320) and equivalents thereof.
'921-Claim 40	address input means	Function: for receiving a first address and a second address through said first bus, said address input means providing said first address as an output in response to a first edge of said external clock signal, said address input means providing said second address as an output in response to a second edge of said external clock signal, said first edge of said external clock signal being different from said second edge of said external clock signal.
	Governed by 35 U.S.C. s. 112 para. 6.	Corresponding structure: address register (1320) and equivalents thereof.
'921-	address	Function: provides said first address in response to said first enable signal, said

Claim 42	input means	address input means provides said second address in response to said second enable signal.
	Governed by 35 U.S.C. s. 112 para. 6.	Corresponding structure: address register (1320) and equivalents thereof.
'921-Claim 53	address input means	Function: for receiving a first address and a second address, said address input means providing said first address as an output in response to an edge of said external clock signal, said address input means providing said second address as an output in response to an edge of said external clock signal.
	Governed by 35 U.S.C. s. 112 para. 6.	Corresponding structure: address register (1320) and equivalents thereof.
'921-Claim 66	address input means	Function: for receiving a first address and a second address, said address input means providing said first address as an output in response to a first edge of said external clock input, said address input means providing said second address as an output in response to a second edge of said external clock input, said first edge of said external clock input being different from said second edge of said external clock input.
	Governed by 35 U.S.C. s. 112 para. 6.	Corresponding structure: address register (1320) and equivalents thereof.
'921-Claim 68	address input means	Function: for receiving a first address and a second address, said address input means providing said first address as an output in response to a first enable signal, said address input means providing said second address as an output in response to a second enable signal.
	Governed by 35 U.S.C. s. 112 para. 6.	Corresponding structure: address register (1320) and equivalents thereof.
'921-Claim 71	address input means	Function: for receiving a first address and a second address, said address input means providing said first address as an output in response to an edge of said external clock signal, said address input means providing said second address as an output in response to an edge of said external clock signal.
	Governed by 35 U.S.C. s. 112 para. 6.	Corresponding structure: address register (1320) and equivalents thereof.
'921-Claim 75	address input means	Function: for receiving a first address and a second address, said address input means providing said first address as an output in response to a first edge of said external clock signal, said address input means providing said second address as an output in response to a second edge of said external clock signal, said first edge of said external clock signal being different from said second edge of said

external clock signal.

	Governed by 35 U.S.C. s. 112 para. 6.	Corresponding structure: address register (1320) and equivalents thereof.
'680-Claim 35	address input means	Function: for receiving and holding said first address from said bus in response to said first edge of said clock signal and for receiving and holding said second address from said bus in response to said second edge of said clock signal.

	Governed by 35 U.S.C. s. 112 para. 6.	Corresponding structure: address register (1320) and equivalents thereof.
'680-Claim 37	address input means	Function: holds said first address based on said first enable signal, said address input means holds said second address based on said second enable signal.

	Governed by 35 U.S.C. s. 112 para. 6.	Corresponding structure: address register (1320) and equivalents thereof.
'921-Claim 5	output means	Function: for delivering said stored information at said first and second addresses from said memory to said data bus.

	Governed by 35 U.S.C. s. 112 para. 6.	Corresponding Structure: output control (1338) and equivalents thereof.
'921-Claim 8	output means	Function: For delivering said stored information at said first and second addresses from said memory block to said data bus.

	Governed by 35 U.S.C. s. 112 para. 6.	Corresponding Structure: output control (1338) and equivalents thereof.
'921-Claim 11	output means	Function: for outputting information stored at said location of said memory block in response to a third edge of said external clock signal.

	Governed by 35 U.S.C. s. 112 para. 6.	Corresponding Structure: output control (1338) and equivalents thereof.
'921-Claim 17	output means	Function: outputs said information in response to said output enable signal.

	Governed by	Corresponding Structure: output control (1338) and equivalents thereof.

	35 U.S.C. s. 112 para. 6.	
'921-Claim 29	output means	Function: for outputting information stored at said location of said memory block in response to an output enable signal.
	Governed by 35 U.S.C. s. 112 para. 6.	Corresponding Structure: output control (1338) and equivalents thereof.
'921-Claim 31	output means	Function: for outputting information from said memory block.
	Governed by 35 U.S.C. s. 112 para. 6.	Corresponding Structure: output control (1338) and equivalents thereof.
'921-Claim 35	output means	Function: for outputting information from said memory block.
	Governed by 35 U.S.C. s. 112 para. 6.	Corresponding Structure: output control (1338) and equivalents thereof.
'921-Claim 36	output means	Function: for outputting said information read from said memory to a data bus in response to an output enable signal.
	Governed by 35 U.S.C. s. 112 para. 6.	Corresponding Structure: output control (1338) and equivalents thereof.
'921-Claim 59	output means	Function: for outputting information stored at said location of said memory block in response to a third edge of said external clock signal.
	Governed by 35 U.S.C. s. 112 para. 6.	Corresponding Structure: output control (1338) and equivalents thereof.
'680-Claim 36	output means	Function: for outputting to said bus, information stored at said location of said memory block in response to a third edge of said clock signal.
	Governed by 35 U.S.C. s. 112 para. 6.	Corresponding Structure: output control (1338) and equivalents thereof.
'921-	write mask	Function: for generating a write prohibition signal for prohibiting writing

Claim 12	means	information to at least one bit location in said memory block based on said mask information.
	Governed by 35 U.S.C. s. 112 para. 6.	Corresponding structure: write mask (1336) and equivalents thereof.
'921-Claim 7	data input means	Function: for receiving data and for holding said data in response to an edge of said external clock signal.
	Governed by 35 U.S.C. s. 112 para. 6.	Corresponding structure: data register (1340) and equivalents thereof.
'921-Claim 18	data input means	Function: for receiving data, said data input means providing said data as an output in response to an edge of said external clock signal.
	Governed by 35 U.S.C. s. 112 para. 6.	Corresponding structure: data register (1340) and equivalents thereof.
'921-Claim 19	data input means	Function: provides said data in response to said data enable signal.
	Governed by 35 U.S.C. s. 112 para. 6.	Corresponding structure: data register (1340) and equivalents thereof.
'921-Claim 24	data input means	Function: for receiving data, said data input means providing said data as an output in response to a data enable signal.
	Governed by 35 U.S.C. s. 112 para. 6.	Corresponding structure: data register (1340) and equivalents thereof.
'921-Claim 33	data input means	Function: for receiving data.
	Governed by 35 U.S.C. s. 112 para. 6.	Corresponding structure: data register (1340) and equivalents thereof.
'921-Claim 35	data input means	Function: for receiving data.

	Governed by 35 U.S.C. s. 112 para. 6.	Corresponding structure: data register (1340) and equivalents thereof.
'921-Claim 61	data input means	Function: for receiving data, said data input means providing said data as an output in response to a third edge of said external clock signal.

	Governed by 35 U.S.C. s. 112 para. 6.	Corresponding structure: data register (1340) and equivalents thereof.
'921-Claim 36	[outputting] means	Function: for outputting said information read from said memory to a data bus in response to an output enable signal.

	Governed by 35 U.S.C. s. 112 para. 6.	Corresponding structure: output control (1338) and equivalents thereof.
'921-Claim 12	mask information input means	Function: for receiving mask information, said mask information input means providing said mask information as an output in response to a third edge of said external clock signal.

	Governed by 35 U.S.C. s. 112 para. 6.	Corresponding Structure: data register 1340.
'921-Claim 36	[reading] means	Function: for reading information stored at said addressable memory location

	Governed by 35 U.S.C. s. 112 para. 6.	Corresponding Structure: block decode 1330.
'921-Claim 5	control means	Function: for receiving said external clock signal from said control bus and being further connected to said address means, said output means and said dynamic random access memory, said control means being responsive to the receipt of said external clock signal for controlling the operation of said address means, said output means, and said dynamic random access memory.

	Governed by 35 U.S.C. s. 112 para. 6.	Corresponding Structure: Random state machine (1366)
'921-Claim 8	control means	Function: for holding a first address of information stored in said dynamic random access memory in response to a first edge of said external clock signal and for holding a second address of said information stored in said dynamic random access memory in response to a second edge of said external clock signal, said first edge of said external clock sign b[sic] different from said second edge of said

external clock signal.

	Governed by 35 U.S.C. s. 112 para. 6.	Corresponding Structure: Random state machine (1366)
'921-Claim 17	control means	Function: for supplying a first enable signal and a second enable signal to said address input means in response to an external control input on an edge of said external clock signal, and for supplying an output enable signal to said output means in response to said external control input on an edge of said external clock signal, each of said first enable signal, said second enable signal and said output enable signal being synchronous with an edge of said external clock signal.

	Governed by 35 U.S.C. s. 112 para. 6.	Corresponding Structure: Random state machine (1366)
'921-Claim 19	control means	Function: for supplying a data enable signal to said data input means in response to an external control input on an edge of said external clock signal, and for supplying awrite enable signal to said write means in response to said external control input on an edge of said external clock signal, each of said data enable signal and said write enablesignal being synchronous with an edge of said external clock signal.

	Governed by 35 U.S.C. s. 112 para. 6.	Corresponding Structure: Random state machine (1366)
'921-Claim 23	control means	Function: for supplying said first enable signal and said second enable signal to said address input means in response to an external control input on an edge of saidexternal clock signal, and for supplying said output enable signal to said output means in response to said external control input on an edge of said external clock signal, each of said first enable signal, said second enable signal and said output enable signal being synchronous with an edge of said external clock signal.

	Governed by 35 U.S.C. s. 112 para. 6.	Corresponding Structure: Random state machine (1366)
'921-Claim 24	control means	Function: supplies said data enable signal to said data input means in response to said external control input on an edge of said external clock signal, and supplies said write enable signal to said write means in response to said external control input on an edge of said external clock signal, each of said data enable signal and said write enable signal being synchronous with an edge of said external clock signal.

	Governed by 35 U.S.C. s. 112 para. 6.	Corresponding Structure: Random state machine (1366)

'921-Claim 40	control means	Function: for receiving said external control input defining said operation mode through said second bus, and for controlling operations of said address input means, said access information input means and said access means in response to said external control input on an edge of said external clock signal.
	Governed by 35 U.S.C. s. 112 para. 6.	Corresponding Structure: Random state machine (1366)
'921-Claim 42	control means	Function: supplies a first enable signal and a second enable signal to said address input means in response to an external control input on an edge of said external clock signal, supplies an access information enable signal to said access information input means in response to said external control input on an edge of said external clock signal, supplies a write enable signal to said write means in response to said external control input on an edge of said external clock signal each of said first enable signal, said second enable signal, said access information enable signal and said write enable signal being synchronous with an edge of said external clock signal.
	Governed by 35 U.S.C. s. 112 para. 6.	Corresponding Structure: Random state machine (1366)
'921-Claim 53	control means	Function: for outputting an internal control signal defining a timing of an internal operation of said synchronous semiconductor memory in response to an external controlinput on an edge of said external clock signal; wherein said control means generates new state information in accordance with an external control input and state information output in response to a first edge of said external clock signal, and outputs a new internal control signal based on said new state information in response to a second edge of said external clock signal, said first edge of said external clock signal being different from said second edge of said external clock.
	Governed by 35 U.S.C. s. 112 para. 6.	Corresponding Structure: Random state machine (1366)
'921-Claim 55	control means	Function: generates further new state information in accordance with an external control input on a third edge of said external clock signal and said new state information, and outputs a further new internal control signal based on said further new state information in response to said third edge of said external, clock signal, said second edge of said external clock signal being different from said third edge of said external clock signal.
	Governed by 35 U.S.C. s. 112 para. 6.	Corresponding Structure: Random state machine (1366)
'921-Claim 68	control means	Function: for receiving a first external control input indicating one of a read mode and a write mode and a second external control input which is different from said first external control input, for generating said third enable signal based on said

first external control input and generating at least one of said first enable signal and said second enable signal based on said second external control input, and for supplying said third enable signal to said access means in response to an edge of said external clock signal and supplying at least one of said first enable signal and said second enable signal to said address input means in response to an edge of said external clock signal.

	Governed by 35 U.S.C. s. 112 para. 6.	Corresponding Structure: Random state machine (1366)
'921-Claim 71	control means	Function: for outputting an internal control signal defining a timing of an internal operation of said synchronous semiconductor memory in response to an external control input on an edge of said external clock signal; wherein said control means comprises a random state machine.

	Governed by 35 U.S.C. s. 112 para. 6.	Corresponding Structure: Random state machine (1366)
'921-Claim 75	control means	Function: for receiving a predetermined set of control signals provided from outside of said synchronous dynamic random access memory, for making a transition from a state to a next state in accordance with said predetermined set of control signals on respective edges of said external clock signal, and for outputting an internal control signal defining a timing of an internal operation of said synchronous dynamic random access memory based on the said next state.

	Governed by 35 U.S.C. s. 112 para. 6.	Corresponding Structure: Random state machine (1366)
'680-Claim 37	control means	Function: for supplying a first enable signal and a second enable signal to said address input means in response to said control input on an edge of said clock signal, and for supplying an output enable signal to said output means in response to said control input on an edge of said clock signal, each of said first enable signal, said second enable signal and said output enable signal being synchronous with an edge of said clock signal.

	Governed by 35 U.S.C. s. 112 para. 6.	Corresponding Structure: Random state machine (1366)
'680-Claim 39	control means	Function: for supplying a data enable signal to said data input means in response to said control input on an edge of said clock signal, and for supplying a write enable signal to said write means in response to said control input on an edge of said clock signal, each of said data enable signal and said write enable signal being synchronous with an edge of said clock signal.

	Governed by	Corresponding Structure: Random state machine (1366)

	35 U.S.C. s. 112 para. 6.	
'680-Claim 42	control means	Function: for receiving said control input through said second bus, and for controlling operations of said address input means, said access information input means and said access means in response to said control input on an edge of said clock signal.
	Governed by 35 U.S.C. s. 112 para. 6.	Corresponding Structure: Random state machine (1366)
'680-Claim 45	control means	Function: for outputting an internal control signal defining a timing of an internal operation of said synchronous dynamic random access memory based on a control input on an edge of said clock signal; wherein said control means generates new state information in accordance with a control input and state information output in response to a third edge of said clock signal, and outputs a new internal control signal based on said new state information in response to a fourth edge of said clock signal, said third edge of said clock signal being different from said fourth edge of said clock signal.
	Governed by 35 U.S.C. s. 112 para. 6.	Corresponding Structure: Random state machine (1366)
'680-Claim 51	control means	Function: for receiving a predetermined set of control signals provided from outside of said memory, for transitioning from one state to at least one next state in accordance with said predetermined set of control signals on respective edges of said clock signal, and for outputting internal control signals defining timings of internal operations of said memory based on the at least one next state.
	Governed by 35 U.S.C. s. 112 para. 6.	Corresponding Structure: Random state machine (1366)
'921-Claim 26	[next state determining] means	Function: for determining a next state in response to a current state and said external control input on an edge of said external clock signal.
	Governed by 35 U.S.C. s. 112 para. 6.	Corresponding Structure: random state machine 1366.
'921-Claim 27	[next state determining] means	Function: for determining a next state in response to a current state and said external control input on an edge of said external clock signal.
	Governed by 35 U.S.C. s. 112 para. 6.	Corresponding Structure: random state machine 1366.

'921-Claim 26	[producing] means	Function: for producing said first enable signal, said second enable signal, said output enable signal, said data enable signal and said write enable signal as a function of said next state.
	Governed by 35 U.S.C. s. 112 para. 6.	Corresponding Structure: state machine 1366.
'921-Claim 27	[producing] means	Function: for producing said first enable signal, said second enable signal and said output enable signal as a function of said next state.
	Governed by 35 U.S.C. s. 112 para. 6.	Corresponding Structure: state machine 1366.

MEI's U.S. Reissue Patent No. 35,921 & U.S. Reissue Patent No. 35,680 DISPUTED CONSTRUCTIONS

Claim(s)	Term	Court's Construction
'921-Claims 5-12, 16-20, 23, 24, 26, 28, 31, 33, 35, 36, 38, 40-42, 48-50, 53-55, 59, 61, 65, 68, 69, 71, 72 and 75	external clock signal	A single timing signal from outside of a device.
'680-Claims 35-39, 42, 45, 48, 49, and 51	clock signal	A single timing signal.
'921-Claims 40 and 42	access information	Information that specifies a memory access.
'680-Claim 42		
'921-Claim 40	access information defining a specification of said operation mode.	Information defining a specification for an operation mode.
'680-Claim 42		
'921-Claim 40	access information defining a specification of said operation mode in combination with said external control input defining said operation specifics of the operation mode.	Information defining a specification for an operation mode, which, together with external control input, defines the mode.
'921-Claim 66	output means	Function: sequentially outputting a plurality of data which belong to separately addressable locations in said memory blocks at substantially a same interval, said plurality of data including data stored at a location in said memory blocks corresponding to said first address

		and said second address provided by said address input means. [Agreed]
	Governed by 35 U.S.C. s. 112 para. 6.	Corresponding Structure: Dynamic latch 1304, serial data port 1306, and output control 1338.
'680-Claim 47	output means	Function: sequentially outputting a plurality of data which belong to separately addressable locations in said individual memory blocks at substantially a same interval, said plurality of data including data stored at a location in said memory block corresponding to said first address and said second address. [Agreed.]
	Governed by 35 U.S.C. s. 112 para. 6.	Corresponding Structure: Dynamic latch 1304, serial data port 1306, and output control 1338.
'921-Claim 10	access means	Function: for accessing a location in said memory block corresponding to said first address and said second address provided by said address input means. [Agreed.]
	Governed by 35 U.S.C. s. 112 para. 6.	Corresponding Structure: output control 1338, write mask 1336, and drawing rule 1354.
'921-Claim 23	access means	Function: for accessing a location in said memory block corresponding to said first address and said second address provided by said address input means. [Agreed.]
	Governed by 35 U.S.C. s. 112 para. 6.	Corresponding Structure: output control 1338, write mask 1336, and drawing rule 1354.
'921-Claim 40	access means	Function: for accessing a location in said memory block corresponding to said first address and said second address provided by said address input means in accordance with said operation mode. [Agreed.]
	Governed by 35 U.S.C. s. 112 para. 6.	Corresponding Structure: output control 1338, write mask 1336, and drawing rule 1354.
'921-Claim 53	access means	Function: for accessing a location in said memory block corresponding to said first address and said second address provided by said address input means. [Agreed.]
	Governed by 35 U.S.C. s. 112 para. 6.	Corresponding Structure: output control 1338, write mask 1336, and drawing rule 1354.
'921-Claim 68	access means	Function: for accessing a location in said memory block corresponding to said first address and said second address provided by said address input means in response to a third enable signal. [Agreed.]
	Governed by 35 U.S.C. s. 112	Corresponding Structure: output control 1338, write mask

	para. 6.	1336, and drawing rule 1354.
'921-Claim 71	access means	Function: for accessing a location in said memory block corresponding to said first address and said second address provided by said address input means. [Agreed.]
	Governed by 35 U.S.C. s. 112 para. 6.	Corresponding Structure: output control 1338, write mask 1336, and drawing rule 1354.
'921-Claim 75	access means	Function: for accessing a location in said memory block corresponding to said first address and said second address provided by said address input means. [Agreed.]
	Governed by 35 U.S.C. s. 112 para. 6.	Corresponding Structure: output control 1338, write mask 1336, and drawing rule 1354.
'680-Claim 35	access means	Function: for accessing a location in said memory block corresponding to said first address and said second address held by said address input means. [Agreed.]
	Governed by 35 U.S.C. s. 112 para. 6.	Corresponding Structure: output control 1338, write mask 1336, and drawing rule 1354.
'921-Claim 7	writing means/write means/means for writing	Function: for writing said held data to said memory. [Agreed.]
	Governed by 35 U.S.C. s. 112 para. 6.	Corresponding Structure: write mask 1336 and drawing rule 1354.
'921-Claim 12	writing means/write means/means for writing	Function: for writing said information to said memory block in accordance with said write prohibition signal within a region in said memory block corresponding to said first address and said second address provided by said address input means. [Agreed.]
	Governed by 35 U.S.C. s. 112 para. 6.	Corresponding Structure: write mask 1336 and drawing rule 1354.
'921-Claim 16	writing means/write means/means for writing	Function: writes said information to said memory block in response to a fourth edge of said external clock signal. [Agreed.]
	Governed by 35 U.S.C. s. 112 para. 6.	Corresponding Structure: write mask 1336 and drawing rule 1354.
'921-Claim 18	writing means/write means/means for writing	Function: for writing said data to said memory block at a location addressed by said first address and said second address in response to an edge of said external clock signal. [Agreed.]
	Governed by 35 U.S.C. s. 112	Corresponding Structure: write mask 1336 and drawing

	para. 6.	rule 1354.
'921-Claim 24	writing means/write means/means for writing	Function: for writing said data to said memory block at a location addressed by said first address and said second address in response to a write enable signal. [Agreed.]
	Governed by 35 U.S.C. s. 112 para. 6.	Corresponding Structure: write mask 1336 and drawing rule 1354.
'921-Claim 33	writing means/write means/means for writing	Function: for writing said data into said memory block. [Agreed.]
	Governed by 35 U.S.C. s. 112 para. 6.	Corresponding Structure: write mask 1336 and drawing rule 1354.
'921-Claim 35	writing means/write means/means for writing	Function: for writing said data into said memory block. [Agreed.]
	Governed by 35 U.S.C. s. 112 para. 6.	Corresponding Structure: write mask 1336 and drawing rule 1354.
'921-Claim 38	writing means/write means/means for writing	Function: for writing said data loaded in said data buffer to said addressable memory location represented by said address loaded in said address buffer. [Agreed.]
	Governed by 35 U.S.C. s. 112 para. 6.	Corresponding Structure: write mask 1336 and drawing rule 1354.
'921-Claim 41	writing means/write means/means for writing	Function: for writing information to said memory block at a location corresponding to said first and said second address in response to a fourth edge of said external clock signal. [Agreed.]
	Governed by 35 U.S.C. s. 112 para. 6.	Corresponding Structure: write mask 1336 and drawing rule 1354.
'921-Claim 42	writing means/write means/means for writing	Function: writes said information in response to said write enable signal. [Agreed.]
	Governed by 35 U.S.C. s. 112 para. 6.	Corresponding Structure: write mask 1336 and drawing rule 1354.
'921-Claim 61	writing means/write means/means for writing	Function: for writing said data to said memory block at a location corresponding to said first and said second address in response to a fourth edge of said external clock signal. [Agreed.]
	Governed by 35 U.S.C. s. 112 para. 6.	Corresponding Structure: write mask 1336 and drawing rule 1354.
'680-Claim 38	writing means/write means/means for writing	Function: for writing said data to said memory block at said location corresponding to said first address and said

		second address in response to a fourth edge of said clock signal. [Agreed.]
	Governed by 35 U.S.C. s. 112 para. 6.	Corresponding Structure: write mask 1336 and drawing rule 1354.
'921-Claim 40	access information input means	Function: for receiving access information through said first bus. [Agreed.]
	Governed by 35 U.S.C. s. 112 para. 6.	Corresponding Structure: address register 1320 and data register 1340.
'921-Claim 42	access information input means	Function: provides said access information in response to said access information enable signal. [Agreed.]
	Governed by 35 U.S.C. s. 112 para. 6.	Corresponding Structure: address register 1320 and data register 1340.
'680-Claim 42	access information input means	Function: for receiving said access information through said first bus and providing said access information as an output in response to said third edge of said clock signal. [Agreed.]
	Governed by 35 U.S.C. s. 112 para. 6.	Corresponding Structure: address register 1320 and data register 1340.
'921-Claim 73	decoding means	Function: for decoding said new state so as to output said internal control signal. [Agreed.]
	Governed by 35 U.S.C. s. 112 para. 6.	Corresponding Structure: state machine 1366.
'680-Claim 50	decoding means	Function: for decoding said new state so as to output said internal control signal. [Agreed.]
	Governed by 35 U.S.C. s. 112 para. 6.	Corresponding Structure: state machine 1366.
'680-Claim 35	address providing means	Function: for providing a first address and a second address on said bus, said first address being valid on said bus on a first edge of a clock signal and said second address being valid on said bus on a second edge of said clock signal, said first edge of said clock signal being different from said second edge of said clock signal. [Agreed.]
	Governed by 35 U.S.C. s. 112 para. 6.	Corresponding Structure: a processor (CPU), a bus 170, and an interface circuit 160.
'680-Claim 38	data providing means	Function: for providing data on said bus which is valid on a third edge of said clock signal. [Agreed.]

	Governed by 35 U.S.C. s. 112 para. 6.	Corresponding Structure: a processor (CPU), a bus 170, and an interface circuit 160.
'680-Claim 37	control input providing means	Function: for providing on said bus a control input, said control input being valid on an edge of said clock signal. [Agreed.]

	Governed by 35 U.S.C. s. 112 para. 6.	Corresponding Structure: a processor (CPU), a bus 170, and an interface circuit 160.
'680-Claim 39	control input providing means	Function: for providing on said bus a control input, said control input being valid on an edge of said clock signal. [Agreed.]

	Governed by 35 U.S.C. s. 112 para. 6.	Corresponding Structure: a processor (CPU), a bus 170, and an interface circuit 160.
'680-Claim 42	control input providing means	Function: for providing said control input on said second bus ... and said control input being valid on said second bus on an edge of said clock signal. [Agreed.]

	Governed by 35 U.S.C. s. 112 para. 6.	Corresponding Structure: a processor (CPU), a bus 170, and an interface circuit 160.
'680-Claim 45	control input providing means	Function: for providing a control input on said bus, said control input being valid on said bus on an edge of said clock signal. [Agreed.]

	Governed by 35 U.S.C. s. 112 para. 6.	Corresponding Structure: a processor (CPU), a bus 170, and an interface circuit 160.
'680-Claim 48	control input providing means	Function: for providing a control input on said bus, said control input being valid on said bus on an edge of said clock signal. [Agreed.]

	Governed by 35 U.S.C. s. 112 para. 6.	Corresponding Structure: a processor (CPU), a bus 170, and an interface circuit 160.
'680-Claim 42	access information providing means	Function: for providing access information defining a specification of said operation mode on said first bus, said access information being valid on said first bus on a third edge of said clock signal. [Agreed.]
	Governed by 35 U.S.C. s. 112 para. 6.	Corresponding Structure: a processor (CPU), a bus 170, and an interface circuit 160.

MEI's U.S. Patent No. 5,189,588 AGREED CONSTRUCTIONS		
Claim(s)	Term	Agreed Construction
2	longitudinal direction	Along the length.
1 and 2	diode	A device that allows current to flow from the

		anode to the cathode and inhibits current flow in the opposite direction.
2	disposed sporadically	This term requires no express construction because it can be understood from its plain and ordinary meaning.
2	a means for respectively connecting said plural signal input/output pads and said first and second power supply wires to the internal circuit Governed by 35 U.S.C. s. 112 para. 6.	Function: for respectively connecting said plural signal input/output pads and said first and second power supply wires to the internal circuit. Corresponding structure: wires as illustrated in figures 1, 2, 3, 5, 6, 7, 8, 9, 10, 11, 12 and equivalents thereof.

MEI's U.S. Patent No. 5,189,588 DISPUTED CONSTRUCTIONS		
Claim(s)	Term	Court's Construction
1	protective MOS transistor	A MOS transistor that provides a discharge path for current to flow from the first power supply terminal to the second power supply terminal when activated by a voltage on the drain that exceeds a predetermined level.
2	peripheral region of the semiconductor chip	Region outside the area of the semiconductor chip in which the internal circuit is formed.
2	plural protective transistors	Multiple transistors which provide a discharge path for current to flow between the first power supply wire and the second power supply wire when activated.
3	protective transistor	A transistor which provides a discharge path for current to flow between the first power supply wire and the second power supply wire when activated.
1 and 2	internal circuit	The internal circuit which is protected by the surge protection apparatus.

MEI's U.S. Patent No. 6,677,195 AGREED CONSTRUCTIONS		
Claim(s)	Term	Agreed Construction
1	connected to	In direct contact with.
5, 6, 8, 9	main conducting metal layer	A metal layer which conducts a substantial portion of the current.
1	contact hole	A vertical hole that allows electrical contact.
1	fuse portion which is configured by a metal wiring layer	A portion of the metal wiring layer that can be disconnected to cause an open circuit.
1, 2, 5-10, 17-21	metal wiring layer	This term requires no express construction because it can be understood from its plain and ordinary meaning.

MEI's U.S. Patent No. 6,677,195 DISPUTED CONSTRUCTIONS		
Claim(s)	Term	Court's Construction
1, 2, 7 and 10	plug electrode	A metal conductor formed in a contact hole, which connects two layers.
1, 2, 5-10, 17-21	formed on said layer insulating film	No construction necessary.

2	formed in a plural number	Two or more plug electrodes are formed.
2	plug electrodes are connected respectively to both sides which are positioned across a part of said fuse portion where cutting off is to be performed	At least one plug electrode connected to the fuse portion on each side of the region where the fuse may be cut.