United States District Court,
N.D. California.

**MATSUSHITA ELECTRIC INDUSTRIAL CO., LTD,**
Plaintiff.
v.
**MEDIATEK, INC., et al,**
Defendants.
**Mediatek, Inc,**
Counterclaimant.
v.
**Matsushita Electric Industrial Co., Ltd., et al,**
Counterclaim Defendants.

No. C 05-3148 MMC

**Nov. 9, 2006.**

Anthony W. Shaw, Steven A. Bowers, Dewey Ballantine LLP, Washington, DC, Lisa B. Deutsch, Jason D. Clark, Dewey Ballantine LLP, New York, NY, Tyler Woods, Attorney at Law, Irvine, CA, Plaintiff.

Kevin P.B. Johnson, Quinn Emanuel Urquhart Oliver & Hedges LLP, Redwood Shores, CA, Adrian M. Pruetz, Benjamin Singer, Eugene Chen, Quinn Emanuel Urquhart Oliver & Hedges LLP, Los Angeles, CA, Eric Hui-Chieh Huang, Quinn Emanuel Urquhart Oliver & Hedges LLP, New York, NY, for Defendants.

Andrew N. Thomases, Michelle Wai Yang, Dechert LLP, Bijal Vijay Vakil, Shamita D. Etienne, James E. Glore, Jennifer Yokoyama, McDermott Will & Emery LLP, Palo Alto, CA, Minn Chung, Morrison & Foerster LLP, San Francisco, CA, Jeffrey L. Kessler, Aldo A. Badini, Jack Q. Lever, Michelle Lo, Jason D. Clark, Dewey Ballantine LLP, New York, NY, Bryon Wasserman, Washington, DC, David M. Stein, McDermott Will & Emery, Irvine, CA, Mark Malin, Dewey Ballantine LLP, East Palo Alto, CA, for Plaintiff and Counterclaim Defendants.

## ORDER CONSTRUING CLAIMS

MAXINE M. CHESNEY**, District Judge.**

Before the Court is the parties' dispute regarding the proper construction of ten terms in four patents. Plaintiff/counterclaim defendant Matsushita Electric Industrial Co., Ltd. and counterclaim defendant Panasonic Corporation of North America (collectively, "Matsushita") have jointly submitted briefs and evidence in support of their positions on the disputed terms, and defendant/counterclaimant Mediatek Inc., defendant Oppo Digital, Inc. and defendant MSI Computer Corp. (collectively, "Mediatek") have jointly submitted briefs and evidence in support of their positions. The matter came on regularly for hearing on July 24, 2006. Jeffrey Kessler of Dewey Ballantine LLP and Fay Morisseau of McDermott Will & Emery LLP

appeared on behalf of Matsushita. Kevin Johnson and Eric Huang of Quinn Emanuel Urquhart Oliver & Hedges LLP appeared on behalf of Mediatek. Having considered the papers submitted and the arguments of counsel, the Court rules as follows.

**A. Disputed Terms in** U.S. Patent 5,970,238 ("'238 Patent")

**1. Second Planarizing Pattern (Claims 22 and 23)**

Matsushita argues "second planarizing pattern" should be construed as "a pattern for making flatter in shape." Mediatek argues "second planarizing pattern" should be construed as "a pattern formed of at least one indiscrete figure formed in the (first) wiring layer and in an area other than the vicinity of any wiring pattern." FN1

FN1. The parties' respective positions as set forth herein are, unless otherwise indicated, taken from their briefs. ( *See, e.g.,* Amended Joint Claim Construction and Prehearing Statement, filed May 8, 2006.)

The Court finds, for the reasons stated by Matsushita, "second planarizing pattern" is properly construed as "a second pattern for making flatter in shape."

**2. Larger Than Said Simple Geometric Figure (Claims 22 and 23)**

Matsushita argues "larger than said simple geometric figure" should be construed as "having a greater area than said simple geometric figure." Mediatek argues "larger than said simple geometric figure" should be construed as "having a greater area than the area of the simple geometric figure of the first planarizing pattern so that the number of figures and the amount of data in the planarizing patterns is reduced."

The Court finds, for the reasons stated by Matsushita, "larger than said simple geometric figure" is properly construed as "having a greater area than the area of the simple geometric figure of the first planarizing pattern."

**B. Disputed Terms in** U.S. Patent 5,548,249 ("'249 Patent")

**1. Phase Comparison Means (Claims 1 and 2)**

Matsushita argues that "phase comparison means" is not subject to means-plusfunction construction, and should be construed as "a phase comparator." Mediatek argues that "phase comparison means" is subject to means-plus-function construction, and that the structure corresponding to the function recited in Claims 1 and 2 is a "phase comparator," identified in Figure 1 of the '249 Patent as "11," and equivalents thereof.

The Court finds, for the reasons stated by Mediatek, that "phase comparison means" is subject to means-plus-function construction, and that the structure corresponding to the function "outputting a phase difference signal indicating a phase difference between the first signal and the second signal" is a "phase comparator," identified in Figure 1 of the '249 Patent as "11," and equivalents thereof.

**2. Detection Means (Claim 2)**

Matsushita argues that "detection means" is not subject to means-plus function construction, and should be

construed as "a detector." Alternatively, Matsushita argues that, if the term is subject to means-plus function construction, the structure corresponding to the function recited in Claim 2 is the "detection circuit" identified in the specification. Mediatek argues that "detection means" is subject to means-plus function construction and that the specification does not sufficiently disclose any structure corresponding to the function recited in Claim 2.

The Court finds, for the reasons stated by Mediatek, that "detection means" is subject to means-plus function construction. The Court further finds, for the reasons stated by Matsushita, that the structure corresponding to the function "outputting a reset signal in response to a predetermined condition" is the "detection circuit" identified in the specification, specifically, a "detection circuit" that sets a "reset signal [ ] at a low level only when it detects a predetermined condition," which predetermined condition "includes a condition where a clock having a frequency one-hundredth or less of the frequency of the base clock (for example, 25 kHz) is input into the PPL circuit [ ] and a condition where all function blocks in a semiconductor device do not need a clock," see 249 Patent col. 10 ll. 39-47, and equivalents thereof. *See, e.g.,* Linear Tech. Corp. v. Impala Linear Corp., 379 F.3d 1311, 1320 (Fed.Cir.2004) (holding that because "circuit" is "structure-connoting term," where specification identifies "circuit" by "language reciting [circuit's] objectives or operations," such language constitutes sufficient disclosure of structure to person of ordinary skill in art).FN2

FN2. The Court provides this citation, as it was not referenced in the briefing submitted by the parties.

**C. Disputed Claims in** U.S. Patent 6,728,475 ("'475 Patent")

**1. Maintaining a Currently Displayed Frame (Claim 1)/Maintain A Currently Displayed Frame (Claim 8)**

Matsushita argues "maintaining a currently displayed frame"/"maintain a currently displayed frame" should be construed as "continuing to display a frame being displayed as this step starts," or, alternatively, "continuing to display a frame displayed after receipt of the manually inputted signal." Mediatek argues "maintaining a currently displayed frame"/ "maintain a currently displayed frame" should be construed as "continuing to display the same picture frame that is being displayed at the time the manually inputted signal is detected."

The Court finds, for the reasons stated by Mediatek, that "maintaining a currently displayed frame"/"maintain a currently displayed frame" is properly construed as "continuing to display the same picture frame that is being displayed when the manually inputted signal is detected." FN3

FN3. At the claim construction hearing, Mediatek suggested the substitution of "when" for "at the time" to alleviate Matsushita's concerns that Mediatek's initial proposed construction would require simultaneity. This modification is supported by the specification. *See, e.g.,* '475 Patent, col. 10, ll. 60-66 ("[I]n the first embodiment, passing data through to the input buffer memory 102 is inhibited *when change of program is detected,* and simultaneously all the data in the input buffer memory 102 is erased while *the display picture deciding means 106 is controlled to maintain the display picture at this time*.") (emphasis added).

**2. Nullifying Decoded Data (Claim 1)/Nullify Decoded Data (Claim 8)**

Matsushita argues "nullifying decoded data"/"nullify decoded data" should be construed as "rendering decoded data null as data." Mediatek argues "nullifying decoded data"/"nullify decoded data" should be construed as "eliminating data from frame buffer memory by replacing it with a null value not used for display, and setting flags indicating that there is no data in the corresponding memory to be displayed."

The Court finds, for the reasons stated by Matsushita, that "nullifying decoded data"/ "nullify decoded data" is properly construed as "rendering decoded data null as data rather than skipping data yet to be decoded." FN4

FN4. The additional clarifying language is derived from the prosecution history, wherein Matsushita distinguished the instant invention over prior art. (See Huang Decl. Ex. E at MTK1109352) ("While [the prior art reference] skips data to be decoded ... to nullify the same when a reproduction speed is varied, it does not delete a decoded memory data utilized for a display ....") (emphasis in original).

**3. Decoded Data Which Has Not Been Displayed (Claims 1 and 8)**

Matsushita argues "decoded data which has not been displayed" should be construed as "data that has been decoded, corresponding to pictures that have not been displayed." Mediatek argues "decoded data which has not been displayed" should be construed as "a decoded forward predictive picture (P picture frame) that has not been displayed." FN5

FN5. At the claim construction hearing, Mediatek expanded its proposed construction to include any "reference" frame and argued its proposed construction should not be "misunderstood" to be limited to only such frames but rather to require at least one such frame.

The Court finds, for the reasons stated by Matsushita, that "decoded data which has not been displayed" is properly construed as "data that has been decoded, corresponding to pictures that have not been displayed."

**D. Disputed Terms in** U.S. Patent 5,970,031 ("'031 Patent")

**1. Disabling Said EFM Decoder (Claims 1 and 6)**FN6

FN6. Claim 1 refers to an "EFM encoder," *see* 031 Patent, col. 9 ll. 1, as does Claim 6, *see* id., col. 10 ll. 22. Mediatek asserts, and Matsushita does not argue to the contrary, that those references are typographical errors.

Mediatek argues "disabling said EFM decoder" should be construed as "stopping the flow of EFM decoded audio data." Matsushita argues "disabling said EFM decoder" should be construed as "deactivating the EFM decoder."

The Court finds, for the reasons stated by Mediatek, that "disabling said EFM decoder" is properly construed as "stopping the flow of EFM decoded audio data." FN7

FN7. Although the term "EFM decoding process," as set forth in Claims 1 and 6, is not one of the ten disputed terms before the Court, it appears Mediatek is arguing "decoding" is used only with reference to

audio data, ( *see* Mediatek's Reply, filed June 14, 2006, at 1:25-27), while Matsushita is arguing "decoding" refers to both audio data and subcode, ( *see* Matsushita's Responsive Brief, filed June 5, 2006, at 5:6-11). The Court is not persuaded by Matsushita's argument on this point. In discussing the prior art, the specification states that an incoming signal "undergoes various data processing stages" and distinguishes the stages of "decoding" and "subcode acquisition." ( *See* '031 Patent, col. 2, ll. 20-24.) In discussing how incoming signals are treated by the instant invention, the specification similarly distinguishes between the "decoding" of audio data and the "processing" of subcode. ( *See* id., col. 6, ll. 33-41.)

**2. Enabling Said EFM Decoder (Claims 1 and 6)**

Mediatek argues "enabling said EFM decoder" should be construed as "restarting the flow of EFM decoded audio data." Matsushita argues "enabling said EMF encoder" should be construed as "activating the EFM decoder."

The Court finds, for the reasons stated by Mediatek, that "enabling said EFM decoder" is properly construed as "restarting the flow of EFM decoded audio data."

**3. Resetting Said CIRC Decoder (Claims 1 and 6)**

Mediatek argues "resetting said CIRC decoder" should be construed as "restoring the CIRC decoder to a state at which it is ready to receive a data frame." Matsushita argues "resetting said CIRC decoder" should be construed as "restoring the CIRC decoder to a prescribed state at or before the occurrence of the defocusing or mistracking event."

The Court finds, for the reasons stated by Mediatek, that "resetting said CIRC decoder" is properly construed as "restoring the CIRC decoder to a state at which it is ready to receive a data frame."

**E. Undisputed Terms**

The Court adopts the following constructions, jointly submitted by the parties. ( *See* Amended Joint Claim Construction and Prehearing Statement, filed May 8, 2006, Ex. A.)

1. The terms "wiring pattern" ('238 Patent, Claim 22) and "first wiring pattern" ('238 Patent, Claim 23) are properly construed as "conductive pathways formed in a wiring layer on a semiconductor substrate."

2. The term "input shutoff means" ('249 Patent, Claims 1 and 2) is subject to means-plus-function construction. The function performed by the "input shutoff means" is "receiving a base clock and reference clock and outputting a first signal and second signal in response to a reset signal, so that when the reset signal is in a first level, the input shutoff control means outputs the base clock to the phase comparison means as the first signal and outputs the reference clock to the phase comparison means as the second signal, and when the reset signal is in a second level different from the first level, the input shutoff control means outputs two signals to the phase comparison means as the first signal and the second signal, the phase difference between the two signals being substantially zero." The structure corresponding to such function is an "input shutoff control circuit," identified in Figure 1 of the '249 Patent as "14," and equivalents thereof.

3. The term "voltage fixing control means" ('249 Patent, Claims 1 and 2) is subject to means-plus-function construction. The function performed by the "voltage fixing control means" is "controlling a voltage of the

phase difference signal in response to the reset signal, so that when the reset signal is in a first level, the voltage fixing control means holds the voltage of the phase difference signal, and when the reset signal is in a second level different from the first level, the voltage fixing control means fix[es] FN8 the voltage of the phase difference signal to a predetermined voltage at which the voltage control oscillation means does not oscillate." The structure corresponding to such function is a "voltage fixing control circuit," identified in Figure 1 of the ' 249 Patent as "15," and equivalents thereof.

FN8. *See* '249 Patent, col. 10, ll. 20-24.

4. The term "discard the data frame" ('031 Patent, Claims 1 and 6) is construed as "to abandon the current data frame."

5. The term "when the next subcode appears" ('031 Patent, Claims 1 and 6) is construed as "when the next subcode is received by the EFM decoder."

**IT IS SO ORDERED.**

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