United States District Court,
N.D. California.

TOSHIBA CORPORATION,
Plaintiff.
v.
HYNIX SEMICONDUCTOR INC, et al,
Defendants.
And Related Counterclaim,
And Related Counterclaims.

No. C-04-4708 VRW

Aug. 21, 2006.

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Ronald Loh-Hwa Yin, Alan A. Limbach, Erin Overom Dungan, Mark Fowler, Vincent Lam, DLA Piper Rudnick Gray Cary U.S. LLP, East Palo Alto, CA, for Plaintiff.

ORDER

VAUGHN R. WALKER**, Chief District Judge.**

The parties have asked the court to construe a total of 16 terms in four patents owned by Toshiba Corporation: United States Patent Nos 5,144,579 ("the '579 patent"); 5,880,994 ("the '994 patent); 6,342,715 ("the '715 patent") and 6,424,588 ("the '588 patent). The court vacated a claim construction hearing originally scheduled for July 6, 2006, after determining that a hearing was unnecessary here. Doc # 39 of 05-4100. Based on the parties' submissions to the court, the court issues the following claim construction order.

As the court writes principally for the parties, it will not discuss the details of the inventions or define terms well-known to those skilled in the art, except as is necessary to construe the patent claims. Nor will the court recapitulate the parties' agreed-upon constructions, which can be found in the final joint claim construction statement. Jt Cl Const (Doc # 32 of 05-4100), Exs A-D.

I

The construction of patent claims is a question of law to be determined by the court. Markman v. Westview Instruments, Inc, 517 U.S. 370 (1996). The goal of claim construction is "to interpret what the patentee meant by a particular term or phrase in a claim." Renishaw PLC v. Marposs SpA, 158 F3d 1243, 1249 (Fed

Cir1998). In doing so, the court looks first to the claim itself:

The claims of the patent provide the concise formal definition of the invention. They are the numbered paragraphs which "particularly [point] out and distinctly [claim] the subject matter which the applicant regards as his invention." 35 USC s. 112. It is to these wordings that one must look to determine whether there has been infringement. Courts can neither broaden nor narrow the claims to give the patentee something different than what he has set forth. No matter how great the temptations of fairness or policy making, courts do not rework claims. They only interpret them.

EI Du Pont de Nemours & Co v. Phillips Petroleum Co, 849 F.2d 1430, 1433 (Fed Cir1988).

"The claims define the scope of the right to exclude; the claim construction inquiry, therefore, begins and ends in all cases with the actual words of the claim." Renishaw, 158 F3d at 1248. "The words used in the claim are viewed through the viewing glass of a person skilled in the art." Brookhill-Wilk 1, LLC v. Intuitive Surgical, Inc, 326 F3d 1215, 1220 (Fed Cir2003) (citing Tegal Corp v. Tokyo Electron Am, Inc, 257 F3d 1331, 1342 (Fed Cir2001)). "Absent a special and particular definition created by the patent applicant, terms in a claim are to be given their ordinary and accustomed meaning." York Prods, Inc v. Central Tractor Farm & Family Ctr, 99 F3d 1568, 1572 (Fed Cir1996). The court may, if necessary, consult a variety of sources to determine the ordinary and customary meaning of a claim term, including "the words of the claims themselves, the remainder of the specification, the prosecution history, and extrinsic evidence concerning relevant scientific principles, the meaning of technical terms, and the state of the art." Innova/Pure Water, Inc v. Safari Water, 381 F3d 1111, 1116 (Fed Cir2004).

The court begins its construction of claim terms by consulting intrinsic evidence of the meaning of disputed claim terms, which includes the claims, the specification and the prosecution history (if in evidence). Lacks Industries, Inc v. McKechnie Vehicle Components USA, Inc, 322 F3d 1335, 1341 (Fed Cir2003) (citation omitted). "If upon examination of this intrinsic evidence the meaning of the claim language is sufficiently clear, resort to 'extrinsic' evidence * * * should not be necessary." Digital Biometrics, Inc, v. Identix, Inc, 149 F3d 1335, 1344 (Fed Cir1998). "[I]f after consideration of the intrinsic evidence, there remains doubt as to the exact meaning of the claim terms, consideration of extrinsic evidence may be necessary to determine the proper construction." *Id*. Although extrinsic evidence such as expert and inventor testimonies, dictionaries and learned treatises can shed useful light on the relevant art, extrinsic evidence is "less significant than the intrinsic record in determining the legally operative meaning of claim language." Phillips v. AWH Corp, 415 F3d 1303, 1317 (Fed Cir2005) (quoting C R Bard, Inc v. United States Surgical Corp, 388 F3d 858, 862 (Fed Cir2004)) (internal quotation marks omitted).

"[A] court may constrict the ordinary meaning of a claim term in at least one of four ways[:]" (1) "if the patentee acted as his own lexicographer and clearly set forth a definition of the disputed claim in either the specification or prosecution history;" (2) "if the intrinsic evidence shows that the patentee distinguished [the] term from prior art on the basis of a particular embodiment, expressly disclaimed subject matter, or described a particular embodiment as important to the invention;" (3) "if the term chosen by the patentee so deprives the claim of clarity as to require resort to the other intrinsic evidence for a definite meaning;" or (4) "if the patentee phrased the claim in step- or means-plus-function format," then "a claim term will cover nothing more than the corresponding structure or step disclosed in the specification, as well as equivalents thereto * * *." CCS Fitness, Inc v. Brunswick Corp, 288 F3d 1359, 1366-67 (Fed Cir2002) (internal citations and quotation marks omitted).

Limitations from the specification, such as from a preferred embodiment, cannot be read into the claims unless expressly intended by the patentee. Teleflex, Inc v. Ficosa North Am Corp, 299 F3d 1313, 1326 (Fed Cir2002) ("The claims must be read in view of the specification, but limitations from the specification are not to be read into the claims."). And "a construction that excludes a preferred embodiment 'is rarely, if ever, correct.' " C R Bard, 388 F3d at 865 (citing Vitronics Corp v. Conceptronic, Inc, 90 F3d 1576, 1583 (Fed Cir1996)).

With these legal principles in mind, the court now construes the disputed claim language in the patents.

II

The '579 patent

The '579 patent describes a structure and fabricating method of a semiconductor memory device whose size is reduced while retaining a sufficient capacitance for its capacitors. '579 patent at Abstract, 2:60-68. The parties dispute four terms in this patent, all of which appear in independent claim 1, which states in full (with the disputed terms underlined):

1. A semiconductor memory device comprising:

a MOSFET including a gate electrode and source and drain regions of a second electrical conductivity type impurity material formed in a surface of a semiconductor substrate of a first electrical conductivity type material;

a bit line connected to one of the source and drain regions of said MOSFET through a bit line contact hole made in *an insulating film covering the surface of said substrate on which the MOSFET is formed;* and

a capacitor including a storage node electeode [sic] formed over a region where said MOSFET is formed, a capacitor insulating film and a plate electrode sequentially formed on said storage node electrode layer to be connected to another of said source and drain regions through a storage node contact hole made in said insulating film,

wherein at least one of said storage node contact hole and bit line contact hole includes a first contact hole made in a *first inter-layer insulating film* formed over said gate electrode and a second contact hole made in a *second inter-layer insulating film* formed over *an electrically conductive layer embedded in said first contact hole up to a level higher than the gate electrode such as to be contacted with said electrically conductive layer*.

The court examines the disputed terms in the order they appear in the claim.

1. "an insulating film covering the surface of said substrate on which the MOSFET is formed"

Toshiba contends that this term does not need construction, but if construed, it means "a non-conducting film that is over a portion of the surface of a substrate on which the MOSFET is formed." Jt Cl Const, Ex A at 1. Hynix instead proposes a construction of "an insulating film that spreads over and is in contact with the entire surface of the semiconductor substrate in which source and drain regions are formed." Id.

There appear to be three points of disagreement between the parties on this term: (1) Can the film cover just

a portion of the "surface of said substrate" or must the film cover the entire surface? (2) Can the film merely be over the surface or must the film be in contact with the surface? (3) Should the term "surface of said substrate on which the MOSFET if formed" be left as is or should it be redefined as the "surface of the semiconductor substrate in which source and drain regions are formed?"

Regarding the first point, the court observes that the clause in which this term appears states in full: "a bit line connected to one of the source and drain regions of said MOSFET through a bit line contact hole made in *an insulating film covering the surface of said substrate on which the MOSFET is formed*." Based on this language, Toshiba contends, "[T]he insulating film cannot possibly cover the entire semiconductor substrate, as the insulating film must have contact holes in it that reach to the substrate." Doc # 26 of 05-4100 VRW (Toshiba Br) at 5. Hynix counters that "[c]laim 1 only requires that the insulating film be 'covering' the substrate *before* the contact holes are made in it." Doc # 33 of 05-4100 VRW (Hynix Rep) at 3 (emphasis in original).

In its submission to the court in support of its *Markman* presentation, Toshiba admitted that Hynix is factually correct on this point, Toshiba *Markman* Presentation at 5, but explained that claim 1 describes a finished product; hence, to say that the insulating film spreads over "the entire surface of the semiconductor substrate" is misleading. Toshiba Br at 4-5. But Toshiba's construction is also misleading because it suggests that even before the contact holes were made, the insulating film only covered a portion of the substrate surface.

Instead, the original claim language is superior to both parties' constructions. Without describing the scope of the insulating film's initial coverage of the substrate surface, the claim states that the insulating film's coverage decreases after the contact holes are made. To infer that, prior to making the contact holes, the insulating film covered either the entire surface or only a part of the surface would be impermissibly to read in a limitation from the specification. Teleflex, 299 F3d at 1326. Accordingly, the court declines to construe the term on this point.

Turning to the second issue, Hynix cites to various portions of the specification to argue, "[T]he term 'covering' is used repeatedly to refer to a film that is spread over and in contact with the entire surface of the structure." Doc # 29 of 05-4100 VRW (Hynix Br) at 5. But in every embodiment that Hynix cites, only the MOSFET's gate electrode is in contact with the insulating film, not the portions of the MOSFET within the semiconductor substrate (i e, the source and drain regions). See '579 patent at 6:29-31, FIG 1(b); 10:36-38, FIG 16(b); 14:10-13, FIG 25(a). Indeed, as Toshiba notes, "if the entire surface of the substrate (including the source and drain regions) were covered and in contact with the insulating film, then the source and drain could not connect to the bit line and storage node electrode as required by the claim." Doc # 30 of 05-4100 VRW (Toshiba Rep) at 2. Because Hynix's proposed construction on this point cannot be correct and because there is no indication that the phrase "insulating film covering the surface" is necessarily limited to the situation in which the film is in contact with the surface, the court declines to construe the term on this point.

Finally, Hynix proposes equating "surface of said substrate on which the MOSFET is formed" with "surface of the semiconductor substrate in which source and drain regions are formed." Even if this proposed construction correct, it appears unnecessary. The claim states that the memory device comprises "a MOSFET including a gate electrode and source and drain regions of a second electrical conductivity type impurity material formed in a surface of a semiconductor substrate." This description clearly indicates the MOSFET's location in relation to the semiconductor surface; hence, it is unnecessary to further define what

constitutes the "surface of [the] substrate on which the MOSFET is formed."

In sum, because the language for this term is both sufficiently clear and is in fact superior to the proposed constructions, the court declines to construe this term.

2. "first inter-layer insulating film" and "second inter-layer insulating film"

Because the underlying issues for these two terms are interrelated, the court construes them together. The principal dispute between the parties is whether these two "inter-layers" are parts of the same "insulating film" at issue in the previously-construed term. Toshiba argues, based on the claim language, "[b]ecause the bit line contact hole is made in the 'insulating film covering the surface of said substrate on which the MOSFET is formed,' and because that same bit line contact hole consists of first and second contact holes that are made in first and second inter-layer insulating films, the 'insulating film covering the surface of said substrate on which the MOSFET is formed' must be comprised of the first and second inter-layer insulating films." Toshiba Br at 7. Accordingly, Toshiba proposes that "first inter-layer insulating film" should be construed as "that portion of the 'insulating film' which covers a portion of the surface of a substrate on which the MOSFET is formed" and that "second inter-layer insulating film" should receive the same construction with the word "that" replaced by "another." Jt Cl Const, Ex A at 13, 16.

Toshiba's proposed constructions, however, do not follow inexorably from the claim language. Merely because the claim recites "the bit line contact hole [is] made in an insulating film" does not preclude the bit line contact hole from additionally including "a first contact hole made in a first inter-layer insulating film" and "a second contact hole made in a second inter-layer insulating film." In other words, the claim could readily be interpreted, as Hynix contends, as requiring the contact holes to pass through three different insulating films: the "insulating film which covers a portion of the surface of a substrate," the "first inter-layer insulating film" and the "second inter-layer insulating film." Such a construction is correct for at least three reasons.

First, the claim itself suggests that the inter-layer insulating films are separate from the previously recited insulating film because the claim uses the indefinite article "a" before mentioning the inter-layer films. '579 patent at claim 1 ("said storage node contact hole and bit line contact hole includes a first contact hole made in *a first inter-layer insulating film* * * * and a second contact hole made in *a second inter-layer insulating film* ").

Second, it would seem anomalous to conclude that the "inter-layer insulating films" are necessarily part of the same "insulating film" given that Toshiba concedes that the two inter-layers are separate films and are deposited at different times, Toshiba Rep at 3, and at least one embodiment in the specification describes the films as separate and distinct from one another. See FIG 1(b) (separate inter-layer insulating films 13 and 23). Moreover, construing the "inter-layer insulating films" as part of the "insulating film" would either render superfluous the "inter-layer" limitation or would create an incoherent situation in which a unitary "insulating film" is somehow composed of discontinuous parts.

Finally, the specification consistently describes embodiments in which a film comprising silicon oxide, a well-known insulator, is deposited on the source and drain regions of the substrate surface and is subsequently removed via etching to create storage node contact holes and bit line contact holes. See '579 patent at 7:28-39, 9:54-60, 10:31-36, 13:21-27, 14:5-10, 19:56-60, 20:32-37. Compare FIGS 3(b), 12(b), 21(b) and 46(b) with FIGS 4(b), 16(b), 25(b) and 50(b), respectively (silicon oxide film 9 is removed to

form a first storage node contact hole 14 and a first bit line contact hole 15). This insulating film is deposited separately from the inter-layer insulating films, which the specification consistently describes as being deposited later. E g, id at 7:28-33 ("[A] silicon oxide film 9 of about 20 nm thickness is formed on the thus obtained substrate by the thermal oxidation method and then a silicon oxide film 13 as an inter-layer insulating film is deposited on the entire substrate by the CVD method."). The presence of this separate silicon oxide film strongly suggests that the "insulating film" through which the contact holes pass is separate from the "inter-layer insulating films."

Accordingly, the court adopts Hynix's proposed constructions, thereby construing "first inter-layer insulating film" as "a first insulating film that is located between layers and that is separate from and not a part of an insulating film covering the surface of said substrate on which the MOSFET is formed" and construing "second inter-layer insulating film" the same way but with "second" replacing "first."

3. "An electrically conductive layer embedded in said first contact hole up to a level higher than the gate electrode such as to be contacted with said electrically conductive layer"

For this very long "term," Toshiba proposes an even longer construction: "An electrically conductive layer is deposited in the first contact hole of an insulating film, with the electrically conductive layer covering the first contact hole. Thereafter, the electrically conductive layer is etched to expose the surface of the insulating film in which the first contact hole is formed with the electrically conductive layer left in the first contact hole at a height that is higher than the gate electrode. The electrically conductive layer is in contact with the 'second contact hole.' " Jt Cl Const, Ex A at 19. Hynix contends that this phrase should not construed because it is indefinite but alternatively proposes replacing "embedded" with "fixed firmly." Id.

Hynix contends that this term is indefinite because "one skilled in the art would not understand what structure of the claimed device must be 'contacted with said electrically conductive layer.' " In particular, Hynix contends it is unclear whether the "electrically conductive layer" is claim 1 is in contact with itself, the "first inter-layer insulating film," "first contact hole," "second inter-layer insulating film," "second contact hole" or the "gate electrode." Hynix Br at 9.

While the court agrees that this "term" is quite poorly written, its meaning is not ambiguous if read in light of the specification. The clause in which this term appears states in full (with the term emphasized):

wherein at least one of said storage node contact hole and bit line contact hole includes a first contact hole made in a first inter-layer insulating film formed over said gate electrode and a second contact hole made in a second inter-layer insulating film formed over *an electrically conductive layer embedded in said first contact hole up to a level higher than the gate electrode such as to be contacted with said electrically conductive layer*.

Figure 1(b) depicts an embodiment encompassed by this claim; Figures 2(b), 3(b), 4(b), 5(b), 6(b), 7(b) and 8(b) and their accompanying text describe how the embodiment pictured in Figure 1(b) was created. First, a metal-oxide semiconductor field-effect transistor (MOSFET) is formed on a substrate, with a gate electrode 6 and source and drain regions 4a and 4b. See FIGS 1(b), 2(b). An inter-layer insulating film 13 (corresponding to the "first inter-layer insulating film" in the claim) is then laid on top of the MOSFET. See FIG 3(b). The inter-layer insulating film 13 is then etched to create a first storage node contact hole 14 and a first bit line contact hole 15 (corresponding to the "first contact hole" in the claim). See FIG 4(b). The contact holes are then filled with a heavily doped polycrystalline silicon film 16 (corresponding to the

"electrically conductive layer" in the claim) up to a level higher than the gate electrode. See FIG 5(b). A storage node electrode 20, capacitor insulating film 21, plate electrode 22 and inter-layer insulating film 23 (corresponding to the "second inter-layer insulating film") are then laid on top of the polycrystalline silicon film 16. FIG 7(b). Finally, the inter-layer insulating film 23 is etched to create a bit line contact 24 (corresponding to the "second contact hole" in the claim). Accordingly, this embodiment makes clear that, as Toshiba argues, claim 1 teaches that the "second contact hole" is "contacted with said electrically conductive layer." The other embodiments in the specification appear to be mere variations on this first embodiment and also support this conclusion. See, e g, '579 patent at 12:38-43. (Embodiment 6: "Provided on the MOSFET is an inter-layer insulating film 23 which in turn is opened with a contact hole. The polycrystalline silicon layer 16 as the embedded layer is formed as contacted with the n-type diffusion layers 4a and 4b through the contact hole opened in the inter-layer insulating film 23."). See also Allen Engineering Corp v. Bartell Industries, Inc, 299 F3d 1336, 1348 (Fed Cir2002) ("[O]ne skilled in the art would understand the bounds of the claim when read in light of the specification.").

Turning to the construction of the "term," Hynix contends that "embedded" should receive its purported ordinary meaning of "fixed firmly." Hynix Br at 8-9. Toshiba instead contends that "embedded" has a special meaning in this patent because the specification "describes two [different] methods of filling the contact hole with electrically conductive material-by an 'embedding' process or by a 'selective growth' process." Toshiba Br at 8. See, e g, '579 patent at 8:1-5 ("Although the polycrystalline silicon film has been embedded all over and then again subjected to the etching in the foregoing steps, the polycrystalline or monocrystalline silicon film may be selectively grown only in the contact cavities as an example."); id at 14:32-35 ("Although the polycrystalline silicon film has been embedded all over and then again subjected to the etching in the foregoing steps, the polycrystalline or monocrystalline silicon film may be selectively grown only in the contact cavities as an example."); id at 16:64-68 (same).

Nonetheless, the court cannot conclude that these embodiments necessarily indicate that the patentees intended to "act[ ] as [their] own lexicographer[s] and clearly set forth a definition of the disputed claim." CCS Fitness, 288 F3d at 1366. Indeed, dependent claim 7 suggests that the term "embedded" encompasses both "embedding" and "selective growth" processes. That claim states:

7. A semiconductor memory device as set forth in any of claims 1 to 5, *wherein said electrically conductive layer is grown* to have a thickness larger than a depth of said first contact hole and to be expanded over a top of the first contact hole.

The patentees' use of the word "grown" here suggests that the "embedded" film in claim 1 could be deposited through a "selective growth" process. Hence, the court rejects Toshiba's construction.

The court also rejects Hynix's proposed substitution of "fixed firmly" for "embedded" given that the ordinary meaning of "embedded" is sufficiently clear and need not be redefined.

In sum, the court finds that the present term is not indefinite and declines to construe the term.

The '994 patent

The '994 patent "relates to a non-volatile semiconductor memory device having a rewrite data setting function," which verifies that data has been properly written to memory. '994 patent at 1:15-16.

1. "bit line"

Claims 1, 4, 7, 10, 15, 18 and 21 contain the term "bit line." Although Toshiba contends that "bit line" need not be construed because it has a well-understood meaning, Toshiba alternatively proposes that "bit line" means "a line coupling the non-volatile memory cell to the sense amplifier during the read cycle and to a data line or latch during a write cycle." Jt Cl Const, Ex B at 1. Hynix construes "bit line" as "an uninterrupted conductor that directly connects to one or more memory cell units." *Id*. In essence, Hynix seeks to read in an additional limitation to the term, namely, that a "bit line" is "uninterrupted by a transistor ." *Id*.

Hynix's arguments fail to persuade. Hynix notes that a "bit line" cannot possibly include a "switching circuit" because the relevant claims specify that a "switching circuit" connects the "bit line" to another electrical component. See '994 patent at claims 1, 4, 7, 10, 15, 18 and 21. But just because the "switching circuit" may include a transistor component does not mean the "bit line" *cannot* contain any transistor, which is the unwarranted limitation Hynix suggests in its construction.

Hynix next argues that the specification never describes the "bit line" as anything other than an uninterrupted conductor. Hynix Br at 12. Even if Hynix is correct, this does not amount to an "intentional disclaimer, or disavowal, of claim scope by the inventor." Phillips, 415 F3d at 1316. The specification does not include any language indicating that a "bit line" must be an uninterrupted conductor or that the absence of a transistor along a bit line distinguishes the invention from the prior art. It would be improper for the court to read in this limitation simply based on the preferred embodiments. See Teleflex, 299 F3d at 1326.

Finally, Hynix resorts to the prosecution history of two related patents, United States Patent Nos 6,493,267 ("the '267 patent") and 5,726,882 ("the '882 patent"), that share virtually the same specification as the '994 patent. Hynix argues Toshiba made two statements to the patent office disavowing "any definition of bit line that includes a line interrupted by a transistor." Hynix Br at 13. In a letter requesting reconsideration of the '267 patent, the patentees distinguished the "bit line" from another wire on the other side of the switching circuit transistor. Doc # 14, Ex E at 2. But this letter adds nothing to Hynix's case because the patent claims already show that the bit line does not extend past the switching circuit. Hynix also relies on a letter from the patentees requesting an extension of time pertaining to the '882 patent but this letter does not speak to the definition of "bit line" and merely references an embodiment present in the ' 994 patent. *Id,* Ex L at 7.

Because Hynix's construction is problematic and Hynix has not provided any reason why the ordinary meaning of "bit line" does not suffice, the court declines to construe this term.

2. "supplied with a potential of"

Claims 7 and 15 contain the term "supplied with a potential of." Toshiba contends that the ordinary meaning of the phrase should apply. Jt Cl Const, Ex B at 20. Alternatively, Toshiba proposes that the phrase means "applied with a voltage of." *Id*. Hynix construes this term as " *directly* supplied with the potential of." *Id* (emphasis added). Again, Hynix seeks to read a limitation into the claim term, requiring that the potential be *directly* supplied.

Hynix's construction relies on a statement that the patentees made during prosecution of the related '267 patent. See *supra* "bit line" construction. The patentees distinguished prior art in which the potential of a certain transistor was less than the potential of a bit line by claiming that the ' 267 patent disclosed circuits supplying the same transistor with the same potential as the bit line. Doc # 14, Ex E at 2. Hence, Hynix

argues the distinguishing and necessary feature of the '994 patent, which is virtually identical to the '267 patent, is that the transistor is "directly" supplied with the same potential as the bit line.

But a plain reading of the patent prosecution statement does not yield Hynix's construction. The patentees merely distinguished the prior art by stating that the '994 patent transistor is "supplied with the potential of the bit line" instead of the lower potential available under the prior art. *Id*. The patentees never said whether the potential is supplied directly or indirectly. Hence, the prosecution history cited by Hynix does not warrant an additional limitation that the "bit line" potential be supplied directly.

Because Hynix has not provided any reason why "supplied with a potential of" should be construed and Toshiba's proposed construction appears nearly identical to the term itself, the court declines to construe this term.

3. "responsive to a potential of"

Claims 1, 4, 7, 10, 18 and 21 contain the phrase "responsive to a potential of." Toshiba contends that this simple term requires no construction. Jt Cl Const, Ex B at 12. Alternatively, Toshiba proposes that "responsive to a potential of" means "responding to a voltage of." *Id*. Hynix construes the phrase as " *directly* supplied with and *reacting* to the potential of." *Id* (emphasis added).

Hynix again seeks to import a limitation from the specification based on an exemplary embodiment. In particular, Hynix relies on Figure 13 to argue that the "gates of transistor Q7 are *directly* supplied with the potential on the bit lines (BL1, BL2, BL3)." *Id* at 16 (emphasis added). Hynix provides no other support for its proposed "directly" limitation. As noted previously, the court cannot import this limitation into a claim construction based on a preferred embodiment. See Teleflex, 299 F3d at 1326.

Because Hynix's construction is flawed and Hynix has not provided any reason why this seemingly simple term must be construed, the court declines to construe "responsive to a potential of."

4. "coupled between"

Claims 1, 4, 7, 10, 15, 18 and 21 contain the phrase "coupled between." Toshiba contends that no construction is necessary and the ordinary meaning of the phrase should apply. Jt Cl Const, Ex B at 9. Alternatively, Toshiba proposes that the phrase means "a current path permitting signals to be transferred between two points ." *Id*. Hynix construes "coupled between" as "[r]esiding between distinct elements and connecting the distinct elements directly or indirectly." *Id*.

Hynix illuminates the court with the following statement: "The phrase 'coupled between [sic] has two aspects: it must *couple* two elements and it must be *between* those two elements." Hynix Br at 17 (emphasis in original). While the court cannot disagree with Hynix's tautological reasoning, Hynix has not provided any reason why its far more cumbersome construction would assist a jury perform its duties better than the simple term "coupled between." Accordingly, the court declines to construe this term.

The '715 patent

The '715 patent describes a technique for producing nonvolatile semiconductor memory devices with better performance capabilities than memory devices produced by prior manufacturing techniques. '715 patent at 1:6-8, 5:34-51.

1. "a plurality of trenches"

This term appears in claims 1, 3 and 16 of the '715 patent. Toshiba does not believe "a plurality of trenches" requires construction but alternatively suggests the term means "more than one groove." Jt Cl Const, Ex C at 1. Hynix argues that the term means "a plurality of recessed areas in which the upper boundary of each trench is defined by the top surface of the material that is removed to form the trench." *Id*. Hynix appears to refer to the "recessed areas" as "trenches" even within its own definition; hence, the court gathers that the crux of Hynix's construction is construing a "trench" as being bounded "by the top surface of the material that is removed to form the trench."

The specification teaches that a trench is formed by removing material from the substrate. '715 patent at 2:60-67, 4:49-52, 15:9-12, 21:1-8. After the trench is formed, it may be eliminated or have its depth reduced by removing other material comprising the trench's side walls. *Id* at 4:57-68 (removal of nitride film). Hynix defines "trench" based on its original dimensions; that is, Hynix contends that a trench extends up to the top surface of the material originally removed to create the trench. But if a trench's side walls are later reduced, Hynix's definition leads to an anomaly in which a "trench" exists in a volume of space above its surrounding material. Hynix has not shown that a person of ordinary skill in the art would expect this counterintuitive result, which contravenes the ordinary understanding that a "trench" is defined by its depth relative to the surface at any given time.

Accordingly, the court rejects Hynix's construction and the court declines to construe this straightforward term.

2. "plurality of trenches having an insulator embedded therein"

This phrase appears in claims 1 and 3 of the '715 patent. Toshiba does not believe the term requires construction but alternatively proposes it means "more than one trench with insulator residing within the trench." Jt Cl Const, Ex C at 4. Hynix argues that "plurality of trenches having an insulator embedded therein" means "a plurality of trenches having an insulator wholly residing within the trench." *Id*.

The parties principally disagree whether the claims specify insulators that reside *wholly* within the trenches or not. Both parties agree that the specification discloses at least two embodiments in which the insulators do not reside wholly within the trench, but rather protrude above it. Hynix Br at 21; Toshiba Br at 15-16. See, e g, '715 patent at FIGS 9H and 13B. But Hynix argues that Toshiba disclaimed these embodiments.

First, Hynix points to language in the specification suggesting that the embodiments in which the insulator protrudes from the trench are disadvantageous and therefore disavowed by Toshiba. *Id* at 22:30-37. But even if the specification acknowledges that these embodiments had shortcomings, that alone does not constitute an express disclaimer of subject matter by the patentees. CCS Fitness, 288 F3d at 1366-67. The claim language plainly allows for an insulator to be embedded in a trench but still protrude from the trench.

Second, Hynix argues that during prosecution the patentee disclaimed any embodiments in which the insulator did not protrude from the trench. Hynix relies on a summary of an interview with a patent examiner in which the examiner noted that if the patentee amended claim 1 "to further clarify an element isolation to wholly reside within a trench then that would be sufficient to defeat [prior art]." Doc # 14, Ex O. But "[d]isclaimers based on disavowing actions or statements during prosecution * * * must be both clear and unmistakable. Moreover, it is the applicant, not the examiner, who must give up or disclaim subject

matter that would otherwise fall within the scope of the claims." Sorensen v. ITC, 427 F3d 1375, 1378-1379 (Fed Cir2005) (internal citations and quotations omitted). A one-line summary by the examiner including the word "wholly" is not a "clear and unmistakable" disavowal by the patentees. Indeed, in subsequently characterizing their agreement with the examiner, the patentees stated that they would "further clarify that the element isolators reside within a trench"-notably not using the word "wholly." Doc # 14, Ex P at 9. And because the claim as amended and allowed does not include the word "wholly," the court declines Hynix's invitation to read in what appears to have been deliberately left out.

Accordingly, the court rejects Hynix's construction and declines to construe the term.

3. "embedded insulator(s)"

This term appears in all claims in the '715 patent except for claims 7, 10, 12 and 15. Toshiba does not believe that the term requires construction. Alternatively, Toshiba suggests that the term means "insulator(s) residing within the trench(es)." Jt Cl Const, Ex C at 13. Hynix argues that "embedded insulator(s)" means "insulating material residing wholly within the trench." *Id*.

As with the previous term, the parties principally disagree whether the claims specify that the insulators must reside *wholly* within the trenches. The court has already determined that the patent does not contain such a limitation. See *supra* construction for "plurality of trenches having an insulator embedded therein." Accordingly, the court rejects Hynix's construction and declines to construe the term.

4. "side surfaces of said embedded insulator being substantially perpendicular to said semiconductor substrate"

This term appears in claim 1 of the '715 patent and a virtually identical phrase appear in claim 3 with the word "therein" inserted between "insulator" and "being." Toshiba does not believe the term requires construction but alternatively suggests the phrase means "side surfaces of the insulator are to a large degree perpendicular to the semiconductor substrate." Jt Cl Const, Ex C at 11. Hynix asserts that this term is indefinite, but in the alternative, proposes that it means "side surfaces of the embedded insulators are within one or two degrees of perpendicular to the semiconductor substrate." *Id*.

Hynix argues that the phrase "substantially perpendicular" is indefinite because "it is unclear what degree of taper, if any, may be present" in the side walls of the embedded insulators. Hynix Br at 24. In particular, Hynix argues this phrase embraces only the minor, one or two degree variations in perpendicularity incidentally formed by the reactive ion etching (RIE) techniques used in this invention. According to Hynix, "substantially perpendicular" cannot encompass deliberate attempts to taper the side walls of the embedded insulators through "RIE techniques under taper etching conditions."

But Hynix's arguments ring hollow. First, Hynix's contentions regarding "RIE techniques under taper etching conditions" have no bearing on the degree of taper in the side walls of the embedded insulators. The patent discusses this fabrication technique only once with respect to creating tapered side walls for the *etch masks,* not the *embedded isolators*. '715 patent at 25:9-12, FIG 37.

More importantly, the specification depicts numerous embodiments in which the side walls of the embedded insulator are slanted by more than one or two degrees. See '715 patent FIGS 15A, 15B, 18, 19, 20A, 20B, 21, 22, 23A, 23B, 24A, 24B, 25A, 25B, 29, 30, 31, 32, 33, 35, 36, 37, 38, 40. Indeed, the court's measurements of the embodiments in these figures indicate that these side walls deviate by at least seven (7)

degrees. Hynix's construction would exclude these embodiments and is therefore disfavored. See C R Bard, 388 F3d at 865 ("[A] construction that excludes a preferred embodiment 'is rarely, if ever, correct.' ").

Although the patent does not provide a numerical limitation for the term "substantially," the disclosed embodiments and the ordinary and plain meaning of "substantially" should be sufficient to guide a jury in performing its duties. If necessary, and if the parties marshal any new intrinsic evidence, the court would consider revisiting this issue at a later date. But for present purposes, the court rejects Hynix's construction and declines to construe this term.

5. "a plurality of memory cell transistors and a plurality of select transistors formed in said plurality of element regions"

This phrase appears in claims 1 and 16 of the '715 patent. Toshiba does not believe that the phrase requires construction but alternatively proposes replacing "a plurality of" and "said plurality of" with "more than one" throughout the term, changing "formed" with "are made," and changing "transistors" and "regions" to their singular forms. Jt Cl Const, Ex C at 20. Hynix argues that the phrase means "a plurality of memory cell transistors and a plurality of select transistors, each of which resides within one of the plurality of element regions." *Id*.

Hynix's construction requires each transistor reside "within one of the plurality of element regions." But the claim language requires only that the transistors be "formed in" these regions. Hynix appears to use "formed in" and "within" interchangeably but Toshiba correctly notes that "within" imports an additional limitation requiring a transistor to be wholly contained inside an element region, whereas a transistor might be "formed in" an element region but include components extending outside the region. Indeed, Hynix's proposed construction would impermissibly exclude the many "T-shaped floating gate" embodiments that have transistors extending laterally beyond the element regions. See '715 patent at FIGS 9G, 9H, 13B, 15A, 15B, 35, 40, 42A, 42B. Hence, Hynix's use of "within" is inappropriate because it imports a limitation supported by neither the specification nor the claim language.

Hynix also argues that each memory cell transistor or select transistor can exist only in a single element region rather than being spread over multiple regions. The language of claims 1 and 16 supports this construction. Those claims specify that "each of said plurality of memory cell transistors" is comprised of different elements stacked atop one another, the bottommost of which is "a first gate insulating film formed on *a corresponding one* of said plurality of first element regions." *Id* at 34:54-57, 37:28-31 (emphasis added). Similarly, those claims specify that "each of said plurality of select transistors" is comprised of multiple stacked elements beginning with "a third gate insulating film formed on *a corresponding one* of said plurality of element regions." *Id* at 34:67-35:2, 37:42-44 (emphasis added). Hence, while a memory cell transistor or select transistor might *extend* outside an element region, each transistor is *formed* in one, and only one, element region.

Accordingly, the court adopts a hybrid construction for this term: "a plurality of memory cell transistors and a plurality of select transistors, each transistor of which is formed in one of said plurality of element regions."

6. "a plurality of memory cell transistors formed in said plurality of first element regions"

This phrase appears in claim 3 of the '715 patent. Toshiba does not believe the phrase requires construction but alternatively proposes it means "more than one memory cell transistor fabricated in more than one

element region." Jt Cl Const, Ex C at 29. Hynix argues that the phrase means "a plurality of memory cell transistors, each of which resides within one of the plurality of first element regions." *Id*.

The parties advance the same arguments as for the previous term. Accordingly, the court adopts a similar hybrid construction: "a plurality of memory cell transistors, each transistor of which is formed in one of said plurality of first element regions."

7. "a third gate insulating film formed on a corresponding one of said plurality of element regions"

This term appears in claims 1 and 16 of the '715 patent. Toshiba does not believe the term requires construction but alternatively suggests it means "a gate insulating film made on the element region that relates to the select transistor." Jt Cl Const, Ex C at 26. Hynix argues the term is indefinite and should not be construed. Alternatively, Hynix asserts the term means "a third gate insulating film formed within a corresponding one of the plurality of element regions." *Id*.

Hynix first argues that the term is indefinite because it is logically impossible to "form" anything on a "region," a two-dimensional area with no defined top surface. While this argument may make some sense as a hypertechnical matter, a person of ordinary skill in the art in the semiconductor manufacturing industry would undoubtedly understand that an insulating film is formed on the substrate's exposed portion within the relevant element region. Hence, the term is not indefinite.

Hynix further argues that the phrase "formed on" as used in claim 3 should mean "formed within." This is essentially the same argument that the court already rejected in construing the term "a plurality of memory cell transistors and a plurality of select transistors formed in said plurality of element regions." To require the insulating film be "formed within" an element region would impermissibly limit the present term.

Accordingly, the court rejects Hynix's construction and declines to construe this term.

The '588 patent

The '588 patent describes an invention for increasing the reliability and manufacturing yield of non-volatile semiconductor memory devices by use of a novel circuit design. '588 patent, Abstract. The parties dispute only one "term" (emphasized below), which appears in claim 1:

1. A semiconductor memory device comprising:

a memory cell array having memory cells or memory cell units formed by connecting at least one memory cell, said memory cells or memory cell units being arranged in an array form,

wherein *selection gate lines are formed by use of a mask having a data pattern in which the width of at least one of a word line and a selection gate line arranged on the end portion of said memory cell array is set larger than that of at least one of a word line and selection gate line arranged on the other portion of said memory cell array*.

Toshiba contends that the term does not need construction, but if construed, the term means "lines connected to the gates of selection transistors are fashioned by a mask with a data pattern such that the width of a word line and a selection gate line on one end portion of the memory array is larger than the width of a word line and a selection gate line on the other end portion of the memory array." Jt Cl Const, Ex D at 1. Hynix

asserts that this phrase is indefinite, but in the alternative, proposes a construction of "selection gate lines are formed by use of a mask having a data pattern in which each of the outermost selection gate line(s) and adjacent word line(s) are wider than the corresponding inner selection gate line(s) and adjacent word line(s)." *Id*.

Hynix contends the claim is indefinite because it is unclear what constitutes the "end portion" and the "other portion" of the "memory cell array." But before the court can even address this argument, the court must determine what the term "memory cell array" means.

"Memory cell array" appears to encompass two different meanings in the specification. The patent describes a "memory cell array" as "memory cells or memory cell units arranged in an array form." See '588 patent at 7:7-11, 7:19-23, 7:29-33, 7:43-46, 7:61-63. The patent also uses "memory cell array" to describe a larger array formed from multiple "blocks" of memory cells. See id at 2:15-19, 10:34-37, 6:62-7:6, Abstract. And the preferred embodiments use "memory cell array" to refer to both smaller arrays of memory cells and larger arrays of "blocks." *Id* at 18:57-19:6. Hence, on its face, the term "memory cell array" as used in claim 1 encompasses both arrays of *memory cells* and arrays of *blocks of memory cells*.

Nonetheless, Toshiba argues this term should not be construed to encompass arrays of "blocks" because related United States Patent Nos 6,836,444 and 7,002,845, which share the same specification as the '588 patent, "claim the array of blocks." Toshiba Rep at 19. But the claims in those patents are not coextensive with claim 1 of the '588 patent. Hence, it is not inconsistent for claim 1 to encompass arrays of "blocks" even if claims in other patents also encompass such arrays.

Moreover, Toshiba's argument fails because the parties' joint construction of "memory cell units" as "a structure having one or more memory cells connected together in series" bears strong resemblance to the specification's description of "blocks" as being "constructed by serially connecting a plurality of memory cells * * *." Doc # 30 at 20; '588 patent at 1:15-20. Since the "memory cell array" of claim 1 may be composed of "memory cell units," it appears that such an array may be composed of "blocks" of memory cells.

Because "memory cell array" could be interpreted as comprising either *memory cells* or *blocks of memory cells,* if the use of "end portion" in either of these contexts is unclear, then the claim is indefinite. This problem is compounded because the specification sometimes uses "end portion" to refer to only *one* end of a memory cell array, and at other times uses "end portion" to refer to *both* ends of a memory cell array. See '588 patent at 3:41-48 (referring to "blocks" on both ends of an array) and at 6:17-21 (referring to a single block on one end portion of an array).

When the specification uses "memory cell array" to refer to a single block of memory cells, there are two, and only two, selection gate lines, one at each end of the array. See id at FIGS 3A, 3B, 5A, 5B (showing selection gate lines SG1 and SG2 at the two ends of the array). Since claim 1 requires that both the "end portion" and the "other portion" each contain a selection gate line, "end portion" can refer to only one end; if it embraced both ends, there would not be an "other portion" containing a selection gate line. Indeed, the specification uses "end portion" to refer to only one end in the embodiments in which "memory cell array" refers to a single block of memory cells. *Id* at 23:11-32. Hence, the "end portion" in an array of memory cells is the portion, at either end of the array, containing a selection gate line and its corresponding word line.

When the specification uses "memory cell array" to refer to a larger array of blocks of memory cells, the meaning of "end portion" is equally clear. The specification consistently refers to the "end portion" of the array of memory cell blocks as the outermost *single* "block" on either end of the array. E g, id at 3:33-48, 8:10-19, 13:20-27, 14:29-35, 14:50-53, 15:3-8. The specification does not appear to use "end portion" to refer any block except the terminal block at either end of the array. Although the specification refers to specific *lines* "on the end portion," this is not inconsistent with the notion that the "end portion" refers to the end "block" containing those lines. *Id* at 17:40-45.

In sum, the "end portion" in an array of "blocks" is the portion defined by the outermost "block" on either end of the array and may refer to one or both ends. If "end portion" refers to one end, "other portion" refers to the rest of the array. If "end portion" refers to both ends, "other portion" refers to the blocks in the midsection of the array, i e, the non-terminal blocks.

Because the court has been able to divine the meaning of "end portion" and "other portion" within a "memory cell array," the term is not indefinite. Allen Engineering, 299 F3d at 1348 (Fed Cir2002) ("[O]ne skilled in the art would understand the bounds of the claim when read in light of the specification.").

Finally, the court rejects Hynix's construction of this term because its construction contradicts the claim language. Hynix requires that the selection gate lines on *both* end portions of the array be wider than any other selection gate line in the "inner" portion. But the claim does not include any such requirement; rather, the claim requires only that " *at least one* * * * selection gate line arranged on the end portion of said memory cell array is set larger than * * * *at least one* * * * selection gate line arranged on the other portion of said memory cell array." '588 patent, 34:13-23 (emphasis added). Since "end portion" can either refer to just *one* end of an array in certain embodiments, Hynix's construction introduces an unwarranted limitation.

Accordingly, the court rejects Hynix's construction and declines to construe the term.

III

In sum, the court has construed some of the disputed terms of the '579, ' 994, '715 and '588 patents according to the intrinsic record and the patents' plain language. The court declined to construe many terms because their meanings were already clear or no longer ambiguous after the court had construed other related terms. The clerk is DIRECTED to file the parties' submissions in support of their *Markman* presentations.

IT IS SO ORDERED.

N.D.Cal.,2006.
Toshiba Corp. v. Hynix Semiconductor, Inc.