United States District Court,
S.D. California.

QUALCOMM INCORPORATED,
Plaintiff.
v.
BROADCOM CORPORATION,
Defendants.
Broadcom Corporation,
Counter-Claimant.
v.
Qualcomm Incorporated,
Counter-Defendant.

Civil No. 05CV1392-B(BLM)

May 1, 2006.

Adam Arthur Bier, Christian E. Mammen, James R. Batchelder, Day Casebeer Madrid and Batchelder, Kevin Kook Tai Leung, Law Office of Kevin Kook Tai Leung, Cupertino, CA, Barry Jerome Tucker, David E. Kleinfeld, Foley & Lardner LLP, James T. Hannink, Kathryn Bridget Riley, Randall Evan Kay, Brooke Beros, Dla Piper US, Brandon Hays Pace, Heller Ehrman LLP, Heidi Maley Gutierrez, Higgs Fletcher and Mack, San Diego, CA, E Joshua Rosenkranz, Heller Ehrman, Evan R. Chesler, Richard J. Stark, Cravath Swaine and Moore LLP, Richard S. Taffet, Bingham McCutchen, New York, NY, Nitin Subhedar, Heller Ehrman, Menlo Park, CA, Jaideep Venkatesan, Heller Ehrman, Menlo Park, CA, Jason A. Yurasek, Perkins Coie LLP, San Francisco, CA, Patrick Taylor Weston, McCutchen Doyle Brown and Enersen, Walnut Creek, CA, William F. Abrams, Bingham McCutchen, East Palo Alto, CA, for Plaintiff.

Alejandro Menchaca, Andrew B. Karp, Brian C. Bianco, Christopher N. George, Consuelo Erwin, George P. McAndrews, Gregory C. Schodde, Joseph F. Harding, Lawrence M. Jarvis, Leonard D. Conapinski, Matthew A. Anderson, Ronald H. Spuhler, Scott P. McBride, Stephen F. Sherry, Thomas J. Wimbiscus, Jean Dudek Kuelper, McAndrews Held and Malloy, Chicago, IL, Allen C. Nunnally, Daniel M. Esrick, John J. Regan, John S. Rhee, Joseph F. Haag, Kate Saxton, Louis W. Tompros, Richard W. O'Neill, Stephen M. Muller, Vinita Ferrera, Wayne L. Stoner, William F. Lee, Wilmer Cutler Pickering Hale and Dorr, Boston, MA, James Sullivan McNeill, Robert S Brewer, Jr, McKenna Long and Aldridge, San Diego, CA, James L Quarles, III, William J. Kolasky, Wilmer Cutler Pickering Hale and Dorr LLP, Alina D. Eldred, Mark W. Nelson, Steven J. Kaiser, Cleary Gottleib Steen and Hamilton, Washington, DC, Maria Kathleen Vento, Mark D. Selwyn, Wilmer Cutler Pickering Hale and Dorr LLP, Palo Alto, CA, for Defendants.

Barry Jerome Tucker, Foley & Lardner LLP, San Diego, CA, Evan R. Chesler, Cravath Swaine and Moore LLP, Richard S. Taffet, Bingham McCutchen, E Joshua Rosenkranz, Heller Ehrman, New York, NY, James R. Batchelder, Day Casebeer Madrid and Batchelder, Cupertino, CA, Nitin Subhedar, Heller Ehrman, Menlo Park, CA, Jean Dudek Kuelper, McAndrews Held and Malloy, Chicago, IL, Mark W. Nelson, Cleary Gottlieb Steen and Hamilton, Washington, DC, for Counter-Claimant.

Barry Jerome Tucker, Foley & Lardner LLP, San Diego, CA, Evan R. Chesler, Cravath Swaine and Moore LLP, Richard S. Taffet, Bingham McCutchen, E Joshua Rosenkranz, Heller Ehrman, New York, NY, James R. Batchelder, Day Casebeer Madrid and Batchelder, Cupertino, CA, Jason A. Yurasek, Perkins Coie LLP, San Francisco, CA, Patrick Taylor Weston, McCutchen Doyle Brown and Enersen, Walnut Creek, CA, William F. Abrams, Bingham McCutchen, East Palo Alto, CA, Nitin Subhedar, Heller Ehrman, Menlo Park, CA, Andrew B. Karp, Brian C. Bianco, Christopher N. George, Gregory C. Schodde, Matthew A. Anderson, Ronald H. Spuhler, Scott P. McBride, Stephen F. Sherry, Thomas J. Wimbiscus, Jean Dudek Kuelper, Lawrence M. Jarvis, Leonard D. Conapinski, McAndrews Held and Malloy, Chicago, IL, James L. Quarles, III, William J. Kolasky, Wilmer Cutler Pickering Hale and Dorr LLP, Mark W. Nelson, Cleary Gottlieb Steen and Hamilton, Washington, DC, Maria Kathleen Vento, Mark D. Selwyn, Wilmer Cutler Pickering Hale and Dorr LLP, Palo Alto, CA, Richard W. O'Neill, Stephen M. Muller, Wayne L. Stoner, William F. Lee, Allen C. Nunnally, Daniel M. Esrick, John J. Regan, Vinita Ferrera, Wilmer Cutler Pickering Hale and Dorr, Boston, MA, Robert S. Brewer, Jr, James Sullivan McNeill, McKenna Long and Aldridge, San Diego, CA, for Counter-Defendant.

CLAIM CONSTRUCTION ORDER FOR UNITED STATES PATENT NUMBER 5,946,344

RUDI M. BREWSTER**, Senior District Judge.**

Pursuant to Markman v. Westview Instruments, Inc., 517 U.S. 370, 116 S.Ct. 1384, 134 L.Ed.2d 577 (1996), on March 27-30, 2006, and April 3, 2006, the Court conducted a Markman hearing concerning the above-titled patent infringement action regarding construction of the disputed claim terms for U.S. Patent Number 5,946,344 ("the '344 patent"). Plaintiff Qualcomm, Inc. was represented by the law firm of Heller Ehrman LLP, and Defendant Broadcom Corp. was represented by the law firm of McAndrews, Held & Malloy, Ltd.

At the Markman hearing, the Court, with the assistance of the parties, analyzed the claim terms in order to prepare jury instructions interpreting the pertinent claims at issue in the '344 patent. Additionally, the Court prepared a case glossary for terms found in the claims and specification for the '344 patent considered to be technical in nature which a jury of laypersons might not understand clearly without a specific definition.

After careful consideration of the parties' arguments and the applicable statutes and case law, the Court **HEREBY CONSTRUES** the claims in dispute for the '344 patent and **ISSUES** the relevant jury instructions as written in Exhibit A, attached hereto. Further, the Court **HEREBY DEFINES** all pertinent technical terms as written in Exhibit B, attached hereto.

IT IS SO ORDERED.

EXHIBIT A FN1

UNITED STATES PATENT NUMBER 5,946,344-CLAIM CHART

VERBATIM CLAIM LANGUAGE	**COURT'S CONSTRUCTION**
Claim 1	**Claim 1**
1. A digital matched filter for a spread spectrum communication system comprises:	A ***digital matched filter for a spread spectrum communication system*** [*a detector that recovers an original digital information signal that was spread over a wide band of*

	frequencies] ***comprises*** [*includes but is not limited to*]:
a digital delay line having a plurality of successive delay stages adapted to receive a digital signal and propagate said digital signal therethrough at a fixed rate;	***digital delay line having a plurality of successive delay stages adapted to receive a digital signal and propagate said digital signal therethrough at a fixed rate*** [*a device that moves digital input values through successive storage locations at a fixed rate. The digital values are delayed by being held in each storage location*];
a first correlator coupled to said digital delay line to correlate said digital signal to a first spreading code having a length M;	a first ***correlator*** [*device which is capable of comparing two signals to determine the extent to which they agree or disagree*] ***coupled*** [*operativelv connected*] to said ***digital delay line*** to ***correlate*** [*to compare two signals to determine the extent to which they agree or disagree*] said digital signal to a first ***spreading code*** [*a predetermined length sequence of chips that is used to modulate or 'spread' the signal before it is sent and that is used to demodulate or despread the signal after it is received*] having a length M;
a second correlator coupled to said digital delay line to correlate said digital signal to a second spreading code having a length N, wherein N is less than M; and	a second ***correlator coupled*** to said ***digital delay line*** to ***correlate*** said digital signal to a second ***spreading code*** having a length N, wherein N is less than M; and
a multiplexer coupled to each of said first and second correlators, said multiplexer selecting an output from one of said first and second correlators that correlates to a respective one of said first and second spreading codes, whereby said first spreading code is used to transmit at a lower data rate with higher jamming resistance, and said second spreading code is used to transmit at a higher data rate with lower jamming resistance.	a ***multiplexer*** [*a device that selects one of its inputs to provide an output*] ***coupled*** to each of said first and second ***correlators,*** said ***multiplexer*** selecting an output from one of said first and second ***correlators*** that ***correlates*** to a respective one of said first and second ***spreading codes,*** whereby said first ***spreading code*** is used to transmit at a lower ***data rate*** [*amount of factual information per unit of time*] with higher ***jamming resistance*** [*resistance to interfering and/or noise-like signals*], and said second ***spreading code*** is used to transmit at a higher ***data rate*** with lower ***jamming resistance.***
Claim 2	**Claim 2**
2. The digital matched filter of claim 1, wherein said first correlator further comprises:	2. The ***digital matched filter*** of claim 1, wherein said first ***correlator*** farther ***comprises:***
M logic gates each having a first input coupled to a corresponding one of said stages of said digital delay line and a second input coupled to a corresponding bit of said first spreading code; and	M ***logic gates*** [*basic electrical building blocks where the state of a logic gate's output is determined by the states of its inputs*] each having a first input ***coupled*** to a corresponding one of said stages of said ***digital delay line*** and a second input coupled to a corresponding ***bit*** [*a character used to represent one of two digits in a system having two possible states, e.g., high or low, on or off, one or zero, + or -, true or false, etc.*] of said first ***spreading code;*** and
a summing device coupled to respective outputs of each of said M logic gates to provide a sum of said outputs indicating a correlation between said first spreading code and said digital signal.	a summing device ***coupled*** to respective outputs of each of said M ***logic gates*** to provide a sum of said outputs indicating a ***correlation*** between said first ***spreading code*** and said digital signal.

Claim 3	**Claim 3**
3. A digital matched filter for a spread spectrum communication system comprising:	3. A ***digital matched filter for a spread spectrum communication system comprising:***
a digital delay line having a plurality of successive delay stages adapted to receive a digital signal and propagate said digital signal therethrough at a fixed rate;	a ***digital delay line having a plurality of successive delay stages adapted to receive a digital signal and propagate said digital signal therethrough at a fixed rate;***
a first correlator coupled to said digital delay line to correlate said digital signal to a first spreading code having a length M;	a first ***correlator coupled*** to said ***digital delay line*** to ***correlate*** said digital signal to a first ***spreading code*** having a length M;
a second correlator coupled to said digital delay line to correlate said digital signal to a second spreading code having a length N, wherein N is less than M; and	a second ***correlator coupled*** to said ***digital delay line*** to ***correlate*** said digital signal to a second ***spreading code*** having a length N, wherein N is less than M; and
a multiplexer coupled to each of said first and second correlators, said multiplexer selecting an output from one of said first and second correlators that correlates to a respective one of said first and second spreading codes, wherein said first correlator further comprises:	a ***multiplexer coupled*** to each of said first and second ***correlators,*** said ***multiplexer*** selecting an output from one of said first and second ***correlators*** that ***correlates*** to a respective one of said first and second ***spreading codes,*** wherein said first ***correlator*** further ***comprises:***
M logic gates each having a first input coupled to a corresponding one of said stages of said digital delay line and a second input coupled to a corresponding bit of said first spreading code; and	M ***logic gates*** each having a first input ***coupled*** to a corresponding one of said stages of said ***digital delay line*** and a second input ***coupled*** to a corresponding ***bit*** of said first ***spreading code;*** and
a summing device coupled to respective outputs of each of said M logic gates to provide a sum signal therefrom indicating a correlation between said first spreading code and said digital signal, wherein said first correlator further comprises means for deriving a data signal and a clock signal from said sum signal.	a summing device ***coupled*** to respective outputs of each of said M ***logic gates*** to provide a sum signal therefrom indicating a ***correlation*** between said first ***spreading code*** and said digital signal, wherein said first ***correlator*** further ***comprises means for deriving a data signal and a clock signal from said sum signal [This is a means-plus-function limitation.*** *The function is deriving a data signal and a clock signal from said sum signal. The corresponding structure is a tracking and bit synchronization logic unit and equivalents thereof.].*
Claim 5	**Claim 5**
5. The digital matched filter of claim 2, wherein said logic gates further comprise exclusive-OR logic gates.	The ***digital matched filter*** of claim 2, wherein said ***logic gates*** further ***comprise exclusive-OR logic gates*** [*logic gates whose outputs are true if either one of their respective inputs, but not both inputs, is true*].
Claim 7	**Claim 7**
7. A digital matched filter for a spread spectrum communication system comprising:	7. A ***digital matched filter for a spread spectrum communication system comprising:***
a digital delay line having a plurality of successive delay stages adapted to receive a	a ***digital delay line having a plurality of successive delay stages adapted to receive a digital signal and propagate said***

digital signal and propagate said digital signal therethrough at a fixed rate;	***digital signal therethrough at a fixed rate;***
a first correlator coupled to said digital delay line to correlate said digital signal to a first spreading code having a length M;	a first ***correlator coupled*** to said ***digital delay line*** to ***correlate*** said digital signal to a first ***spreading code*** having a length M;
a second correlator coupled to said digital delay line to correlate said digital signal to a second spreading code having a length N, wherein N is less than M; and	a second ***correlator coupled*** to said ***digital delay line*** to ***correlate*** said digital signal to a second ***spreading code*** having a length N, wherein N is less than M; and
a multiplexer coupled to each of said first and second correlators, said multiplexer selecting an output from one of said first and second correlators that correlates to a respective one of said first and second spreading codes, wherein said second correlator further comprises:	a ***multiplexer coupled*** to each of said first and second ***correlators,*** said ***multiplexer*** selecting an output from one of said first and second ***correlators*** that ***correlates*** to a respective one of said first and second ***spreading codes,*** wherein said second ***correlator*** further ***comprises:***
N logic gates each having a first input coupled to a corresponding one of said stages of said digital delay line and a second input coupled to a corresponding bit of said second spreading code; and	N ***logic gates*** each having a first input ***coupled*** to a corresponding one of said stages of said ***digital delay line*** and a second input coupled to a corresponding ***bit*** of said second ***spreading code;*** and
a summing device coupled to respective outputs of each of said N logic gates to provide a sum signal therefrom indicating a correlation between said second spreading code and said digital signal, wherein said second correlator further comprises means for deriving a data signal and a clock signal from said sum signal.	a summing device ***coupled*** to respective outputs of each of said N ***logic gates*** to provide a sum signal therefrom indicating a ***correlation*** between said second ***spreading code*** and said digital signal, wherein said second ***correlator*** further ***comprises means for deriving a data signal and a clock signal from said sum signal.***
Claim 16	**Claim 16**
16. A digital matched filter for a spread spectrum communication system comprises:	16. **A *digital matched filter for a spread spectrum communication system comprises:***
a digital delay line having a plurality of successive delay stages adapted to receive a digital signal and propagate said digital signal therethrough at a fixed rate;	a **digital delay line having a plurality of successive delay stages adapted to receive a digital signal and propagate said digital signal therethrough at a fixed rate:**
a plurality of correlators coupled to said digital delay line and adapted to correlate said digital signal to a plurality of different length spreading codes;	a ***plurality*** [*two or more*] of ***correlators coupled*** to said ***digital delay line*** and adapted to ***correlate*** said digital signal to a ***plurality*** of different length ***spreading codes:***
a multiplexer coupled to each of said plurality of correlators, said multiplexer selecting an output from one of said plurality of correlators that correlates to a respective one of said plurality of spreading codes, whereby said spreading codes are selected for transmitting at a data rate based on a desired	a ***multiplexer coupled*** to each of said ***plurality*** of ***correlators,*** said ***multiplexer*** selecting an output from one of said ***plurality*** of ***correlators*** that ***correlates*** to a respective one of said ***plurality*** of ***spreading codes,*** whereby said ***spreading codes*** are selected for transmitting at a ***data rate*** based on a desired level of data throughput and ***jamming resistance.***

level of data throughput and jamming resistance.	
Claim 17	**Claim 17**
17. The digital matched filter of claim 16, wherein each one of said plurality of correlators further comprises:	17. The ***digital matched filter*** of claim 16, wherein each one of said ***plurality*** of ***correlators*** further ***comprises:***
a plurality of logic gates each having a first input coupled to a corresponding one of said stages of said digital delay line and a second input coupled to a corresponding bit of a respective one of said plurality of spreading codes; and	a ***plurality*** of ***logic gates*** each having a first input ***coupled*** to a corresponding one of said stages of said ***digital delay line*** and a second input ***coupled*** to a corresponding ***bit*** of a respective one of said ***plurality*** of ***spreading codes;*** and
a summing device coupled to respective outputs of each of said plurality of logic gates to provide a sum of said outputs indicating a correlation between said respective one of said spreading codes and said digital signal.	a summing device ***coupled*** to respective outputs of each of said ***plurality*** of ***logic gates*** to provide a sum of said outputs indicating a ***correlation*** between said respective one of said ***spreading codes*** and said digital signal.
Claim 18	**Claim 18**
18. A digital matched filter for a spread spectrum communication system comprising:	18. ***A digital matched filter for a spread spectrum communication system comprising:***
a digital delay line having a plurality of successive delay stages adapted to receive a digital signal and propagate said digital signal therethrough at a fixed rate;	a ***digital delay line having a plurality of successive delay stages adapted to receive a digital signal and propagate said digital signal therethrough at a fixed rate:***
a plurality of correlators coupled to said digital delay line and adapted to correlate said digital signal to a plurality of different length spreading codes;	a ***plurality*** of ***correlators coupled*** to said ***digital delay line*** and adapted to ***correlate*** said digital signal to a ***plurality*** of different length ***spreading codes:***
a multiplexer coupled to each ot said plurality of correlators, said multiplexer selecting an output from one of said plurality of correlators that correlates to a respective one of said plurality of spreading codes, wherein each one of said plurality of correlators further comprises:	a ***multiplexer coupled*** to each of said ***plurality*** of ***correlators,*** said ***multiplexer*** selecting an output from one of said ***plurality*** of ***correlators*** that ***correlates*** to a respective one of said ***plurality*** of ***spreading codes,*** wherein each one of said ***plurality*** of ***correlators*** further ***comprises:***
a plurality of logic gates each having a first input coupled to a corresponding one of said stages of said digital delay line and a second input coupled to a corresponding bit of a respective one of said plurality of spreading codes; and	a ***plurality*** of ***logic gates*** each having a first input coupled to a corresponding one of said stages of said ***digital delay line*** and a second input coupled to a corresponding ***bit*** of a respective one of said ***plurality*** of ***spreading codes;*** and
a summing device coupled to respective outputs of each of said plurality of logic gates to provide a sum signal therefrom indicating a correlation between said respective one of said spreading codes and said digital signal, wherein said each one of said plurality of	a summing device ***coupled*** to respective outputs of each of said ***plurality*** of ***logic gates*** to provide a sum signal therefrom indicating a ***correlation*** between said respective one of said ***spreading codes*** and said digital signal, wherein said each one of said ***plurality*** of ***correlators*** further ***comprises means for deriving a data signal and a clock signal from said sum***

correlators further comprises means for deriving a data signal and a clock signal from said sum signal.	***signal.***
Claim 20	**Claim 20**
20. The digital matched filter of claim 17, wherein each one of said plurality of logic gates further comprises exclusive-OR logic gates.	20. The ***digital matched filter*** of claim 17, wherein each one of said ***plurality*** of ***logic gates*** further ***comprises exclusive-OR logic gates.***
Claim 21	**Claim 21**
21. The digital matched filter of claim 16 wherein said plurality of correlators further comprises at least two correlators, wherein a first one of said at least two correlators is adapted to correlate said digital signal to a first one of said plurality of spreading codes having a length M, and a second one of said at least two correlators is adapted to correlate said digital signal to a second one of said plurality of spreading codes having a length N.	21. The digital matched inter of claim 16 wherein said plurality of correlators further comprises at least two correlators, wherein a first one of said at least two correlators is adapted to correlate said digital signal to a first one of said plurality of spreading codes having a length M, and a second one of said at least two correlators is adapted to correlate said digital signal to a second one of said plurality of spreading codes having a length N.
Claim 22	**Claim 22**
22. In a spread spectrum communication system including a receiver adapted to receive a digital signal at a fixed chipping rate, a method for despreading the digital signal comprises:	22.In a ***spread spectrum communication system*** including a receiver adapted to receive a digital signal at a fixed ***chipping rate*** [*the rate at which information is received or transmitted as a sequence of data chips*], a method for ***despreading*** [*using a spreading code to recover information from the received signal*] the digital signal ***comprises:***
propagating the digital signal at the chipping rate through a digital delay line having a plurality of successive delay stages;	propagating the digital signal at the ***chipping rate*** through a ***digital delay line having a plurality of successive delay stages;***
correlating said digital signal in said digital delay line to a first spreading code having a length M and to a second spreading code having a length N, wherein N is less than M; and	***correlating*** said digital signal in said ***digital delay line*** to a first ***spreading code*** having a length M and to a second ***spreading code*** having a length N, wherein N is less than M; and
selecting an output signal based on a correlation with one of said first and second spreading codes, whereby said first spreading code is used to transmit at a lower data rate with higher jamming resistance, and said second spreading code is used to transmit at a higher data rate with lower jamming resistance.	selecting an output signal based on a ***correlation*** with one of said first and second ***spreading codes,*** whereby said first ***spreading code*** is used to transmit at a lower ***data rate*** with higher ***jamming resistance,*** and said second ***spreading code*** is used to transmit at a higher ***data rate*** with lower ***jamming resistance.***
Claim 23	**Claim 23**
23. The method of claim 22, wherein said correlating step further comprises:	23. The method of claim 22, wherein said correlating step further ***comprises:***

comparing each respective data chip from a corresponding one of said delay stages of said digital delay line to corresponding chips of said first and second spreading codes; and	comparing each respective ***data chip*** [*the smallest element in a spread spectrum information signal*] from a corresponding one of said delay stages of said ***digital delay line*** to corresponding chips of said first and second ***spreading codes:*** and
providing a sum value of each said comparison indicating a degree of correlation between said first spreading code and said digital signal and between said second spreading code and said digital signal.	providing a sum value of each said comparison indicating a degree of ***correlation*** between said first ***spreading code*** and said digital signal and between said second ***spreading code*** and said digital signal.
Claim 24	**Claim 24**
24. In a spread spectrum communication system including a receiver adapted to receive a digital signal at a fixed chipping rate, a method for despreading the digital signal comprises:	24. In a ***spread spectrum communication system*** including a receiver adapted to receive a digital signal at a fixed ***chipping rate,*** a method for ***despreading*** the digital signal ***comprises:***
propagating the digital signal at the chipping rate through a digital delay line having a plurality of successive delay stages;	propagating the digital signal at the ***chipping rate*** through a ***digital delay line having a plurality of successive delay stages:***
correlating said digital signal in said digital delay line to a first spreading code having a length M and to a second spreading code having a length N, wherein N is less than M; and	***correlating*** said digital signal in said ***digital delay line*** to a first ***spreading code*** having a length M and to a second ***spreading code*** having a length N, wherein N is less than M; and
selecting an output signal based on a correlation with one of said first and second spreading codes, wherein said correlating step further comprises:	selecting an output signal based on a ***correlation*** with one of said first and second ***spreading codes,*** wherein said correlating step further ***comprises:***
comparing each respective data chip from a corresponding one of said delay stages of said digital delay line to corresponding chips of said first and second spreading codes;	comparing each respective ***data chip*** from a corresponding one of said delay stages of said ***digital delay line*** to corresponding chips of said first and second ***spreading codes:***
providing a sum value of each said comparison indicating a degree of correlation between said first spreading code and said digital signal and between said second spreading code and said digital signal; and	providing a sum value of each said comparison indicating a degree of ***correlation*** between said first ***spreading code*** and said digital signal and between said second ***spreading code*** and said digital signal; and
deriving a respective data signal and clock signal from each said sum value.	deriving a respective data signal and clock signal from each said sum value.
Claim 26	**Claim 26**
26. The method of claim 22, wherein said correlating step is performed at a rate that is at least double said chipping rate.	26. The method of claim 22, wherein said correlating step is performed at a rate that is at least double said ***chipping rate.***

EXHIBIT B

UNITED STATES PATENT NUMBER 5.946.344-GLOSSARY OF TERMS

TERM	***DEFINITION***
bit	a character used to represent one of two digits in a system having two possible states, e.g., high or low, on or off, one or zero, + or-true or false, etc.
chipping rate	the rate at which information is received or transmitted as a sequence of data chips
comprises	includes but is not limited to
correlate	to compare two signals to determine the extent to which they agree or disagree
correlating	See definition of "correlate"
correlation	See definition of "correlate"
correlator	device which is capable of comparing two signals to determine the extent to which they agree or disagree
coupled	operatively connected
data chip	the smallest element in a spread spectrum information signal
data rate	amount of factual information per unit of time
despreading	using a spreading code to recover information from the received signal
digital delay line having a plurality of successive delay stages adapted to receive a digital signal and propagate said digital signal therethrough at a fixed rate	a device that moves digital input values through successive storage locations at a fixed rate. The digital values are delayed by being held in each storage location
digital delay line	See definition of " ***digital delay line having a plurality of successive delay stages adapted to receive a digital signal and propagate said digital signal therethrough at a fixed rate*** "
digital matched filter for a spread spectrum communication system	a detector that recovers an original digital information signal that was spread over a wide band of frequencies
exclusive-OR logic gates	logic gates whose outputs are true if either one of their respective inputs, but not both inputs, is true
jamming resistance	resistance to interfering and/or noise-like signals
logic gates	basic electrical building blocks where the state of a logic gate's output is determined by the states of its inputs
means for deriving a data signal and a clock signal from said sum signal	**This is a means-plus-function limitation.** The function is deriving a data signal and a clock signal from said sum signal. The corresponding structure is a tracking and bit synchronization logic unit and equivalents thereof.
multiplexer	a device that selects one of its inputs to provide an output
plurality	two or more
spreading code	a predetermined length sequence of chips that is used to modulate or 'spread' the signal before it is sent and that is used to demodulate or despread the signal after it is received
spread spectrum communication system	See definition of " ***digital matched filter for a spread spectrum communication system*** "

FN1. All terms appearing in bold face type and underlined have been construed by the court and appear with their definitions in the glossary in Exhibit B. The definition for each construed term appears in italics after its first use in the patent.

S.D.Cal.,2006.
Qualcomm Inc. v. Broadcom Corp.