United States District Court,
S.D. California.

HEWLETT-PACKARD DEVELOPMENT COMPANY, L.P,
Plaintiff.
v.
GATEWAY, INC,
Defendant.
Gateway, Inc,
Counterclaim-Plaintiff.
v.
Hewlett-Packard Development Company, L.P., Hewlett-Packard Company and Compaq Information Technologies Group, L.P,
Counterclaim-Defendants.
Intel Corp,
Intervenor.

Civil No. 04CV0613-B(LSP)

Jan. 12, 2006.

John Allcock, DLA Piper US, San Diego, CA, for Plaintiff/Counterclaim-Defendants.

Darryl J. Adams, Dean M. Munyon, James D. Smith, Wayne Harding, Dewey Ballantine, Austin, TX, Jonathan D. Baker, Dechert LLP, Mountain View, CA, W. Bryan Farney, Dechert LLP, Austin, TX, for Defendant.

CLAIM CONSTRUCTION ORDER FOR UNITED STATES PATENT NUMBER 5,381,530

RUDI M. BREWSTER**, Senior District Judge.**

Pursuant to Markman v. Westview Instruments, Inc., 517 U.S. 370, 116 S.Ct. 1384, 134 L.Ed.2d 577 (1996), on November 3 and 10, 2005, the Court conducted a Markman hearing in the above-titled patent infringement action regarding construction of the disputed claim terms for U.S. Patent Number 5,381,530 ("the '530 patent"). Plaintiff Hewlett-Packard Development Company, L.P. ("HP") was represented by the law firm of DLA Piper Rudnick Gray Cary U.S. LLP, Defendant Gateway, Inc. ("Gateway") was represented by the law firm of Dewey Ballantine LLP, and Intervenor Intel Corporation ("Intel") was represented by the law firm of Weil, Gotshal & Manges LLP.

At the Markman hearing, the Court, with the assistance of the parties, analyzed the claim terms in order to prepare jury instructions interpreting the pertinent claims at issue in the '530 patent. Additionally, the Court prepared a case glossary for terms found in the claims and the specification for the '530 patent considered to be technical in nature which a jury of laypersons might not understand clearly without specific definition.

After careful consideration of the parties' arguments and the applicable statutes and case law, the Court **HEREBY CONSTRUES** the claims in dispute in the '530 patent and **ISSUES** the relevant jury instructions as written in Exhibit A, attached hereto. Further, the Court **HEREBY DEFINES** all pertinent technical terms as written in Exhibit B, attached hereto.

IT IS SO ORDERED.

EXHIBIT A FN1

UNITED STATES PATENT NUMBER 5,381.530-CLAIM CHART

VERBATIM CLAIM LANGUAGE	**COURT'S CONSTRUCTION**
Claim 1	
1. A method for filtering input commands directed to a controller operating using a series of software commands responsive to input commands, said controller accessed by a microprocessor, said input commands intended to direct said controller to produce system control signals in response to said input commands from said microprocessor, comprising the steps of:	1. A method for filtering input commands directed to a controller ***operating using a series of software commands responsive to input commands*** [*the input commands cause the controller to execute a series of software instructions when the controller receives the input commands*], said controller accessed by a microprocessor, ***said input commands intended to direct said controller to produce system control signals*** [*the input commands intended by a program executed by the microprocessor to cause the controller to produce* ***system control signals] (system control signals*** [*signals used to direct the operation of, and capable of being understood by, any device that has to handle them in the system*]) in response to said input commands from said microprocessor, comprising the steps of:
monitoring signal lines coupled to output terminals of said microprocessor, said signal lines communicating input commands from the microprocessor;	monitoring signal lines coupled to output terminals of said microprocessor, said signal lines communicating input commands from the microprocessor;
processing a selected input command using a logic device; and	processing a selected input command using a ***logic device*** [*a programmable device for performing specific logic functions*]; and
producing an output signal from said logic device corresponding to said selected input command, as said system control signal, and in replacement of said system control signal directed to be produced by said controller, after a shorter delay from the. time said monitoring step detects said selected input command than the delay if said controller operated using a series of software commands responsive to said selected input command.	***producing an output signal from said logic device corresponding to said selected input command, as said system control signal, and in replacement of said system control signal directed to be produced by said controller,*** [*the* ***logic device*** *generating the* ***system control signal*** *the controller would have generated if the controller had initially received the selected input command*] after a shorter delay from the time said monitoring step detects said selected input command than the delay if said controller ***operated using a series of software commands responsive to said selected input command*** [*the selected input command causes the controller to execute a series of software instructions when the controller receives the selected input command*].
Claim 2	
2. The method of claim 1, further	2. The method of claim 1, further comprising:

comprising:	
blocking a write command signal from being applied to said controller for said selected input command.	blocking a write command signal from being applied to said controller for said selected input command,
Claim 3	
3. The method of claim 2, wherein said logic device has an input coupled to receive said write command signal, and has an output for presenting said write command signal to said controller; and	3. The method of claim 2, wherein said ***logic device*** has an input coupled to receive said write command signal, and has an output for presenting said write command signal to said controller; and
wherein said blocking step is performed by said logic device not presenting said write command signal to said controller responsive to receiving said selected input command.	wherein said blocking step is performed by said ***logic device*** not presenting said write command signal to said controller responsive to receiving said selected input command.
Claim 4	
4. The method of claim 1, wherein said logic device is a separate integrated circuit from said controller.	4. The method of claim 1, wherein said ***logic device*** is a separate ***integrated circuit*** [*a small piece of semiconductive material that contains interconnected miniaturized electronic circuits, often referred to as a "chip"*] from said controller.
Claim 5	
5. The method of claim 1, wherein said system control signal corresponds to an address bit masking signal.	5. The method of claim 1, wherein said ***system control signal*** corresponds to an address bit masking signal.
Claim 6	
6. The method of claim 1, wherein said system control signal corresponds to a microprocessor reset signal.	6. The method of claim 1, wherein said ***system control signal*** corresponds to a ***microprocessor reset signal*** [*a signal that causes the microprocessor to return to the state it would be in if the power were turned off and then on again*].
Claim 7	
7. The method of claim 1, wherein said controller is of the 8042 type.	7. The method of claim 1, wherein said controller is ***of the 8042 type*** [*an INTEL 8042 keyboard controller*].
Claim 8	
8. A method of controlling a computer system, said computer system comprising a microprocessor having real and protected mode operation capabilities and a controller for operating in a programmed manner according to input commands produced by the microprocessor, said microprocessor coupled to signal lines for communicating the input commands to the controller, said	8. A method of controlling a computer system, said computer system comprising a microprocessor having real and protected mode operation capabilities and a controller ***for operating in a programmed manner according to input commands*** [*the input commands cause the controller to execute a series of programmable instructions when the controller receives the input commands*] produced by the microprocessor, said microprocessor coupled to signal lines for communicating the input commands to the controller, said method comprising the steps of:

method comprising the steps of:	
detecting a FORCE-A20 input command on the signal lines, said FORCE-A20 input command intended to direct the controller to produce a FORCE-A20 system control signal for use in masking address bit A20; and	detecting a ***FORCE-A20 input command*** [*a command initiating the FORCE-A20 function of causing the A20 line of the microprocessor to stay low] on the signal lines,* ***said FORCE-A20 input command intended to direct the controller to produce a FORCE-A20 system control signal*** [*the* ***FORCE-A20 input command*** *intended by a program executed by the microprocessor to cause the controller to produce a FORCE-A20* ***system control signal***] for use in masking address bit A20; and
responsive to said detecting step, producing the FORCE-A20 system control signal with circuitry coupled to the signal lines;	responsive to said detecting step, producing the FORCE-A20 ***system control signal*** with *circuitry* [*a programmable device for performing specific logic functions*] coupled to the signal lines;
wherein the propagation delay of the circuitry in producing the FORCE-A20 system control signal responsive to said detecting step is shorter than the delay of the controller operating in the programmed manner to the FORCE-A20 input command.	wherein the propagation delay of the ***circuitry*** in producing the FORCE-A20 ***system control signal*** responsive to said detecting step is shorter than the delay of the controller operating in the programmed manner to the ***FORCE-A20 input command.***
Claim 9	
9. The method of claim 8, further comprising:	9. The method of claim 8, further comprising:
blocking a write command signal from being applied to the controller responsive to said detecting step, so that said controller is rendered inoperable to produce the FORCE-A20 system control signal responsive to said FORCE-A20 input command.	blocking a write command signal from being applied to the controller responsive to said detecting step, so that said controller is rendered inoperable to produce the FORCE-A20 ***system control signal*** responsive to said ***FORCE-A20 input command.***
Claim 10	
10. The method of claim 9, wherein said circuitry has an input for receiving the write command signal, and has an output coupled to said controller for communicating the write command signal thereto; and	10. The method of claim 9, wherein said ***circuitry*** has an input for receiving the write command signal, and has an output coupled to said controller for communicating the write command signal thereto; and
wherein said blocking step is performed by said circuitry.	wherein said blocking step is performed by said ***circuitry.***
Claim 11	
11. The method of claim 8, wherein said circuitry is in a separate integrated circuit from that of said controller.	11. The method of claim 8, wherein said ***circuitry*** is in a separate ***integrated circuit*** from that of said controller.
Claim 12	
12. The method of claim 8, further	12. The method of claim 8, further comprising:

comprising:	
detecting a CPU-RESET input command on the signal lines, said CPU-RESET input command intended to direct the controller to produce a CPU-RESET system control signal for application to the microprocessor; and	detecting a ***CPU-RESET input command*** [*a command initiating the reset function of causing the microprocessor to return to the state it would be in if the power were turned off and then on again*] on the signal lines, ***said CPU-RESET input command intended to direct the controller to produce a CPU-RESET system control signal*** [*the* ***CPU-RESET input command*** *intended by a program executed by the microprocessor to cause the controller to produce a CPU-RESET* ***system control signal***] for application to the microprocessor; and
responsive to said step of detecting the CPU-RESET input command, producing the CPU-RESET system control signal with the circuitry.	responsive to said step of detecting the ***CPU-RESET input command,*** producing the CPU-RESET ***system control signal*** with the ***circuitry.***
Claim 13	
13. The method of claim 8, wherein the controller comprises a keyboard controller of the 8042 type.	13. The method of claim 8, wherein the controller comprises a keyboard controller ***of the 8042 type.***

Claim 14

14. A data processing system, comprising:	14. A data processing system, comprising:
a microprocessor of a type having the capability of operating in real mode and in protected mode, said microprocessor coupled to an address bus including an A20 address line, said microprocessor having the functional capability of forcing the A20 address line to a logic level responsive to a FORCE-A20 signal;	a microprocessor of a type having the capability of operating in real mode and in protected mode, said microprocessor coupled to an address bus including an A20 address line, said microprocessor having the functional capability of forcing the A20 address line to a logic level responsive to a FORCE-A20 signal;
a controller having inputs for receiving a set of input commands produced by said microprocessor intended to cause said controller to direct system operation in a programmed manner in response to said input commands, said set of input commands comprising a FORCE-A20 input command that is intended to generate the FORCE-A20 signal; and	a controller having inputs for receiving a set of input commands produced by said microprocessor ***intended to cause said controller to direct system operation in a programmed manner in response to said input commands, said set of input commands comprising a FORCE-A20 input command that is intended to generate the FORCE-A20 signal*** [*intended by a program executed by the microprocessor to cause the controller to direct system operation in a programmed manner, the input commands including a command intended by the program executed by the microprocessor to produce commands to generate the FORCE-A20 signal*]; and
circuitry, having inputs coupled to said microprocessor to receive input commands therefrom, for generating the FORCE-A20 signal responsive to receiving a FORCE-A20 input command from said microprocessor and in replacement of said controller	***circuitry,*** having inputs coupled to said microprocessor to receive input commands therefrom, ***for generating the FORCE-A20 signal responsive to receiving a FORCE-A20 input command from said microprocessor and in replacement of said controller generating the FORCE-A20 signal;*** [*in response to receiving a FORCE-A20 input command, generating the FORCE-A20 signal that the controller would have generated if the controller had initially received the*

generating the FORCE-A20 signal;	***FORCE-A20 input command***]
wherein said generating circuitry generates the FORCE-A20 signal responsive to the FORCE-A20 input command in a shorter time than the delay of said controller operating in the programmed manner responsive to the FORCE-A20 input command.	wherein said generating ***circuitry*** generates the FORCE-A20 signal responsive to the ***FORCE-A20 input command*** in a shorter time than the delay of ***said controller operating in the programmed manner responsive to the FORCE-A20 input command*** [*the controller executing a series of programmable instructions to produce the FORCE-A20 signal if the controller received the* ***FORCE-A20 input command***].
Claim 15	
15. The system of claim 14, wherein said generating circuitry is located in a separate integrated circuit from that of said controller.	15. The system of claim 14, wherein said generating ***circuitry*** is located in a separate ***integrated circuit*** from that of said controller.
Claim 16	
16. The system of claim 14, wherein said generating circuitry is also for blocking a write command signal from being applied to said controller for said FORCE-A20 input command.	16. The system of claim 14, wherein said generating ***circuitry*** is also for blocking a write command signal from being applied to said controller for said ***FORCE-A20 input command.***
Claim 17	
17. The system of claim 16, wherein said generating circuitry has an input for receiving a write command signal, and has an output coupled to said controller for presenting the write command signal thereto.	17. The system of claim 16, wherein said generating ***circuitry*** has an input for receiving a write command signal, and has an output coupled to said controller for presenting the write command signal thereto.
Claim 18	
18. The system of claim 14, wherein said microprocessor also has an input for receiving a CPU-RESET signal;	18. The system of claim 14, wherein said microprocessor also has an input for receiving a CPU-RESET signal;
wherein said set of input commands further comprises a CPU-RESET input command that is intended to generate the CPU-RESET signal; and	wherein said set of input commands further comprises a ***CPU-RESET input command*** that is intended to generate the CPU-RESET signal; and
wherein said generating circuitry is also for generating the CPU-RESET signal responsive to receiving the CPU-RESET input command from said microprocessor and in replacement of said controller generating the CPU-RESET signal.	wherein said generating ***circuitry*** is also for ***generating the CPU-RESET signal responsive to receiving the CPU-RESET input command from said microprocessor and in replacement of said controller generating the CPU-RESET signal*** [*in response to receiving the* ***CPU-RESET input command,*** *generating the CPU-RESET signal the controller would have generated if the controller had initially received the* ***CPU-RESET input command***].
Claim 19	
19. The system of claim 18, wherein said generating circuitry comprises a programmable logic array.	19. The system of claim 18, wherein said generating ***circuitry*** comprises a programmable logic array.
Claim 20	

20. The system of claim 18, wherein said generating circuitry comprises:	20. The system of claim 18, wherein said generating ***circuitry*** comprises:
a first programmable logic array for generating the FORCE-A20 signal responsive to receiving a FORCE-A20 input command from said microprocessor; and	a first programmable logic array for generating the FORCE-A20 signal responsive to receiving a ***FORCE-A20 input command*** from said microprocessor; and
a second programmable logic array for generating the CPU-RESET signal responsive to receiving a CPU-RESET input command from said microprocessor.	a second programmable logic array for generating the CPU-RESET signal responsive to receiving a ***CPU-RESET input command*** from said microprocessor.
Claim 21	
21. A method of controlling a computer system, said computer system comprising a microprocessor and a controller for operating in a programmed manner according to input commands produced by the microprocessor, said microprocessor coupled to signal lines for communicating the input commands to the controller, said method comprising the steps of:	21. A method of controlling a computer system, said computer system comprising a microprocessor and a controller ***for operating in a programmed manner according to input commands*** produced by the microprocessor, said microprocessor coupled to signal lines for communicating the input commands to the controller, said method comprising the steps of:
detecting a microprocessor reset input command on the signal lines, said microprocessor reset input command intended to direct the controller to produce a microprocessor reset system control signal for application to the microprocessor; and	detecting a ***microprocessor reset input command*** [*a command initiating the reset function of causing the microprocessor to return to the state it would be in if the power were turned off and then on again*] on the signal lines, ***said microprocessor reset input command intended to direct the controller to produce a microprocessor reset system control signal*** [*the* ***microprocessor reset input command*** *intended by a program executed by the microprocessor to cause the controller to produce a* ***microprocessor reset system control signal***] for application to the microprocessor; and
responsive to said detecting step, producing the microprocessor reset system control signal with circuitry coupled to the signal lines and to the microprocessor;	responsive to said detecting step, producing the ***microprocessor reset system control signal*** [*a* ***system control signal*** *that causes the microprocessor to return to the state it would be in if the power were turned off and then on again*] with ***circuitry*** coupled to the signal lines and to the microprocessor;
wherein the propagation delay of the circuitry in producing the microprocessor reset system control signal responsive to said detecting step is shorter than the delay of the controller operating in the programmed manner to the microprocessor reset input command.	wherein the propagation delay of the ***circuitry*** in producing the ***microprocessor reset system control signal*** responsive to said detecting step is shorter than the delay of the controller operating in the programmed manner to the ***microprocessor reset input command.***
Claim 22	

22. The method of claim 21, further comprising:	22. The method of claim 21, further ***comprising:***
blocking a write command signal from being applied to the controller responsive to said detecting step, so that said controller is rendered inoperable to produce the microprocessor reset system control signal responsive to said microprocessor reset-input command.	blocking a write command signal from being applied to the controller responsive to said detecting step, so that said controller is rendered inoperable to produce the ***microprocessor reset system control signal*** responsive to said ***microprocessor reset input command.***
Claim 23	
23. The method of claim 22, wherein said circuitry has an input for receiving the write command signal, and has an output coupled to said controller for communicating the write command signal thereto; and	23. The method of claim 22, wherein said ***circuitry*** has an input for receiving the write command signal, and has an output coupled to said controller for communicating the write command signal thereto; and
wherein said blocking step is performed by said circuitry.	wherein said blocking step is performed by said ***circuitry.***
Claim 24	
24. The method of claim 21, wherein said circuitry is in a separate integrated circuit from that of said controller.	24. The method of claim 21, wherein said ***circuitry*** is in a separate ***integrated circuit*** from that of said controller.
Claim 25	
25. The method of claim 21, wherein the controller comprises a keyboard controller of the 8042 type.	25. The method of claim 21, wherein the controller comprises a keyboard controller ***of the 8042 type.***
Claim 26	
26. A data processing system, comprising:	26. A data processing system, ***comprising:***
a microprocessor having an input for receiving a microprocessor reset signal;	a microprocessor having an input for receiving a ***microprocessor reset signal:***
a controller having inputs for receiving a set of controller input commands produced by said microprocessor intended to cause said controller to direct system operation in a programmed manner in response to said controller input commands, said set of input commands comprising a microprocessor reset input command that is intended to generate the microprocessor reset signal;	a controller having inputs for receiving a set of controller input commands produced by said microprocessor ***intended to cause said controller to direct system operation in a programmed manner in response to said controller input commands, said set of input commands comprising a microprocessor reset input command that is intended to generate the microprocessor reset signal;*** [*intended by a program executed by the microprocessor to cause the controller to direct system operation in a programmed manner, the input commands including a* ***microprocessor reset input command*** *intended by the program executed by the microprocessor to produce commands to generate the* ***microprocessor reset signal***]

circuitry, having inputs coupled to said microprocessor to receive input commands therefrom, for generating the microprocessor reset signal responsive to receiving a microprocessor reset input command from said microprocessor and in replacement of said controller generating the microprocessor reset signal;	***circuitry,*** having inputs coupled to said microprocessor to receive input commands therefrom, for ***generating the microprocessor reset signal responsive to receiving a microprocessor reset input command from said microprocessor and in replacement of said controller generating the microprocessor reset signal;*** [*in response to receiving a* ***microprocessor reset input command,*** *generating the* ***microprocessor reset signal*** *that the controller would have generated if the controller had initially received the* ***microprocessor reset input command***]
wherein said generating circuitry generates the microprocessor reset signal responsive to the microprocessor reset input command in a shorter time than the delay of said controller operating in the programmed manner responsive to the microprocessor reset input command.	wherein said generating ***circuitry*** generates the ***microprocessor reset signal*** responsive to the ***microprocessor reset input command*** in a shorter time than the delay of ***said controller operating in the programmed manner responsive to the microprocessor reset input command.*** [*the controller executing a series of programmable instructions to produce the* ***microprocessor reset signal*** *if the controller received the* ***microprocessor reset input command***]
Claim 27	
27. The system of claim 26, wherein said generating circuitry is located in a separate integrated circuit from that of said controller.	27. The system of claim 26, wherein said generating ***circuitry*** is located in a separate ***integrated circuit*** from that of said controller.
Claim 28	
28. The system of claim 26, wherein said generating circuitry is also for blocking a write command signal from being applied to said controller for said microprocessor reset input command.	28. The system of claim 26, wherein said generating ***circuitry*** is also for blocking a write command signal from being applied to said controller for said ***microprocessor reset input command.***
Claim 29	
29. The system of claim 28, wherein said generating circuitry has an input for receiving a write command signal, and has an output coupled to said controller for presenting the write command signal thereto.	29. The system of claim 28, wherein said generating ***circuitry*** has an input for receiving a write command signal, and has an output coupled to said controller for presenting the write command signal thereto.

EXHIBIT B

UNITED STATES PATENT NUMBER 5.381.530-GLOSSARY OF TERMS

TERM	*DEFINITION*
Circuitry	a programmable device for performing specific logic

	functions
CPU-RESET input command	a command initiating the reset function of causing the microprocessor to return to the state it would be in if the power were turned off and then on again
For operating in a programmed manner according to input commands	the input commands cause the controller to execute a series of programmable instructions when the controller receives the input commands
FORCE-A20 input command	a command initiating the Force-A20 function of causing the A20 line of the microprocessor to stay low
Generating the CPU-RESET signal responsive to receiving the CPU-RESET input command from said microprocessor and in replacement of said controller generating the CPU-RESET signal	in response to receiving the CPU-RESET input command, generating the CPU-RESET signal the controller would have generated if the controller had initially received the CPU-RESET input command
Generating the FORCE-A20 signal responsive to receiving a FORCE-A20 input command from said microprocessor and in replacement of said controller generating the FORCE-A20 signal	in response to receiving a FORCE-A20 input command, generating the FORCE-A20 signal that the controller would have generated if the controller had initially received the FORCE-A20 input command
Generating the microprocessor reset signal responsive to receiving a microprocessor reset input command from said microprocessor and in replacement of said controller generating the microprocessor reset signal	in response to receiving a microprocessor reset input command, generating the microprocessor reset signal that the controller would have generated if the controller had initially received the microprocessor reset input command
Integrated circuit	a small piece of semiconductive material that contains interconnected miniaturized electronic circuits, often referred to as a "chip"
Intended to cause said controller to direct system operation in a programmed manner in response to said input commands, said set of input commands comprising a FORCE-A20 input command that is intended to generate the FORCE-A20 signal	intended by a program executed by the microprocessor to cause the controller to direct system operation in a programmed manner, the input commands including a command intended by the program executed by the microprocessor to produce commands to generate the FORCE-A20 signal
Intended to cause said controller to direct system operation in a programmed manner in	intended by a program executed by the microprocessor to cause the controller to direct system operation in a

response to said controller input commands, said set of input commands comprising a microprocessor reset input command that is intended to generate the microprocessor reset signal	programmed manner, the input commands including a microprocessor reset input command intended by the program executed by the microprocessor to produce commands to generate the microprocessor reset signal
Logic device	a programmable device for performing specific logic functions
Microprocessor reset input command	a command initiating the reset function of causing the microprocessor to return to the state it would be in if the power were turned off and then on again
Microprocessor reset signal	a signal that causes the microprocessor to return to the state it would be in if the power were turned off and then on again
Of the 8042 type	an INTEL 8042 keyboard controller
Operated using a series of software commands responsive to said selected input command	the selected input command causes the controller to execute a series of software instructions when the controller receives the selected input command
Operating using a series of software commands responsive to input commands	the input commands cause the controller to execute a series of software instructions when the controller receives the input commands
Producing an output signal from said logic device corresponding to said selected input command, as said system control signal, and in replacement of said system control signal directed to be produced by said controller	the logic device generating the system control signal the controller would have generated if the controller had initially received the selected input command
Said controller operating in the programmed manner responsive to the microprocessor reset input command	the controller executing a series of programmable instructions to produce the microprocessor reset signal if the controller received the microprocessor reset input command
Said controller operating in the programmed manner responsive to the FORCE-A20 input command	the controller executing a series of programmable instructions to produce the FORCE-A20 signal if the controller received the FORCE-A20 input command
Said CPU-RESET input command intended to direct the controller to produce a CPU-	the CPU-RESET input command intended by a program executed by the microprocessor to cause the

RESET system control signal	controller to produce a CPU-RESET system control signal
Said FORCE-A20 input command intended to direct the controller to produce a FORCE-A20 system control signal	the FORCE-A20 input command intended by a program executed by the microprocessor to cause the controller to produce a FORCE-A20 system control signal
Said input commands intended to direct said controller to produce system control signals	the input commands intended by a program executed by the microprocessor to cause the controller to produce system control signals
Said microprocessor reset input command intended to direct the controller to produce a microprocessor reset system control signal	the microprocessor reset input command intended by a program executed by the microprocessor to cause the controller to produce a microprocessor reset system control signal
System control signals	signals used to direct the operation of, and capable of being understood by, any device that has to handle them in the system

FN1. All terms appearing in bold face type and underlined have been construed by the court and appear with their definitions in the glossary in Exhibit B. The definition for each construed term appears in italics after its first use in the patent.

S.D.Cal.,2006.
Hewlett-Packard Development Co., L.P. v. Gateway, Inc.