United States District Court,
N.D. California.

ZORAN CORPORATION and Oak Technology, Inc,
Plaintiffs.
v.
MEDIATEK, INC., Mintek Digital, Inc., Asustek Computer, Inc., Lite-On Information Technology Corp., Teac Corporation, Teac America, Inc., Terapin Technology Pte., Ltd. Corporation and Teraoptix L.P. d/b/a Terapin Technology,
Defendants.

No. C-04-02619 RMW, C-04-04609 RMW

Sept. 9, 2005.

James C. Otteson, Lisa G. McFall, Michael A. Ladra, for Defendants.

Gerald T. Sekimura, John Allcock, Mark Fowler, Thomas A. Burg, William G. Goldman, for Plaintiffs.

CLAIM CONSTRUCTION ORDER REGARDING U.S PATENT NOS. 6,584,527 **AND** 6,546,440

WHYTE**, J.**

[Re: Docket No. 236]

At issue is the construction of disputed terms used in two patents descending from a single patent application, U.S. Patent Appl. No. 08/673,327 ("the '327 application"). The two patents are U.S. Patent No. 6,584,527 ("the '527 patent") and U.S. Patent No. 6,546,440 ("the '440 patent). Plaintiffs and defendants briefed the issues and argued their respective positions at a claim construction hearing on August 22-23, 2005. The court has read the moving and responding papers, including the patents-in-suit and the relevant prosecution history, considered the arguments of counsel, and now construes the disputed terms in the claims. FN1

FN1. The parties dispute other terms in the '527 and '440 patents. This order addresses only those limitations deemed dispositive by the parties and argued at the claim construction hearing.

I. BACKGROUND

A. Factual Background

Plaintiffs Zoran and Oak are co-owners by assignment of several patents relating to controllers for optical disk drives capable of playing both CDs and DVDs. The controller chips at issue are generally incorporated into the circuit boards of optical disk storage devices; the circuit boards can then be incorporated into

standalone DVD players and recorders or CD/DVD players and recorders that are installed in personal computers. Three of these patents are at issue in this case. This order construes claims in the two of those patents, both of which share a common lineage to the '327 application: the '527 patent and the '440 patent.

The '527 patent which issued on June 24, 2003, is a continuation of patent application 08/264,361, filed June 22, 1994, which issued as U.S. Patent No. 5,581,715 ("the '715 patent"). The '440 patent which issued on April 8, 2003 is a continuation of the '527 patent. The '527 and '440 patents particularly deal with an improved CD-ROM drive controller which provides faster and simplified data communication

Of the 35 claims in the '440 patent, only claims 1 and 14 are at issue in the instant litigation. Both are independent claims. '440 patent, 28:32-29:4; 29:47-30:11. All three claims of the '527 patent are at issue. '527 patent 28 :29-30 :12.

B. Legal Background

The '715 patent, which issued from the parent application of the '327 application, was previously asserted by plaintiff Oak against defendant MediaTek and others before the International Trade Commission. The ITC construed the terms of the '715 patent and ultimately concluded that the products accused of infringing the '715 patent were in fact non-infringing. The non-infringement determination was appealed to the Federal Circuit, which affirmed the ITC's claim construction and finding of no infringement. Before this court, Oak filed an action based upon breach of contract and fraud to which MediaTek and its co-defendant United Media Corporation ("UMC") asserted certain defenses based on patent law. As a result, this court construed two disputed claim terms for the '715 patent: "host interface means" and "digital signal processor interface."

Plaintiffs subsequently initiated an action in the ITC asserting the three patents at issue in this action against allegedly infringing products produced by MediaTek and other defendants in this action, Investigation No. 337-TA-506 ("the '506 investigation"). Plaintiffs asserted the same claims as are asserted here. FN2 The parties, led by Zoran for plaintiffs and MediaTek for defendants, engaged in a two-week trial before Administrative Law Judge Luckern at the ITC. He issued his Final Initial and Recommended Determinations in May 2005, which includes his construction of many of the terms at issue and his infringement, invalidity, and enforceability analysis. FN3

FN2. '736 patent: claims 1 and 7; '527 patent: claims 1-3; '440 patent: claims 1 and 14.

FN3. Judge Luckern determined all asserted claims were valid and the patents were enforceable. He also determined that the accused products infringed claim 3 of the '527 patent, but did not infringe any of the other asserted claims (1, 2 of the '527 patent; 1, 7 of the '726 patent; 1, 14 of the '440 patent).

C. Defendants' Sur-Reply

Five days before the claim construction hearing and mere hours before the Friday case management conference to discuss that hearing, defendants filed a request for leave to file a sur-reply to plaintiffs' reply claim construction briefing under Civil Local Rule 7-11, contending that the sur-reply was necessary to respond to arguments raised by plaintiffs in their reply brief. Plaintiffs' arguments were based on recently-decided Federal Circuit authority, specifically, Phillips v. AWH Corp., 415 F.3d 1303 (Fed.Cir. July 12, 2005); Salazar v. Proctor and Gamble Co., 414 F.3d 1342 (Fed.Cir. July 8, 2005); and NTP, Inc. v. Research

in Motion, Ltd ., 418 F.3d 1282, 2005 WL 1806123 (Fed.Cir. Aug. 2, 2005). FN4 The court granted defendants' request in part but permitted plaintiffs to file a response to the sur-reply. Because the timing of the request to file the sur-reply did not permit plaintiffs to respond until after the claim construction hearing, the court did not permit defendants to raise arguments based on the sur-reply at the hearing. The court has now reviewed the sur-reply and response. It does not find that further oral argument on the points raised in the additional briefing is necessary. It will note what impact, if any, the supplemental briefing had on its claim construction determinations as appropriate.

FN4. Plaintiffs filed their opening brief on June 14, 2005; defendants filed their responsive claim construction brief on July 18, 2005; and plaintiffs filed a reply brief on August 8, 2005.

II. ANALYSIS

The construction of patent claim terms is a matter of law for the court. Markman v. Westview Instruments, Inc., 517 U.S. 370, 372 (1996) ("*Markman II*"). "It is a bedrock principle of patent law that the claims of a patent define the invention to which the patentee is entitled the right to exclude." Innova/Pure Water, Inc. v. Safari Water Filtration Sys., 381 F.3d 1111, 1115 (Fed.Cir.2004). Because the two patents herein construed derive from the same parent application and share many common terms, the court must interpret the claims consistently across all asserted patents. NTP, 2005 WL 1806123. As a general rule, the claim language carries its ordinary and customary meaning. Toro Co. v. White Consol. Indus., Inc., 199 F.3d 1295, 1299 (Fed.Cir.1999). The ordinary meaning of a term cannot, however, be construed in a vacuum; rather, a court "must look at the ordinary meaning in the context of the written description and the prosecution history." Medrad, Inc. v. MRI Devices Corp., 401 F.3d 1313, 1319 (Fed.Cir.2005). To ascertain the meaning of a claim term, the court refers to "those sources available to the public that show what a person of skill in the art would have understood disputed claim language to mean." Phillips v. AWH Corp., 415 F.3d 1303, 1314 (Fed.Cir.2005) (en banc). The court does so to "determine whether the inventor used any terms in a manner inconsistent with their ordinary meaning." Vitronics Corp. v. Conceptronics, Inc., 90 F.3d 1576, 1582 (Fed.Cir.1996). The sources include "the words of the claims themselves, the remainder of the specification, the prosecution history, and extrinsic evidence concerning relevant scientific principles, the meaning of technical terms, and the state of the art ." Phillips, 415 F.3d at 1314 (citing Innova, 381 F.3d at 1116).

The court begins with the language of the claims. PSC Computer Prods., Inc. v. Foxconn Int'l, 355 F.3d 1353, 1359 (Fed.Cir.2004). When considering the claim language, "the context in which a term is used in the asserted claim can be highly instructive." Phillips, 415 F.3d at 1314. The court may also consider the other claims of the patent, both asserted and unasserted. *Id*. For example, as claim terms are normally used consistently throughout a patent, the usage of a term in one claim may illuminate the meaning of the same term in other claims. *Id*. The court may also consider differences between claims to guide in understanding the meaning of particular claim terms. *Id*.

As the claims do not stand alone, they "must be read in view of the specification, of which they are a part." Phillips, 415 F.3d at 1315 (citing Markman v. Westview Instruments, 52 F.3d 967, 979 (Fed.Cir.1995)). "The construction that stays true to the claim language and most naturally aligns with the patent's description of the invention will be, in the end, the correct construction." Renishaw PLC v. Marposs Societa' per Azioni, 158 F.3d 1243, 1250 (Fed.Cir.1998). When the specification reveals a special definition given to a claim term by the patentee that differs from the meaning it would otherwise possess, the inventor's lexicography governs. Phillips, 415 F.3d at 1316 (citing CCS Fitness, Inc. v. Brunswick Corp., 288 F.3d

1359, 1366 (Fed.Cir.2002)). The specification may reveal an intentional disclaimer, or disavowal, of claim scope by the inventor. *Id*. (citing SciMed Life Sys., Inc. v. Advanced Cardiovascular Sys., Inc., 242 F.3d 1337, 1343-44 (Fed.Cir.2001)).

The Federal Circuit also reaffirmed the importance of the prosecution history. Phillips, 415 F.3d at 1317. The prosecution history represents an ongoing negotiation between the PTO and the applicant. *Id*. The prosecution history, like the specification, "provides evidence of how the PTO and the inventor understood the patent." *Id*. (citing Lemelson v. Gen. Mills, Inc., 968 F.2d 1202, 1206 (Fed.Cir.1992)). However, it is subject to inherent ambiguity because is represents the negotiation, rather than the final product of the negotiation, and is thus less useful than the specification. *Id*.

Extrinsic evidence "can shed useful light on the relevant art," but the Federal Circuit considers it "less significant than the intrinsic record in determining 'the legally operative meaning of claim language." ' *Id*. (citing C.R. Bard, Inc. v. U.S. Surgical Corp., 388 F.3d 858, 862 (Fed.Cir.2004)). "Extrinsic evidence may be useful to the court, but it is unlikely to result in a reliable interpretation of patent claim scope unless considered in the context of the intrinsic evidence." Id. at 1319. The Federal Circuit has held that it remains within the court's discretion to admit extrinsic evidence, provided the court keeps in mind the flaws inherent in such evidence. *Id*. FN5

FN5. The Federal Circuit noted the following deficiencies in extrinsic evidence: (1) extrinsic evidence is not part of the patent and does not have the virtue of being created at the time of patent prosecution for the purpose of explaining the patent's scope and meaning; (2) extrinsic publications may not be written by or for skilled artisans and therefore may not reflect the understanding of a person of skill in the field of the patent; (3) expert reports and testimony "is generated at the time of and for the purpose of litigation and thus can suffer from bias that is not present in intrinsic evidence"; and (4) the "universe of potential extrinsic evidence of some marginal relevance that could be brought to bear on any claim construction question" is vast and parties will naturally choose the pieces of extrinsic evidence most favorable to its cause, "leaving the court with the considerable task of filtering the useful extrinsic evidence from the fluff." Phillips, 415 F.3d at 1318.

In *Phillips,* the Federal Circuit clarified its position on the use of dictionaries as extrinsic evidence by reprioritizing their use with regard to the specification. Phillips, 415 F.3d at 1319-24. "District courts are authorized 'to rely on extrinsic evidence, which consists of all evidence external to the patent and prosecution history, including ... dictionaries' as one of many claim construction tools." Terlep v. Brinkmann Corp., 418 F .3d 1379, 2005 WL 1950186, (Fed.Cir.2005) (citing Phillips, 415 F.3d at 1317)). However, district courts must attach the appropriate weight to dictionary definitions. In particular, judges must consider extrinsic evidence such as dictionaries while keeping in mind that the specification is " 'the single best guide to the meaning of a disputed term,' and that the specification 'acts as a dictionary when it expressly defines terms used in the claims or when it defines terms by implication." ' Phillips, 415 F.3d at 1321 (citing Vitronics, 90 F.3d at 1582 and Irdeto Access, Inc. v. Echostar Satellite Corp., 383 F.3d 1295, 1300 (Fed.Cir.2004)). Attempting to determine whether one of skill in the art would read embodiments in the specification as the outer bounds of a claim term or exemplar is best done in the context of the patent-at-issue because doing so is "likely to capture the scope of the actual invention more accurately than either strictly limiting the scope of the claims to the embodiments disclosed in the specification or divorcing the claim language from the specification." Id. at 1324. The Federal Circuit emphasized that in undertaking this endeavor, "[t]he sequence of steps used by the judge in consulting various sources is not important; what

matters is for the court to attach the appropriate weight to be assigned to those sources in light of the statutes and policies that inform patent law." *Id*.

A. "Data Error Detection and Correction Circuitry"

1. Proposed Constructions

Plaintiffs argue that "data error detection and correction circuitry" should be construed to mean "any error detection and correction circuity." Defendants, on the other hand, assert that the term should be construed as "circuitry that first performs Reed-Solomon error correction, followed by error detection with a cyclic redundancy checker." There are three fundamental construction disputes between the parties: (1) whether the term implies any temporal requirements, (2) whether the error correction must be done using only Reed-Solomon error correction codes, and (3) whether error detection must be done with a cyclic redundancy checker. Plaintiffs contend that there is no sequence implied by the claim term; defendants argue that the vagueness of the term mandates reference to the specification, which clearly sets forth the sequence of operations performed by the "error detection and correction circuitry" and further requires error correction to be done according to the Reed-Solomon error correction codes and error detection to be done by a cyclic redundancy checker.

2. Claim Language and Prior Construction of Similar Terms

The term "data error detection and correction circuitry" appears in claims 1 and 2 of the '527 patent. The Federal Circuit construed "data error detection and correction means" as claimed in the '715 patent to require both Reed-Solomon error correction codes and error detection using a cyclic redundancy checker. Plaintiffs contend that, contrary to defendants' assertions otherwise, this construction is not warranted with regard to the "data error detection and correction circuitry" in claims 1 and 2 of the '527 patent. Plaintiffs illustrate the limitations set forth in the '715 patent claim term that are inappropriate to the '527 by setting the claims side-by-side and underlining the limitations they contend that defendants seek to impermissibly import:

'715 patent term	'527 patent term
"data error detection and correction means for correcting said assembled data, said detection and correction means including error correction circuitry for performing error correction on said assembled data and a *cyclic redundancy checker* for detecting errors in said assembled data *after* correction of said data by said correction circuitry for providing corrected data."	"data error detection and correction circuitry, said detection and correction circuitry including: error correction circuitry for performing error correction on data received from said interface and generating corrected data, and error detection circuitry for detecting errors in data prior to transmission to said host computer"

The court agrees that these limitations require different constructions. First, the Federal Circuit noted in affirming the ITC's construction requiring error correction before error detection, Reed-Solomon error correction codes, and the cyclic redundancy checker "that the plain language of the disputed limitation of claim I explicitly requires certain interactions between the 'error correction circuitry,' the 'cyclic redundancy checker' and 'said assembled data." ' Oak v. ITC, 248 F.3d 1316, 1325 (Fed.Cir.2001). FN6 In limiting the claim to a particular sequence of error correction and detection, the Federal Circuit appropriately relied upon the language in the '715 claim providing for the use of a cyclic redundancy checker to detect errors in the assembled data after the correction circuitry had provided corrected data. However, the Federal Circuit also recognized that "[t]he sequential limitation is imposed by the claim language itself, and the written description simply confirms this understanding." Id. at 1328-29. By contrast, the language at issue in the '527 patent utilizes no language requiring interactions between the components indicating sequential operation of the error correction and detection circuitry, except that errors must be detected prior to transmission to transmission to the host computer.

FN6. Notably, the Federal Circuit did not construe the "data error detection and correction means" as a means-plus-function claim under 35 U.S.C. s. 112 para. 6. The parties stated at oral argument that Oak and UMC had stipulated that this claim limitation was not to be construed as means-plus-function.

Defendants rely upon the Federal Circuit's statement that the intrinsic record of embodiments in the shared specification provides no discussion of " 'error detection and correction means' which do not operate in a straightforward sequential manner" and that "if such a disclosure existed, these embodiments would not be covered by the language selected by the claim drafter." Id. at 1329. However, there is little question claim drafter for the '527 patent chose different language. It is that language, not the claim language of the '715 patent, that this court must construe.

3. Specification

The specification discusses the "error detection and correction circuitry" in several places. The abstract of the '527 patent states that "an error correction code (ECC) data corrector, an error detection and correction (EDC) device employing cyclical redundancy checking techniques (EDC/CRC) ... are described." '527 patent, Abstract. The Summary of the Invention of the '527 patent specification discloses that

[t]he digital signal processor interface of the CDDC [compact disk drive controller] further comprises an error correction code circuit to perform error correction on said digital information. That error correction circuit could employ Reed-Solomon codes. The digital signal processor interface of the CDDC further comprises a cyclic redundancy checker for detecting errors in the digital information after correction of the digital information by the error code correction circuit.

'527 patent 3 :20-28. The patent specification describes the error correction and detection circuitry referring to Fig. 2:

The error correction circuitry would first perform Reed-Solomon error correction on each block of data. Reed-Solomon codes are random single- or multiplesymbol error correcting codes operation on symbols which are elements of a finite field. All encoding, decoding, and correction computations are performed in the field. Then, a cyclic redundancy check of the corrected data would be performed. Since each codeword contains two parity bytes the drive controller of this invention can correct one error in each codeword.

These ECC and EDC/CRC circuits are commonly available as hardware used in many other applications. The host control allows the corrected data to be transferred from the RAM to the host.

Id. at 6:26-41. The parties do not dispute that the specification only expressly discloses one method of error correction and detection in the preferred embodiment. In this method, the error correction is implemented using the Reed-Solomon error codes and is performed prior to error detection (which is implemented by way of a cyclic redundancy checker). The court agrees with the Federal Circuit that there is no specific discussion of error code detection and correction that operates in a different sequence than that suggested by the defendants. However, "although the specification often describes very specific embodiments of the invention, [the Federal Circuit has] repeatedly warned against confining the claims to those embodiments." Phillips, 415 F.3d at 1323 (citing Liebel-Flarsheim Co. v. Medrad, Inc., 358 F.3d 898, 906-08 (Fed.Cir.2004); also citing Nazomi Communications, Inc. v. ARM Holdings, PLC, 403 F.3d 1364, 1369 (Fed.Cir.2005) for the proposition that claims may embrace "different subject matter than is illustrated in the specific embodiments in the specification").

In addition, the specification, by stating that "error correction circuit *could* employ Reed-Solomon codes," *id*. at 3:22-23 (emphasis added), makes it reasonably clear that the Reed-Solomon is one option for error correction, but not the only one. Furthermore, as pointed out by plaintiffs at the claim construction hearing and in their response to defendants' sur-reply, the specification cites a text, *Practical Error Correction Design for Engineers,* which describes various error correction codes and techniques. Plaintiffs attach excerpts of this text, published in 1991, to their declaration in support of their response to defendants' sur-reply. Reed-Solomon is one of the techniques, indeed, the preferred technique, disclosed for error correction and detection for optical drives but there are others. *See* Neil Glover & Trent Dudley, *Practical Error Correction Design for Engineers* (2d ed. Cirrus Logic 1991), Decl. of William Goldman Supp. Resp. Sur-reply, Ex. A. at pp. 158, 272, 276-77.

Similarly, the discussion of a "cyclic redundancy checker" in the patent specification indicates that a cyclic redundancy checker may not always be required in an error code detection and correction system. As with Reed-Solomon codes, the specification indicates that a cyclic redundancy checker in an alternate embodiment. The specification states that the "digital processor interface of the CDDC further comprises a cyclic redundancy checker for checking errors in the digital information after correction of the digital information by the error correction code circuit." '527 patent at 3:25. This indicates that the cyclic redundancy checker need not necessarily be present nor need error detection be performed in a particular sequence with respect to error correction. The "further comprises" language also demonstrates that the specification is disclosing an embodiment rather than establishing the outer boundary of claim scope.

4. Prosecution History

The prosecution history of the '527 patent includes exchanges regarding the "error detection and correction circuitry." Applicants filed original claim 25, which issued as claim 1, as a preliminary amendment to a continuation application under 37 C.F.R. 1.62. The relevant portion of original claim 25 read:

data error detection and correction circuitry, said detection and correction circuitry including error correction circuitry for performing error correction on said data received from said interface and generating corrected data therefrom, and a cyclic redundancy checker for detecting errors in said data or in said corrected data

'527 Prosecution History (" '527 PH"), Schwartz Decl., Ex. C at ZC12000. The preliminary amendment also included claim 30, dependent upon original claim 25 which read, "[t]he drive controller of claim 25, wherein said error correction circuitry performs Reed-Solomon error correction on said data received from said interface." Id. at ZC001201.

On June 13, 2000, the applicants amended claim 25 in response to a January 13, 2000 office action. FN7 The amendment to claim 25 removed the cyclic redundancy checker limitation, replacing the words "a cyclic redundancy checker" with "error detection circuitry." The amendment also removed "or in said corrected data", replacing it with "prior to transmission to said computer." Id. at ZC001502. FN8 The accompanying comments read

FN7. The January 13, 2000 office action is found at ZC001229.

FN8. These amendments to original claim 25 modified the language to that with which it ultimately issued as claim 1 to the '527 patent:
data error detection and correction circuitry, said detection and correction circuitry including: error correction circuitry for performing error correction on said data received from said interface and generating corrected data, and error detection circuitry for detecting errors in data prior to transmission to said host computer.

Applicant has also amended claim 25 to further clarify that with regard to the timing of error detection operations, it is only required that data errors be detected before the data is transferred to the host computer. Moreover, any kind of error detection circuitry may be employed, regardless of whether or not it uses a cyclical redundancy code or error detection codes other than a cyclical redundancy check code.
A notice of allowability was issued on the '327 application on December 4, 2000. Id. at ZC001510. In the reasons for allowance issued with that notice, the examiner took official notice that

the claimed invention requires that the data errors must be detected and corrected before the data is transferred to the host computer and the error correction must occur before the data error detection. The Official position is that the scope of all the independent claims ... are interpreted in view of the embodiment disclosed in the specification. In particular, see Specification, page 8, lines 3-9 ... and page 9 after line 8....

Id. at ZC001511. He also noted with regard to error detection circuitry that

Applicant stated in the Remarks that "any kind of error detection circuitry may be employed, regardless of whether or not it uses a cyclical redundancy code or error detection codes other than a cyclical redundancy check code." Official notice is taken that the only kind of error detection circuitry disclosed in the Specification is a cyclical redundancy check (CRC) circuitry.... Official notice is taken that, at the time of the invention, the only one specific type of EDC-CRC commonly available as hardware used in many other applications was a linear feedback shift register.

Id. at ZC001512. Thereafter, applicants filed a continued prosecution application that included "comments on statements of reasons for allowance." In those comments, the applicants disagreed with the examiner's December 2000 statement for reasons of allowance, stating

The "Statement of Reasons for Allowance" relies upon a decision of the ITC ... that Applicant is currently appealing.... For the same reasons asserted by the Applicant in this appeal, the Applicant respectfully disagrees with the "Statement of Reasons for Allowance."

Id. at ZC001621. On August 7, 2001, the applicants filed original claim 35, which issued as claim 2 to the '527 patent. Along with that claim the applicants again addressed the December 4, 2000 notice of allowability, referring to the Federal Circuit's opinion in *ITC II:*

The claim language relied upon by the Federal Circuit is not present in the now pending claims and there is no basis for restricting these claims in this manner.... Applicant traverses paragraph 3 of the "Statement of Reasons for Allowance" because it inappropriately takes Official notice that "the claimed invention requires that the data errors must be detected and corrected before the data is transferred to the host computer and that the error correction must occur before the data error detection." ... Similarly, Applicant traverses paragraph 4 of the "Statement of Reasons for Allowance" because it also reads limitations of the specification into claim 25. In this regard, the Federal Circuit decision clearly based its decision on the language in the claims of U.S. Patent 5, 581,715, which language clearly is not present in the now pending claims of this application. As such, Applicant respectfully requests withdrawal of the "Statement of Reasons for Allowance" and reconsideration of the new pending claims.

Id. at ZC001741-43.

The examiner rejected claims 25 and 35 in an office action dated July 8, 2002. He based the rejection in part on obviousness under 35 U.S.C. s. 103(a) in light of the Yellow Book specification, stating "Based on 'Yellow Book' specification, one of ordinary skill in the art would recognize that the error correction process is performed before the error detection process." *Id*. at ZC001827. Applicants responded by stating, "With regard to claims 25 and 35, there is no limitation that 'the error correction process is performed before the error detection process'...." *Id*. at ZC001938. Plaintiffs argue that these broadening statements clarify the knowledge of one of skill in the art and demonstrate that they did not acquiesce to the examiner's statement regarding Reed-Solomon and cyclic redundancy checker being the only techniques known to one of skill in the art. Plaintiffs' '527 Reply Br. at 5. They argue that the inventors' traverse prevented any disavowal of claim scope. *Cf*. Salazar, 414 F.3d at 1347.

a. "Cyclic Redundancy Checker" Removed During Prosecution

When construing claims, courts may rely on unissued claims to determine the scope of a claim term. *Cf*. Lemelson v. TRW, Inc., 760 F.2d 1254, 1262 (Fed.Cir.1985). As evidence that defendants' attempt to require the "error detection and correction circuitry" use a cyclic redundancy checker is improper, plaintiffs point out that the limitation "cyclic redundancy checker" was removed during prosecution and replaced with "error detection circuitry." Hence, they contend that defendants' attempt to narrow their claim by substituting "cyclic redundancy checker" back into the claim for "error detection circuitry" impermissibly narrows a claim broadened during prosecution. U.S. v. Telectronics, Inc., 857 F.2d 778, 783 (Fed.Cir.1988) ("courts are not permitted to read 'back into the claims limitations which were originally there and were removed during prosecution of the application through the Patent Office." ').

b. Claim Differentiation

Plaintiffs also argue that the claim cannot be construed to require Reed-Solomon error correction because

the prosecution history demonstrates that pending claim 25 (now claim 1) was accompanied by pending dependent claim 30, which provided that error correction would be done via Reed-Solomon codes. According to plaintiffs, this indicates that claim 25 did not require Reed-Solomon correction, and likewise did not include a requirement that error correction precede error detection before the corrected data was transferred to the MPEG decoder. Long-established principles of claim differentiation support plaintiffs' contention. *Cf.* Wright Medical Technology, Inc. v. Osteonics Corp., 122 F.3d 1440, 1445 (Fed.Cir.1997) ("we must not interpret an independent claim in a way that is inconsistent with a claim which depends from it....").

c. Understanding of One of Skill in the Art

Defendants contend that the only method of error correction known to one of skill in the art as of the effective filing date of the patent application was Reed-Solomon correction. *See* Phillips, 415 F.3d at 1313 ("We have made clear, moreover, that the ordinary and customary meaning of a claim term is the meaning that the term would have to a person of ordinary skill in the art in question at the time of the invention, i.e., as of the effective filing date of the patent application."). They contend that this level of understanding at the time of filing was confirmed by the Federal Circuit in *Oak v. ITC,* and again by the examiner when he took official notice that Reed-Solomon and the cyclic redundancy checker were the only methods at the time of filing that were known to one of skill in the art for error correction and detection respectively. Thus, according to defendants, the only possible way to construe "error detection and correction circuitry" would require error correction by Reed-Solomon error code prior to error detection using a cyclic redundancy checker.

5. Jepson Claim Format

Their sur-reply, defendants contend, based loosely on *Phillips,* that the Jepson form of claim 3 of the '527 patent demonstrates that the error detection and correction circuitry requires the Reed-Solomon, cyclic redundancy checker, and temporal limitations. Notably, the "error detection and correction circuitry" limitation appears nowhere in claim 3. Instead, defendants contend that the term "optical drive controller," which appears in the preamble, requires error detection and correction circuitry according to the specification. Because the preamble of a Jepson claim defines structural limitations that are conventional or known, Rowe v. Dror, 112 F.3d 473, 479 (Fed.Cir.1997), defendants contend that the optical drive controller includes error detection and correction circuitry as would have been known in the art at the time the parent application was filed. Because they contend that the only such circuitry known in the art would have used Reed-Solomon and a cyclic redundancy checker, they assert that the form of claim 3 supports their construction of the "error detection and correction circuitry" limitation.

The court finds defendants' argument to be without merit. First, nothing in *Phillips* justifies the late assertion of defendants' Jepson argument. The argument is a relatively transparent attempt to advance a new claim construction theory on the eve of the claim construction hearing. Second, defendants' attempt to fix the knowledge of one of skill in the art with respect to a term that does not appear in the claim (error detection and correction circuitry) though a prior art term (optical drive controller) by asserting that the structure of the optical drive controller requires error detection and correction circuitry is an unwarranted stretch. Construing "error detection and correction circuitry" through the "optical drive controller" cited in the preamble of a Jepson claim by reference to the required element of a prior art optical drive controller is attenuated at best, particularly given that the term explicitly appears in claims 1 and 2 of the '527 patent. Third, as set forth above, plaintiffs have presented evidence that techniques other that Reed-Solomon where known by one of skill in the art at least as of 1991 when the second edition of *Practical Error Correction*

Design for Engineers was published.

6. Conclusion

The court declines to narrowly construe the term based on the understanding of one of skill in the art as set forth by the Federal Circuit in *Oak v. ITC* and by the examiner of the '527 patent in the examiner's notice. FN9 As set forth above, the claim language does not limit error detection and correction circuitry to using Reed-Solomon or a cyclic redundancy checker. The specification leaves open the possibility that Reed-Solomon is but one possible error correction method and that cyclic redundancy checker is one error detection method. Likewise, the indication in the specification that the error correction circuitry "further comprises" a cyclic redundancy checker indicates that error detection need be accomplished by a cyclic redundancy checker nor need it occur in any particular sequence in the error detection and correction subsystem. Further, during prosecution, the applicants clearly asserted that error correction and detection could be done either in the sequence disclosed or another sequence. The applicants stated that error detection and correction could be accomplished by any means, specifically challenging the PTO's "Statement for Reasons of Allowance" on the grounds that neither a cyclic redundancy checker nor error detection after correction were required. None of these assertions is at all ambiguous. Finally, plaintiffs have presented extrinsic evidence cited in the specification itself that corroborates that techniques for performing error correction with techniques other than Reed-Solomon may have been known (although potentially not employed) at the time the parent application was filed. Thus, the court finds "data error detection and correction circuitry" means, as plaintiffs contend, "any error detection and correction circuitry."

FN9. The court's decision on this matter does not necessarily mean the claim is valid. For example, claims having this limitation may suffer from enablement problems, but that is a separate inquiry. *See Phillips,* 415 F.3d at 1337 ("While we have acknowledged the maxim that claims should be construed to preserve their validity, we have not applied that principle broadly, and we have certainly not endorsed a regime in which validity analysis is a regular component of claim construction.") (citing Nazomi, 403 F.3d at 1368-69); *see also,* Nat'l Recovery Techs., Inc. v. Magnetic Separation Sys., Inc., 166 F.3d 1190, 1196 (Fed.Cir.1999) (separating the claim construction and enablement inquiry).

B. "Preclude from Accessing"

1. Proposed Constructions

The parties dispute the proper construction of "preclude from accessing." The claim language at issue is found in claims 1 and 14 the '440 patent. Claim 1 reads: "circuitry operable to alter said BSY bit ... to indicate said host computer is precluded from accessing said plurality of ATA command block register addresses"; claim 14 reads: "said status register including a BSY bit ... that indicates when access by said host computer to said ATA command block register addresses is precluded." FN10 Plaintiffs assert that the correct construction of these phrases is "the BSY bit indicates whether the host computer is permitted to access the command block registers"; defendants assert that "the BSY bit indicates when it is impossible for the host computer to access-i .e., read or write-the ATA command block registers." Defendants' '527 Br. at 16; Plaintiffs' '527 Br. at 13.

FN10. Both parties agree that the limitations at issue refer to "precluding" the host computer from accessing the command block registers, not the command block register addresses, as stated in the claims.

Both parties are in agreement that the BSY bit is an indicator and does not itself operate to prevent the host computer from accessing the command block registers. However, they disagree over what the BSY bit indicates in the claims at issue. Plaintiffs, referring to the ATA specification, contend that the indicator is permissive, such that the BSY bit unset *permits* the host computer to access the command block registers and only indicates when the host computer *should not* access the command block registers. Defendants contend that the plain language of the claims makes it clear that the BSY bit indicates when the host computer is prevented from accessing the command block registers (i.e., it is impossible to access the command block register when the BSY bit is set). Plaintiffs on the other hand, argue the defendants' construction relies on a dictionary definition of "preclude." This reliance, they contend, is impermissible under *Phillips*.

Plaintiffs' protests aside, *Phillips* does not prevent a court from referring to a dictionary definition, so long as that definition is given the proper weight. *See, e.g.,* Terlep, 2005 WL 1950186 at *5 (citing Phillips, 415 F.3d at 1317). Because the claim language and specification are unhelpful to determining the meaning of preclude, the court first attempts to discern the ordinary meaning of "preclude," which, as defendants assert, has the ordinary meaning of "to make impossible." American Heritage Dictionary, 4th Ed.2000; Webster's Ninth New Collegiate Dictionary, 1988. Generally, a court may deviate from the ordinary meaning of a claim term in one of the following four circumstances. "First, the claim term will not receive its ordinary meaning if the patentee acted as his own lexicographer and clearly set forth a definition of the disputed claim term in either the specification or prosecution history." CCS Fitness v. Brunswick Corp., 288 F.3d 1359, 1366 (Fed.Cir.2002).FN11 The court discerns in neither the specification nor prosecution history any attempt to clearly set forth a definition of "precluded from accessing" that resembles plaintiffs' permissive construction. Indeed, "preclude" appears nowhere in the '440 patent, except in the claims. "Second, a claim term will not carry its ordinary meaning if the intrinsic evidence shows that the patentee distinguished that term from prior art on the basis of a particular embodiment, expressly disclaimed subject matter, or described a particular embodiment as important to the invention." Id. Again, there is no indication that the patentee distinguished the implementation of the BSY bit in the claimed invention in any way from the prior art, or otherwise described an implementation as important to the invention that supports plaintiffs' construction of "precluded from accessing." "Third ..., a claim term also will not have its ordinary meaning if the term 'chosen by the patentee so deprives the claim of clarity' as to require resort to the other intrinsic evidence for a definite meaning." Id. at 1367. The meaning of "precluded" is clear and does not conflict with the language of the claims or any description set forth in the specification. The fourth way cited by the Federal Circuit involves step- or means-plus-function format claims under 35 U.S.C. s. 112 para. 6, which is inapplicable to this case. Id. Based on this analysis, the court would conclude that the ordinary meaning of preclude obtains.

FN11. *CCS Fitness* was couched in terms of an alleged infringer attempting to overcome the plain meaning of a term. CCS Fitness, 288 F.3d at 1366 ("An accused infringer may overcome this "heavy presumption" and narrow a claim term's ordinary meaning but he cannot do so simply by pointing to the preferred embodiment or other structures or steps disclosed in the specification or prosecution history."). There is no reason why the same principles should not apply to a patentee advocating a construction that diverges from the ordinary meaning of the term.

The parties both argue that the following extrinsic evidence lends support to their respective constructions: the ATA specification FN12 and the implementation of the OTI-11 chip, which is the commercial

embodiment of the patent's preferred embodiment, *see, e.g.,* '527 patent, Fig. 3a. They agree that the ATA specification and the OTI-11 both specify that requests to access the command block register are to be redirected to another location, the status register, when the BSY bit is set.

FN12. The parties dispute whether the ATA specification is intrinsic or extrinsic evidence. Defendants characterize the ATA specification as extrinsic evidence. Plaintiffs, on the other hand, contend that it is intrinsic because it is referenced in the '440 patent specification and was submitted to the PTO during prosecution of the '440 patent. Plaintiffs' Resp. to Sur-reply at 9. They cite Phillips for support. 415 F.3d at 1317 ("The prosecution history, which we have designated as part of the 'intrinsic evidence,' consists of the complete record of the proceedings before the PTO and includes the prior art cited during the examination of the patent.").

Plaintiffs assert that this redirection to the status register demonstrates that defendants' construction requiring read and write access to be impossible when the BSY bit is set is not supportable. Even if writing to the command block register is precluded according to defendants' definition, plaintiffs contend that reading from the command block register is always possible. In particular, they argue the command block register not inaccessible when the BSY bit is set because it remains possible for part of the command block register (namely the status register) to be read. The redirect logic described above only sends the request to a different register in the command block, and that register is read instead. Defendants, on the other hand, argue that redirecting the request to another location is the same as precluding access to a command block register. Defendants essentially assert that because it is not feasible to physically preclude access to the command block registers, the redirect logic serves as the mechanism to make accessing the command block register impossible when the BSY bit is set.

The court agrees that, while access to the command block registers would technically be possible in the preferred embodiment because access is not physically prevented, reading from the command block register would only be accomplished by violating the rules established by the ATA specification or the logic of the OTI-11. Thus, the implementation described under either the ATA specification or implementation of the OTI-11, redirecting the read request away from the requested command block register when the BSY bit is set, would serve to make read access to the command block register impossible while the BSY bit is set.

Even assuming the ATA specification does not require the command block register to refuse access requests when the BSY bit is set, the plain language of the claims nonetheless clearly indicates that the BSY bit indicates when the host computer is *precluded* from accessing the command block register. In this case, the use of the term "precluded" carries the ordinary meaning of "prevented." Plaintiffs present no evidence that "preclude" would have generally suggested an alternative meaning to one of skill in the art. The extrinsic evidence set forth above appears to support the plain meaning of the term. Thus, the court finds that "precluded" carries its ordinary meaning. The "precluded from accessing" limitation is construed such that "the BSY bit indicates when it is impossible for the host computer to access the ATA command block registers." "Precluding" includes redirecting the request to another location.

C. "Sequentially ... Contiguous"

1. Proposed Constructions

The language at issue appears in various forms in both the '527 and '440 patents. The parties do not dispute the meaning of the words "sequential" or "contiguous." Rather, they dispute what it is that must be done in

a contiguous and sequential manner. Plaintiff contends that this limitation simply means the bytes of command information are received from the host computer in a sequential and contiguous fashion and may be stored in any fashion in the multi-byte command buffer. Defendants, however, contend that the host interface must additionally store multiple command bytes in a sequentially contiguous manner, as in a FIFO. The dispute appears to be whether the data received sequentially and contiguously from the host computer must also be stored in that way. Defendants contend that the location of the words "sequential" and "contiguous" in relation to the verb "store" dictates the nature of the storage of the data in the multi-byte buffer.

2. Claim Language

The words "sequentially" and "contiguous" generally appear as a limitation to the multi-byte buffer FN13 in all asserted claims of the '527 and '440 patents. Specifically, the claims read as follows:

FN13. One exception is claim 1 of the '527 patent wherein the words appear in context of an "ATA block register address." '527 patent at 28:52-53.

claim 1 of the '440 patent	"a multi-byte command buffer ... to store sequentially contiguous multiple command bytes
	received from said host computer"
claim 14 of the '440 patent	"a multi-byte command buffer ... to sequentially store multiple command bytes received
	contiguously from said host computer"
claim 1 of the '527 patent	"an ATA command block register address at which to store sequentially contiguous bytes of
	command data"
claim 2 of the '527 patent	"a multibyte command packet buffer ... to store sequentially contiguous bytes of command
	information"
claim 3 of the '527 patent	"a multibyte command packet buffer operable to sequentially store a packet of contiguous bytes of
	command information"

Plaintiffs point to differences in language to support their contention that "sequentially" and "contiguous" in

claim 1 of the '440 patent and claims 1 and 2 of the '527 patent means only that data be received be sequential and contiguous, while claim 14 of the '440 patent and claim 3 of the '527 patent require that receipt and storage of the command data be sequential and contiguous. The placement of the adjectives, argue plaintiffs, should inform the court's construction.

In claim 1 of the '440 patent ("to store sequentially contiguous multiple command bytes received"); claim 1 of the '527 patent ("to store sequentially contiguous bytes of command data" and claim 2 of the '527 patent ("to store sequentially contiguous bytes of command information"), "sequentially contiguous" is used to describe how the multiple bytes of command data in a single multi-byte command packet are received because the use of the term "sequentially contiguous" before "bytes" indicates that the limitation is intended to be applied to the way the bytes are received. By contrast, the other two claims specify that the command packet buffer is "to sequentially store ... contiguous bytes." FN14

FN14. Defendants rebut this argument by stating that "sequentially" and "contiguous" clearly modify the verb "store." The court disagrees that this is clear.

Defendants contend that, because the claimed controller *does not* control the characteristic of the bytes of command data received from the host but *does* control what happens to the bytes after it receives them, it would make no sense to construe the limitations "sequentially" and "contiguous" to apply only to the way the bytes are received. To do so, according to defendants, would read out an express limitation in the term. *See* Wright Medical Technology, 122 F.3d at 1444. This argument has merit: if the inventive controller cannot influence how bytes are received from the host computer, plaintiffs' construction that "sequentially" and "contiguous" in claims 1 and 2 of the '527 patent and claim 1 of the '440 patent refers only to how the data is received would be superfluous. There would be no sense in specifying this limitation because there would be no way for the inventive controller to alter it. Plaintiffs have not countered this argument. Thus, the court is inclined toward defendants' construction of the term.

3. Specification

Defendants point to the disclosure in the specification of read and write FIFOs to support their contention that "sequentially" and "contiguous" refer to how the received bytes are stored. However, while the FIFO controls how data is input and output to the buffer, it does not necessarily dictate how bytes are to be stored onto the buffer. The court finds that the specification does not provide adequate guidance on the issue.

4. Prosecution History

Defendants assert that the "sequentially" and "contiguous" language was added during prosecution to address prior art concerns expressed by the examiner. They contend that the applicants limited the claimed multi-byte buffer to one that stored bytes sequentially and contiguously because the examiner rejected the use of a multi-byte command buffer rather than the single-byte buffer in prior art in CD-ROM applications as obvious. Schwartz Decl., Ex. C at ZC001827. Plaintiffs counter that the prosecution history is inconclusive: the claims were amended to address the examiner's rejection over the Kikinis patent and the Yellow Book regarding error correction limitations of the claims, not to address the manner in which command information was received or controlled by the controller. Id. at ZC001754-58.FN15

FN15. Defendants present evidence that Zoran's expert, Samuels, endorses the view that bytes must be stored sequentially and contiguously. In the ITC proceedings, Zoran's expert testified that claim 14 of the

'440 patent and claim 3 of the '527 patent required that the data received be sequentially and contiguously stored, while claim 1 of the '440 patent and claims 1 and 2 of the '527 patent required only that the bytes be sequentially received because the adjectives modified "bytes" rather than "store." Chen Decl., Ex. 4 at 716:1-718:18. However, he acknowledged that he testified at his deposition that '527 claims 1 and 2 and '440 claim 1 required that the bytes be stored sequentially and contiguously. The court finds this evidence inconclusive as regards the construction of this language.

The "sequential" and "contiguous" limitations appeared following the two office actions, changing the claims in response to both concerns expressed by the examiner. Thus, it is likely that the addition of the disputed limitations was made in response to the examiner's obviousness concern. Nevertheless, the prosecution history is inconclusive as to what the limitations were meant to modify.

Based primarily on the function of the controller, the court rejects plaintiffs' argument that the sequentially contiguous language refers only to receiving data in claims 1 and 2 of the '527 patent and claim 1 of the '440 patent. It agrees with defendants: in all claims, "sequentially" and "contiguous" refer to the method of storing the command data, that is, storing successive command data in consecutive storage locations. Although the language of each claim differs slightly, it is permissible for the inventor to use different words to describe and claim the same limitation. *See* Kraft Foods, Inc. v. Int'l Trading Co., 203 F.3d 1362, 1368 (Fed.Cir.2000); Tate Access Floors, Inc. v. Maxacess Techs., Inc., 222 F.3d 958, 967-68 (Fed.Cir.2000). FN16 Here, it would appear that the inventors were using varying syntax to describe the storage of multi-byte data, as the controller does not seem to influence how data is received. Thus, the court adopts the defendants' construction of "sequentially contiguous" as requiring the device to have the ability to store multiple command bytes in a sequentially contiguous manner.

FN16. Although plaintiffs argue that claim differentiation requires the five claims to be construed differently, the claim differentiation doctrine has limits. "While two claims of a patent are presumptively of different scope, the doctrine of claim differentiation cannot broaden claims beyond their permissible scope ." Tate, 222 F.3d at 967-68 (citing Kraft, 203 F.3d at 1368).

D. Claim 3

1. Requested Constructions for Claim 3

The parties dispute how the court should construe claim 3 of the '527 which recites, in relevant part: "an ATA register address at which to receive data addresses and command data from said host computer and transmit data to said host computer, and a multibyte command packet buffer operable to sequentially store a packet of contiguous bytes of command information received through the ATA register address."

The parties have asked the court to construe the following limitations within claim 3:(1) optical drive controller; (2) "an ATA register address at which to receive data addresses and commands from said host computer and transmit data to said host computer, and a multibyte command packet buffer operable to sequentially store a packet of contiguous bytes ..."; and (3) "multibyte command packet buffer."

2. "Drive controller"

The parties agree that a controller may consist of a device or group of devices to control the communication

of data between a host computer and drive electronics. Defendants' '527 Br. at 18; Plaintiffs' Reply at 11. Plaintiffs ask the court to construe the term "drive controller" to exclude external translation circuitry, insisting that the patent specification and prosecution history teach away from the use of translation circuitry. Defendants, by contrast, argue that a controller is not defined by physical boundaries, but by elements necessary to accomplish the purpose of the controller. *Id*. at 19. Accordingly, they assert that, absent any express intention to exclude translation circuitry in the claims, specification, or prosecution history, translation circuitry may be included in the construction of "drive controller" where translation circuitry is employed to accomplish the purpose of the controller.

Defendants contend that if plaintiffs' construction is adopted, such that a "drive controller" excludes translation circuitry, the result would be that none of the accused devices would be infringing because they all comply with ATAPI. They assert that all ATAPI devices must engage in translation as sector addresses in CD-ROM devices are recorded in "minutes, seconds and fractions" ("MSF") format. However, because the host computer sends ATAPI commands in logical block address ("LBA") format, the communication between host computer and an ATAPI CD-ROM requires translation of address information in ATAPI command packets from LBA format to MSF format. In response to this argument, FN17 plaintiffs clarify that their proposed construction does not seek to exclude all translation circuitry, rather it seeks to exclude external translation circuitry, such as the external interface or host adapter card which the invention expressly sought to eliminate. *See, e.g.,* '527 patent at 2:41-3 ("This would obviate the need for an additional host adapter card and associated electronics.").

FN17. Plaintiffs also correctly point out that claims are not to be construed in light of the accused device. NeoMagic Corp. v. Trident Microsys., Inc., 287 F.3d 1062, 1074 (Fed.Cir.2002).

Plaintiffs support their position by pointing to several disclaimers found in the specification. The '527 patent states as the purpose of the invention that "it would be desirable to provide a CD drive with built-in controller functionality and a standard connection. This would obviate the need for an additional host adapter card and associated electronics." '527 patent at 2:39-43. It also emphasizes, "This invention reduces the cost of a host adapter card or additional ISA bus interface electronics." Id. at 5:45-48; *see also* id. at 7:24-32. They also point to a disavowal of claim scope in the prosecution history. In response to a December 3, 2001 office action, the inventors stated with regard to a "host interface" that "directly" connects that "the quoted limitations *cannot* be met where a controller requires a translator card or other intervening circuitry between the controller and the IDE bus to translate or manipulate command data due to the inability of the controller to properly handle native ATA command." Schwartz Decl., Ex. C at ZC001817.FN18

FN18. Plaintiffs contend that the inventors were distinguishing prior art translation devices such as the Mitsumi prototype created by Oak prior to its development of the OTI-11, which had an external card housing the translation circuitry. In their sur-reply briefing, the parties dispute whether the Mitsumi prototype was overcome during patent prosecution. The court finds that this discussion is unhelpful to the determination of whether the inventors disclaimed external translation circuitry.

The court finds that the inventors disclaimed external translation circuitry. Thus, the proper construction of "drive controller" includes translation circuitry but excludes circuitry necessarily located on an external adapter card.

3. "ATA register address"

Claim 3 recites "*an ATA register address* at which to receive data addresses and commands from said host computer and transmit data to said host computer, and a multibyte command packet buffer operable to sequentially store a packet of contiguous bytes of command information received through *the ATA register address*." '527 patent at 30:9-12. Although defendants agree that the claim language requires one ATA register address to receive data addresses and commands, transmit data and receive command information, they contend that the term should be construed such that *all* command information, whether single- or multi-byte, be received through a single ATA register address. Plaintiffs, on the other hand, argue that the claim language only requires that one ATA register address receive multi-byte command information, but that another ATA register address may receive single-byte commands.

The claim language does not refer to single-byte commands. It requires only an ATA register address "at which ... commands" are received and through which "contiguous bytes of command information" are received. There is no disclosed embodiment in the specification that includes an ATA register address that receives single- and multi-byte commands from the host computer and transmits data to a host computer. "A patent claim should be construed to encompass at least one disclosed embodiment in the written description portion of the patent specification." Johns Hopkins University v. Cellpro, Inc., 152 F.3d 1342, 1355 (Fed.Cir.1998). Because the claims do not address single-byte commands, the court concludes that the ATA register address of claim 3 is not required to receive both single-byte and multi-byte commands from the host computer.

4. ATA Block Registers and the Multibyte Command Packet Buffer

The parties agree that the host interface requires certain structures to connect an optical drive controller to the host computer over the IDE/ATA bus. They also agree as to the requirement for certain basic structures to be present, namely: (1) support for all eight ATA command block registers; (2) the following ATA signals: CS1FX, CS3FX, DA0-DA2, DASP, PDIAG, DIOR, DIOW, and INTERQ (HIRQ) and DD0-DD15; (3) the DRV bit; and (4) the BSY bit. Defendants' '527 Br. at 24; *see also Oak Technology v. UMC,* Claim Construction Order (Case No. C-97-20959 RMW). The parties also agree that a multibyte command packet buffer must exist. They disagree, however, as to whether a multi-byte command packet buffer must be present in addition to and separate from the eight ATA command block registers.

Defendants contend that the claim language itself supports the construction requiring the multi-byte command packet buffer to be present and distinct from the ATA command block registers. For example, in claim 1 of the '440 patent, the multi-byte command packet buffer ('440 patent at 28:38) is referenced as distinct from at least three of the ATA command block registers, id. at 28:44-49. In one portion of the claim, the multi-byte command buffer is addressed by the command block register addresses ("the multi-byte command buffer addressed by one of a plurality of ATA command block register addresses" (Id. at 28:42-44)); in another, the DRV bit, which is addressed by the command block register, indicates whether to store commands in the multi-byte buffer ("said DRV bit to determine whether to store commands in said multi-byte command buffer" (Id. at 28:44-49)).

Plaintiffs nevertheless argue that there is no requirement that the ATA command block register necessarily be physically distinct from the multi-byte command packet buffer or operate simultaneously. They contend that there is nothing in the specification that indicates that there must be separate and distinct physical structures for these elements. Nor is there anything in the specification that requires that these elements to

operate at the same time. For further support, they cite to *NTP,* in which the Federal Circuit determined that an express "hook" was required in the language of the patent to read in a requirement that is not otherwise expressly stated. NTP, ___ F.3d ___, 2005 WL 180612 at *21 ("Our case law requires a textual "hook" in the claim language for a limitation of this nature to be imposed.... In other words, 'there must be a textual reference in the actual language of the claim with which to associate a proffered claim construction." ' (citing Johnson Worldwide Assocs., Inc. v. Zebco Corp., 175 F.3d 985, 990 (Fed.Cir.1999)). They contend that, for a limitation requiring the ATA command block registers to be distinct from the multi-byte command packet buffer, the claim must designate such elements as being "separate." The court agrees that there is no textual hook present in the claims, thus the court concludes that it is not required that the ATA block registers and multi-byte command packet buffer be distinct or separate structures.

III. CLAIM CONSTRUCTION

Having considered the papers submitted by the parties and the arguments of counsel during the claim construction hearing, the court interprets the disputed claim terms as set forth below.

CLAIM LANGUAGE	CONSTRUCTION
"data error detection and correction circuitry"	means "any error detection and correction circuitry."
"precluded from accessing"	means "the BSY bit indicates when it is impossible for the host computer to access the ATA command block registers." Access is precluded when a read request is directed away from the command block register.
"sequentially ... contiguous"	requires the device to have the ability to store multiple command bytes in a sequentially contiguous manner
"drive controller"	includes translation circuitry but excludes circuitry located on an external adapter card.
"ATA register address"	The ATA register address of claim 3 is not required to receive both single-byte and multi-byte commands from the host computer.
ATA block registers and multibyte command packet buffer	It is not required that the ATA block registers and multi-byte command packet buffer be distinct or

	separate structures.

N.D.Cal.,2005.
Zoran Corp. v. Mediatek, Inc.