United States District Court,
N.D. California.

TOSHIBA CORPORATION,
Plaintiff Counterclaim Defendant.
v.
LEXAR MEDIA, INC,
Defendant Counterclaim Plaintiff.

No. C-02-5273 MJJ

Jan. 24, 2005.

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CLAIM CONSTRUCTION ORDER

MARTIN J. JENKINS**, District Judge.**

INTRODUCTION

Before the Court is the parties' proposed construction of several disputed terms contained in six of Lexar Media Inc.'s ("Lexar") patents. Having carefully read and considered the parties' briefs and the arguments proffered by the parties at the August 11, 2004 claim construction hearing, the Court construes the disputed claim terms as follows.

FACTUAL BACKGROUND

The patents at issue are U.S. Patent Number 5, 479,638 ("the '638 patent") entitled "Flash Memory Mass Storage Architecture Incorporation Wear Leveling Technique;" U.S. Patent Number 6,040,997 ("the '997 patent") entitled "Flash Memory Leveling Architecture Having No External Latch;" U.S. Patent Number 6,145,051 ("the '051 patent") entitled "Moving Sectors Within a Block of Information in a Flash Memory Mass Storage Architecture;" U.S. Patent Number 6,262,918 ("the '918 patent") entitled "Space Management for Managing High Capacity Nonvolatile Memory;" U.S. Patent Number 6,397,314 ("the '314 patent") entitled "Increasing the Memory Performance of Flash Memory Devices By Writing Sectors Simultaneously

to Multiple Flash Memory Devices;" and U.S. Patent Number 6, 202, 138 ("the '138 patent") entitled "Increasing the Memory Performance of Flash Memory Devices By Writing Sectors Simultaneously to Multiple Flash Memory Devices." All six patents are owned by Lexar and relate to how memory controllers operate to read, write, erase, and re-write information from nonvolatile memory. The technology is used in digital cameras, portable music players (such as MP3 players), and portable data storages for personal computers.

The '638 patent, the oldest of the patents-in-suit, describes a method and apparatus for rewriting a block of memory without having to simultaneously erase old data. The old data is instead flagged as superceded and stored as "ready for erasure" as soon as no new blocks are available. Each time this occurs, the device automatically rearranges the "ready for erasure" sectors, bundling them into a single block for erasure as soon as there are no empty blocks. Because prior art had to erase old data before writing new data, re-writing took a long time. The '638 patent technology saves time. If there are no empty blocks to store the "old" data that is ready to be erased, the device is automatically prompted to erase entire blocks of superceded, ready-to-erase data.

The '997 patent describes a method and apparatus for moving data within memory to facilitate the use of all sectors and blocks such that no sector or block is used so frequently that it wears out before the other sectors and blocks. The '051 patent describes a method and apparatus for re-writing less than an entire block of memory (re-writing by sector). The '918 patent, the "super block patent," describes a method and apparatus for enabling the erasure of multiple blocks simultaneously to save time.

The '314 patent, the most recent of the patents-in-suit, is a continuation of the '138 patent. The patents have identical disclosures and describe an apparatus for writing multiple sets of data to different memory devices to save time. The '314/'138 patent is related, at least in part, to the '051 patent in that they share a common parent application. The application for the '051 patent, however, was only a continuation-in-part of the application that led to the '314/'138 patent.

In the December 8, 2003 Joint Submission of Claim Terms for Construction, the parties disclosed twenty-four disputed claim terms to be construed by the Court. This number included-nine universal terms agreed to by the parties, two additional terms chosen by Lexar, eight additional terms chosen by Toshiba Corporation ("Toshiba"), and five additional claim terms chosen by Pretec Electronics Corporation, et al. ("Pretec"). After careful consideration of the briefs, the submitted list of claim terms, and the patents themselves, the Court concluded that to construe each of these terms properly, the Court must actually engage in 48 separate claim construction analyses, far more than the 30 to which the Court originally agreed. This is because each of nine of the first ten of the disputed claim terms appears in more than one of the patents-in-suit. For "controller," for example, this means four separate claim construction analyses because the term appears in five of the six patents-in-suit (two of which have identical disclosures such that the Court need only engage in one analysis to construe a common claim term). Consequently, the Court ordered that it would construe a sub-set of the claim terms originally identified by the parties, including: the nine universal terms (which amounts, by the Court's count, to a total of 30 separate constructions since eight of the nine terms appear in multiple patents), the two additional terms identified by Lexar in the Joint Statement (one of which requires two separate analyses because it appears in two separate patents), two terms (of the original eight) chosen by Toshiba, and two terms (of the original five) chosen by Pretec. In total, the Court engaged in 37 separate analyses of the meaning of various claims. Oral argument on the construction of these claim terms was held on August 11, 2004. At oral argument, the Court discerned that there was no real dispute regarding many of the claim terms to be construed. Accordingly, the Court

construes only disputed claim terms in this Order. To the extent that the parties determine later that there truly is a dispute as to the construction of those other terms, the Court will construe those terms.

DISPUTED CLAIM TERMS

The following is a list of the disputed claim terms construed in this Order:

-> "controller" in the '638 patent

-> "controller" in the '997 patent

-> "controller" in the '051 patent

-> "controller" in the '314/'138 patents

-> "host" in the '997 patent

-> "host" in the '051 patent

-> "host" in the '314/'138 patents

-> "host" in the '918 patent

-> "block" in the '638 patent

-> "block" in the '918 patent

-> "block" in the '314/'138 patents

-> "sector" in the '051 patent

-> "sector" in the'918 patent

-> "sector" in the '314/'138 patents

-> "super-block" in the '918 patent

-> "program" in the '638 patent

-> "program" in the '314 patent

-> "writing ... simultaneously" in the '314/'138 patents

-> "logical block address" in the '051 patent

-> "physical block address" in the '051 patent

-> "virtual block address" in the '051 patent

-> "information block" in the '051 patent

-> "avoids transfer" in the '051 patent

-> "being operative to access portions of an information block stored in more than one block locations" in the '051 patent

-> "directly correlating" in the '638 patent

LEGAL STANDARD

The construction of a patent claim is a matter of law for the Court. Markman v. Westview Instruments, Inc., 517 U.S. 370, 372, 116 S.Ct. 1384, 134 L.Ed.2d 577 (1996). The Court must conduct an independent analysis of the disputed claim terms. It is insufficient for the Court to simply choose between the constructions proposed by the adversarial parties. Exxon Chem. Patents v. Lubrizol Corp., 64 F.3d 1553, 1555 (Fed.Cir.1995). "The subjective intent of the inventor when he used a particular term is of little or no probative weight in determining the scope of a claim (except as documented in the prosecution history)." Markman v. Westview Instruments, Inc., 52 F.3d 967, 985 (Fed.Cir.1995) (*en banc*), *aff'd,* Markman, 517 U.S. 370, 116 S.Ct. 1384, 134 L.Ed.2d 577. "Rather the focus is on the objective test of what one of ordinary skill in the art at the time of the invention would have understood the term to mean." Id. at 986. To determine the meaning of a patent claim, the Court considers three sources: the claims, the specification, and the prosecution history. Id. at 979.

The Court looks first to the words of the claims. Vitronics Corp. v. Conceptronic, Inc., 90 F.3d 1576, 1582 (Fed.Cir.1996). "Although words in a claim are generally given their ordinary and customary meaning, a patentee may choose to be his own lexicographer and use terms in a manner other than their ordinary meaning, as long as the special definition of the term is clearly stated in the patent specification or file history." *Id*. (citation omitted). "A technical term used in a patent document is interpreted as having the meaning that it would be given by persons experienced in the field of the invention, unless it is apparent from the patent and the prosecution history that the inventor used the term with a different meaning." Hoechst Celanese Corp. v. BP Chems. Ltd., 78 F.3d 1575, 1578 (Fed.Cir.1996). The doctrine of claim differentiation creates the presumption that limitations stated in dependent claims are not to be read into the independent claim from which they depend because different language used in separate claims is presumed to indicate that the claims have different meanings and scope. Tandon Corp. v. U.S. Int'l Trade Comm'n., 831 F.2d 1017, 1023 (Fed.Cir.1987).

Second, it is always necessary to review the specification to determine whether the inventor has used any terms in a manner inconsistent with their ordinary meaning. Vitronics, 90 F.3d at 1582. The specification can act as a dictionary when it expressly or impliedly defines terms used in the claims. *Id*. Because the specification must contain a description of the invention that is clear and complete enough to enable those of ordinary skill in the art to make and use it, the specification is the single best guide to the meaning of a disputed term. *Id*. The written description part of the specification itself does not delimit the right to exclude, however; that is the function and purpose of claims. Markman, 52 F.3d at 980.

Third, the court may consider the prosecution history. Vitronics, 90 F.3d at 1582. "Although the prosecution

history can and should be used to understand the language used in the claims, it too cannot enlarge, diminish, or vary the limitations in the claims." Markman, 52 F.3d at 980 (internal quotation marks deleted) (citations omitted). However, a concession made or position taken to establish patentability in view of prior art on which the examiner has relied, is a substantive position on the technology for which a patent is sought, and will generally generate an estoppel. In contrast, when claim changes or arguments are made in order to more particularly point out the applicant's invention, the purpose is to impart precision, not to overcome prior art. Such prosecution is not presumed to raise an estoppel, but is reviewed on its facts, with the guidance of precedent. Pall Corp. v. Micron Separations, Inc., 66 F.3d 1211, 1220 (Fed.Cir.1995) (citations omitted).

Disputed claim terms are construed consistently across all claims within a patent. Southwall Techs., Inc. v. Cardinal IG Co., 54 F.3d 1570, 1579 (Fed.Cir.1995). Where patents-in-suit share the same disclosures, common terms are construed consistently across all claims in both patents. Mycogen Plant Set., Inc. v. Monsanto Co., 252 F.3d 1306, 1311 (Fed.Cir.2001) (*overruled on other grounds*). Similarly, where two patents share common disclosures, common claim terms should be construed consistently. *Id*. Also, where multiple patents stem from the same parent application, the prosecution history of one is relevant to the construction of common claim terms. Microsoft Corp. v. Multi-Tech Sys., 357 F.3d 1340, 1349 (Fed.Cir.2004). However, common claim terms in patents stemming from the same parent application need not necessarily be construed consistently across patents. MSM Invs. Co., LLC v. Carolwood Corp., 259 F.3d 1335 (Fed.Cir.2001).

Ordinarily, the Court should not rely on expert testimony to assist in claim construction, because the public is entitled to rely on the public record of the patentee's claim (as contained in the patent claim, the specification, and the prosecution history) to ascertain the scope of the claimed invention. Vitronics, 90 F.3d at 1583. "[W]here the public record unambiguously describes the scope of the patented invention, reliance on any extrinsic evidence is improper." *Id*. Extrinsic evidence should be used only if needed to assist in determining the meaning or scope of technical terms in the claims, and may not be used to vary or contradict the terms of the claims. *Id*. (quoting Pall Corp., 66 F.3d at 1216); Markman, 52 F.3d at 981.

The Court is free to consult technical treatises and dictionaries at any time, however, in order to better understand the underlying technology and may also rely on dictionary definitions when construing claim terms, so long as the dictionary definition does not contradict any definition found in or ascertained by a reading of the patent documents. Vitronics, 90 F.3d at 1584 n. 6. The Court also has the discretion to admit and rely upon prior art proffered by one of the parties, whether or not cited in the specification or the file history, but only when the meaning of the disputed terms cannot be ascertained from a careful reading of the public record. Id. at 1584. Referring to prior art may make it unnecessary to rely on expert testimony, because prior art may be indicative of what all those skilled in the art generally believe a certain term means. *Id*. Unlike expert testimony, these sources are accessible to the public prior to litigation to aid in determining the scope of an invention. *Id*.

ANALYSIS

Before reaching the actual construction of the claim terms in dispute, the Court must address two matters of significance. First, the Court rejects Lexar's contention that common terms appearing across multiple patents should, as a rule, be construed consistently. The Court declines to assign a one-size-fits-all construction to a common claim term without conducting an individualized analysis of the claim term's meaning in the context of each of the patents in which the term appears. Unless patents containing common claim terms

have the same disclosures, it is improper to assign a claim term a uniform construction across multiple patents even where those patents pertain to similar technology, have the same inventor, and the same owner or assignee. *See e.g.* Abbott Labs. v. Dey, L.P., 287 F.3d 1097, 1105 (Fed.Cir.2002) (the prosecution history of one patent is not necessarily relevant to the claim construction analysis of a claim term in another patent even where the patent applications have the same assignee, the same inventor, and similar subject matter); MSM, 259 F.3d 1335 (just because a related patent limits claims to certain uses does not compel the court to construe the same claim in another patent as so limited). The Court notes, however, that having engaged in such a particularized analysis, it turns out that some of the disputed claim terms appearing in more than one patent have the same meaning, regardless of the unrelatedness of the patents.

Second, the Court notes that three of the patents-in-suit are related to one another, at least in part. The '314 and '138 patents have identical specifications; therefore, claim terms common to both patents, such as "controller" and "host," are to be construed identically. Also, the '051 patent shares, in part, a common parent application with the '314/'138. This means that the prosecution history of each of the three patents ('051, '314, ' 138) maybe relevant to an understanding of the scope of a term (such as "controller") common among the patents. However, because the '051 patent's disclosures are different from the '314/'138's, the claim terms common to the ' 051 patent on the one hand and the '314/'138 on the other are not necessarily to be construed consistently.

I. "controller"

A. Preliminaries

The term "controller" appears in five of the six patents-in-suit as follows:

-> '638 patent, claim 18 (and dependent claims 19, 22, and 24);

-> '997 patent, claims 1, 3, and 12;

-> '051 patent, claims 1 (and dependent claims 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15, 16, and 17) and 18 (and dependent claims 19, 20, 21, 22, 23, 24, 25, and 26);

-> '314 patent, claim 1; and

-> '138 patent, claims 1 (and dependent claims 2, 3, 7, 8, 12), 13 (and dependent claims 14 and 15), 21, 36, and 46.

B. Construction

i. "controller" in the '638 patent

Lexar's proposed construction:	**Toshiba's proposed construction:**	**Pretec's proposed construction:**
A device that interfaces between a host and flash memory	-none-A device that interfaces between a host and nonvolatile memory	

The parties' disagreement over the meaning of the term "controller" in the '638 patent is less about the meaning of the actual claim term and more about the scope of the device with which the controller

interfaces. While Pretec suggests that the "controller" interfaces between the host and any kind of nonvolatile memory, Lexar proposes a narrower construction, that the controller interfaces with a specific type of nonvolatile memory-"flash memory (or any other semiconductor having the same characteristics as flash memory)." Toshiba offers no proposed construction.

Lexar suggests that the claim language in the '997 and the specification of the '051 patent supports its construction. However, the '997 and '051 patents, wholly unrelated to the '638 patent, are irrelevant to the claim construction analysis of the term "controller" in the '638 patent for the reasons explained above.

Pretec argues that claims 31 and 34 support construing "controller" as interfacing with a broader range of semiconductors: all nonvolatile memory. The Court agrees. In Claim 31 (dependent from Claim 18 in which a "controller" is first claimed), "flash memory" is expressly claimed as one form of nonvolatile memory with which the controller may interface. Dependent Claim 31 alone, according to the doctrine of claim differentiation, creates the presumption that the claim from which Claim 31 is dependent (independent Claim 18) is broader than flash memory; otherwise, it is assumed, the inventor need not state the additional limitation in the dependent claim. However, the Court need not rely solely on the claim differentiation presumption here because another dependent claim, Claim 34, claims that the controller may alternatively interface with E ^{2}PROM cells. That another dependent claim offers an alternative type of nonvolatile memory with which the controller may interface means that the independent claim from which claims 31 and 34 are dependent claims a broader range of nonvolatile memory. Therefore, the language of the claims themselves supports Pretec's proposed construction.

The '638 specification does nothing to limit the claims further. It might be argued that the nonvolatile memory is really limited to flash memory because the preferred embodiment uses flash memory for memory storage. ('638 patent, 3:46-47.) But in construing disputed claim terms, a limitation cannot be imported from the preferred embodiment into the claims themselves. Markman, 52 F.3d at 980. In any case, we need not even address that line of argument because the description of the preferred embodiment actually expressly embraces E ^{2}PROM as a form of nonvolatile memory with which the controller may interface: "In the preferred embodiment, all of the memory storage is flash EEPROM. *It is possible to substitute E ^{2}PROM for some or all of the data bits shown*" ('638 patent, 3:46-49 (emphasis added).) The specification does not limit "controller" to flash memory and in fact, serves to support Pretec's proposed broader construction.

Lexar suggests that the title of the '638 patent, "Flash Memory Mass Storage Architecture Incorporation Wear Leveling Technique," supports limiting the construction of "controller" to a device that interfaces with flash memory, rather than all non-volatile memory. But it is well-settled that the title of a patent is largely "irrelevant to claim construction." Robert L. Harmon, *Patents and the Federal Circuit* s. 6.3(c) (6th ed.2003). "[I]f courts do not read limitations into the claims from the specification that are not found in the claims themselves, then they certainly will not read limitations into the claims from the patent title." Id. Here, although the title of the patent suggests that the inventor intended to focus on flash memory, the Court will not allow implications from the title of the patent to override what the patent, having considered the claims themselves and the specification, actually claims.

The Court therefore declines to adopt Lexar's proposed construction of "controller" in the '638 patent as it is unsupportably narrow and instead finds Pretec's proposed construction is the correct one. In the '638 patent, the "controller" is a device that interfaces between a host and nonvolatile memory.

ii. "controller" in the '997 patent

Lexar's proposed construction:	**Toshiba's proposed construction:**[FN1]

FN1. Pretec offers no proposed construction here, Pretec only proposes constructions for disputed terms in the '638 and '051 patents.

A device that interfaces between a host and flash memory	the internal controller of the flash array and control signaling from the external controller

Lexar proposes that "controller" in the '997 patent should be construed as a device that interfaces between a host and flash memory (or another semiconductor with the same characteristics). Lexar suggests three ways in which its proposed construction is supported. First, Lexar argues that the specification of the '051 patent supports its construction. Again, the ' 051 patent, wholly unrelated to the '997 patent, is irrelevant to the claim construction analysis of the term "controller" in the '997 patent as explained above. The '051 specification will not be considered in this discussion. Second, Lexar argues that the title of the '997 patent, "Flash Memory Leveling Architecture Having No External Latch," supports its proposed construction of "controller ." As explained above, the title of a patent is largely "irrelevant to claim construction." Harmon, *Patents and the Federal Circuit* s. 6.3(c). The Court will not ignore the title as entirely insignificant but it will not find the title dispositive either. Third, and most convincingly, Lexar suggests that the claim language in the '997 supports its construction because independent claim 1 and its corresponding dependent claims (2, 5, 7, 8, 9, 11, and 12) all expressly claim "a flash memory system comprising flash memory." (Lexar's Opening Brief at 9.) Because the '997 patent claims are expressly limited to flash memory (unlike, for example, the ' 638 patent discussed above), Lexar is correct. Indeed, Toshiba concurs that the controller interfaces between a host and flash memory.

But there is more to the dispute over this term than the type of nonvolatile memory with which the controller interfaces. Toshiba's disagreement with Lexar's construction of "controller" in the '997 patent is not centered on the type of memory with which the device interfaces so much as with clarifying the controller's role with respect to the internal flash controller and the control signals from the external controller. Toshiba argues that because the controller, as recited in claims 1 and 12 of the '997 patent, encompasses both the internal controller (that directly transfers data to the destination) and the control signals from the external controller (that allows the internal controller to transfer data), "controller" should be construed to include those functions. The Court finds that to do so, however, would render the portions of the claims specifying the functions of internal controller function control signals from the external controller redundant. Loading the single term "controller" with additional limitations already captured by the rest of the claims themselves is unnecessary. The Court therefore construes "controller" in the '997 patent as a device that interfaces between a host and flash memory.

iii. "controller" in the '051 patent

Lexar's proposed construction:	**Toshiba's proposed construction:**	**Pretec's proposed construction:**
A device that interfaces between a	interfaces with	A device that interfaces between a host

host and flash memory	nonvolatile memory	and nonvolatile memory

Again, the dispute here is over the type of nonvolatile memory with which the controller interfaces. Lexar proposes that "controller" in the '051 patent be construed as a device that interfaces between a host and flash memory (or another semiconductor with the same characteristics) while Toshiba and Pretec propose that the controller interfaces with a broader range of semiconductors: all nonvolatile memory.

Lexar suggests that the claim language of the '997 patent supports its construction. The '997 and '051 patents do not share a common specification. Therefore the Court finds that the '997 patent is not particularly relevant to the construction of the term "controller" in the '051 patent. Lexar also argues that two aspects of the '051 patent itself evidence its position that the controller interfaces with flash memory only. First, Lexar argues that the title of the '051 patent, "Moving Sectors Within a Block of Information in a Flash Memory Mass Storage Architecture," supports its proposed construction of "controller." As explained above (in the context of construing "controller" in the '638 patent), limitations will not be read into the claims based solely on the patent's title. Lexar's second and more compelling argument is that the language of the claims in the '051 patent dictates that the controller interface between a host and flash memory (not, as Defendants propose, between a host and all nonvolatile memory).

For example, Claim 1, wherein a "controller" is first claimed, describes a "memory controller for use with a host requiring access to a nonvolatile memory" and then claims that "nonvolatile memory includ[es] a plurality of selectively erasable block locations." Lexar claims that nonvolatile memory other than flash memory (*e.g .,* Electronically Erasable Programmable Read Only Memory ("EEPROM")) cannot have a plurality of selectively erasable block locations and that therefore, the controller, as claimed in the '051 patent, cannot be construed to interface with anything other than flash memory (or another semiconductor with like characteristics). To the contrary, Pretec claimed, both in its brief and at oral argument, that EEPROM can indeed be erased in blocks. (Claim Construction Hearing Transcript at 184-85; Pretec Brief, Ex. D.) Either way, the language of the preferred embodiment, absent more explicit language in the claims limiting nonvolatile memory to flash, suggests that an alternative embodiment of the invention could interface with EEPROM. ('051 patent 8 :34-36 .) A claim construction that does not read on a preferred embodiment is "rarely, if ever, correct." Vitronics, 90 F.3d at 1583-84. Therefore, the Court cannot construe "controller" here to be limited to flash memory because the preferred embodiment allows the controller to interface with EEPROM. The appropriate construction for the '051 term "controller" is a device that interfaces between a host and nonvolatile memory.

iv. "controller" in the '314/'138 patents

Lexar's proposed construction:	**Toshiba's proposed construction:**[FN2]

FN2. Pretec offers no proposed construction here. Pretec only proposes constructions for disputed terms in the '638 and '051 patents.

A device that interfaces between a host and flash memory	interfaces with nonvolatile memory

The dispute here is the same. Lexar again proposes that "controller" interfaces with flash memory only

while Toshiba contends the controller interfaces with all nonvolatile memory.

The Court looks first to the language of the claims. Toshiba argues that the language of the claims themselves supports a finding that "controller" in the ' 314/'138 patent interfaces with all nonvolatile memory. Indeed, nothing in the language of the claims themselves suggests that the "controller" interfaces with just flash. Specifically, Claim 1 of the '314 and Claims 1, 13, and 46 of the '138 recite a controller connected to a nonvolatile memory unit, and say nothing about flash memory. Toshiba additionally argues that the doctrine of claim differentiation supports its construction but that argument is without merit. According to Toshiba, Claim 11 and Claim 29 in the '138 patent, which claim that the nonvolatile memory unit is a "flash memory chip," suggests that the doctrine of claim differentiation applies here. Had the patentee intended to teach a controller that interfaces only with flash memory, the argument goes, the patentee would not have specified flash in the dependent claims only. However, as Lexar correctly pointed out at oral argument, a flash memory *chip* is one method of using flash memory. That a flash chip is claimed in a dependent claim does not necessarily indicate, through the doctrine of claim differentiation, that the independent claim is intended to claim all nonvolatile memory. Indeed, the dependent claim's mention of a flash memory chip alone could very well mean that the broader, independent claim claims all forms of flash memory. Toshiba's claim differentiation argument fails. This does not mean, however, that Toshiba's construction of "controller" is wrong.

Lexar argues that the Court must look at the larger context of the patents. Flash memory, according to Lexar, is the only type of nonvolatile memory that can be erased in blocks and the patents claim only the type of nonvolatile memory that is erasable in blocks. However, even if, *arguendo,* being selectively erasable is what distinguishes flash memory from other types of nonvolatile memory, the '314/'138 patents do not expressly limit the claimed "controller" to interface only with selectively erasable nonvolatile memory in the same way that the '051 does. Lexar contended at oral argument that the '138 patent teaches a "block-oriented memory structure." But Lexar's characterization is a leap from claim language that expressly claims a device that interfaces with nonvolatile memory generally and neither claims that it is limited to flash memory devices nor that it is limited to nonvolatile memory that is selectively erasable. Based on the language of the claims, Toshiba has the better of the argument here.

Having determined that the claim language suggests that the broader construction of "controller" is the proper one, the Court next examines the specification to determine whether the patentee acted as his own lexicographer and assigned a construction other than the ordinary meaning as understood by a person skilled in the relevant art. In keeping with its contextual argument, Lexar contends that it is clear from the disclosures in the '138/'314 patent that the inventor intended that "nonvolatile memory" be limited to flash. Specifically, Lexar suggests that the title of the '314/'138 patent, "Increasing the Memory Performance of Flash Memory Devices By Writing Sectors Simultaneously to Multiple Flash Memory Devices," is suggestive of its limitation to flash memory. But again, while the title of the patent may be considered, it is not dispositive of the construction of a disputed claim term. Second, Lexar proposes that the block-oriented nature of the patents, as gleaned from the Abstract and the Field of the Invention sections, supports limiting the construction to flash. However, it is a strict rule of claim construction that limitations from the specification cannot be imported into the claims. Markman, 52 F.3d at 980. Moreover, nothing in the specification suggests any narrower a construction than exists in the language of the claims themselves. While the Court does not pretend that context is insignificant, the Court finds that here, the language of the claims indicates the broader construction is the right one and the specification does not compel a different result. FN3

FN3. Lexar again attempts to use other patents (the '997 and '051 patents) to support its construction of "controller." The '997 patent is wholly unrelated to the '314/'138 patent and does not help Lexar. While the '051 is related (in part) to the '314/'138, common claim terms need not be construed consistently across patents. MSM, 259 F.3d 1335. The Court therefore declines to look to other patents to construe "controller" in the '314/'138.

Not only is there no support in the specification for a narrower construction, there is, as Toshiba points out, support in the specification for the broader construction of "controller" consistent with a plain reading of the claim language. The Summary of the Invention in the '314/'138 patent states as follows:

It is an object of the present invention to increase the performance of a digital system having a controller coupled to a host for operating a nonvolatile memory bank including one or more nonvolatile memory devices, **such as flash and/or EEPROM chips,** by reducing the time associated with reading and writing information to the nonvolatile memory bank.

('314 patent, 3:61-65; '138 patent, 3:54-60 (emphasis added).) That EEPROM is mentioned as a type of nonvolatile memory device in the context of a description of the invention supports construing "controller" broadly, consistent with the claim language, which claims a controller that interfaces with nonvolatile memory devices generally, not just flash. Toshiba also directs the Court to the '138's specification, column 1, lines 38-40, in which EEPROM is mentioned, and argues that this suggests that the patentee considered types of nonvolatile memory, other than flash, to be encompassed by the claims. (Toshiba's Opposition at 10.) However, this portion of the specification, as well as column 1, lines 43-47 of the '314 patent, describes the prior art, not the invention itself. The claims cannot be construed solely on the basis of a prior art description. These portions of the specification merely provide the context for the problem that the inventor sought to resolve, not what is actually claimed in the patent. The misguidedness of that particular argument notwithstanding, Toshiba is right that the specification supports the broader construction of "controller" here.

In the '314/'138 patent, the plain language of the claims recites all nonvolatile memory, not flash. The specification provides no support for a narrower construction and its mention of EEPROM in the Summary of the Invention actually supports the broader construction consistent with the claim language. Therefore, the Court agrees with Toshiba that the "controller" in the '314/' 138 patent interfaces between a host and nonvolatile memory.

II. "host"

A. Preliminaries

The claim term "host" appears in five of the six patents-in-suit as follows:

-> '997 patent, claim 13 (and dependent claim 15);

-> '051 patent, claims 1 (and dependent claims 2 and 3) and 18 (and dependent claim 21);

-> '314 patent, claims 1 and 7;

-> '138 patent, claims 1, 13, 16 (and dependent claims 17 and 20), and 35; and

-> '918 patent, claims 1, 10, and 17.

As with the dispute over the construction of "controller," the difference between Lexar's proposed construction on the one hand, and Toshiba's and Pretec's proposed constructions on the other, turns on the device with which the host interfaces (through the controller). Lexar contends that the "host" writes information to and reads information from flash memory while Toshiba and Pretec propose more broadly that a host interfaces with all nonvolatile memory.

B. Construction

i. "host" in the '997 patent

Lexar's proposed construction:	**Toshiba's proposed construction:**	**Pretec's proposed construction:**
A host writes information to and reads information from flash memory through a controller device.	interfaces with nonvolatile memory	A host writes information to and reads information from non-volatile memory through a controller device.

The Court's analysis as to the proper construction of "controller" in the '997 patent applies equally to "host" in the '997 patent. Therefore, the "host" in the '997 patent interfaces, through the controller, with flash memory.

ii. "host" in the '051 patent

Lexar's proposed construction:	**Toshiba's proposed construction:**	**Pretec's proposed construction:**
A host writes information to and reads information from flash memory through a controller device	interfaces with nonvolatile memory	A host writes information to and reads information from non-volatile memory through a controller device

The Court's analysis as to the proper construction of "controller" in the ' 051 patent applies equally to "host" in the '051 patent. The Court construes "host" in the '051 patent as interfacing, through the controller, with nonvolatile memory.

iii. "host" in the'314/'138

Lexar's proposed construction:	**Toshiba's proposed construction:**[FN4]
A host writes information to and reads information from flash memory	interfaces with

FN4. Pretec offers no proposed construction here. Pretec only proposes constructions for disputed terms in the '638 and '051 patents.

through a controller device	nonvolatile memory

The Court's analysis regarding construction of "controller" in the '314/' 138 patent applies equally to "host" in the '314/' 138. The Court therefore construes "host" in the '314/'l 38 as interfacing, through the controller, with nonvolatile memory.

iv. "host" in the '918 patent

Lexar's proposed construction:	**Toshiba's proposed construction:**[FN5]

FN5. Pretec offers no proposed construction here. Pretec only proposes constructions for disputed terms in the '638 and '051 patents.

A host writes information to and reads information from flash memory through a controller device	interfaces with nonvolatile memory

The claim term "controller" does not appear in the '918 patent, but "host" does. Therefore, the Court must analyze separately the construction of "host" in the '918. Again, the difference between Lexar's and Toshiba's proposed constructions of "host" in the '918 patent turns on that with which the host indirectly interfaces (through the controller). Lexar points to nothing in the '918 patent itself to support its construction except the patent's title (not dispositive as discussed supra) and except to clarify that the "flash memory *chips*" recited in dependent claim 16 are not the same as "flash memory," presumably to discourage the Court from mistakenly determining that the doctrine of claim differentiation applies here.

Toshiba suggests that "host," as claimed in the '918 patent, must be construed as interfacing (through the controller) with any type of nonvolatile memory because the language of the claims themselves and the specification support that broader construction. Indeed, Claims 1, 10, and 17 claim a "host" that interfaces with "nonvolatile memory devices." Nothing in those independent claims or in the corresponding dependent claims suggests that the nonvolatile memory with which the claimed "host" indirectly interfaces is limited to flash memory or any other sub-category of nonvolatile memory. Moreover, nothing in the specification suggests an intention on the part of the inventor to assign a meaning to "host" (or more accurately, to that with which the "host" indirectly interfaces) narrower than its plain meaning. In fact, Toshiba is correct to point out that the specification supports the broader construction of "host" in that the preferred embodiment discloses that "[t]he nonvolatile memory devices may be flash, EEPROM or other type of solid state memory." ('918 patent, 4:22-25.)

The Court therefore declines to adopt Lexar's proposed construction of "host" in the '918 patent as it is unsupportably narrow. The Court instead finds that Toshiba's proposed construction is the correct one. Therefore, the Court finds that "host" as it appears in the '918 patent interfaces, through the controller, with nonvolatile memory.

III. "block"

A. Preliminaries

The claim term "block" appears in all six of the patents-in-suit as follows:

-> '638 patent, claims 1 (and dependent claims 2, 3, 5, 6, 7, 8, 9, 10, 11, and 12), 14 (and dependent claims 15, 16, 18, 19, 20, 21, 22, 23, 24, and 25), 27 (and dependent claims 28, 29, 31, and 34), and 37 (and dependent claims 38, 39, 40, and 41);

-> '997 patent, claims 1 (and dependent claims 3 and 4), 5 (and dependent claim 6), 7 (and dependent claims 8 and 9), 10, 11, 12, and 13 (and dependent claims 14 and 15);

-> '051 patent, claim 1 (and dependent claims 2, 3, 4, 5, 8, 9, 10, and 11) and 18 (and dependent claims 21, 22, 23, and 24);

-> '918 patent, claims 1 (and dependent claims 2, 3, 4, 5, 7, and 9), 10 (and dependent claims 11, 12, 13, 14, and 15), and 17 (and dependent claim 18);

-> '314 patent, claims 1 and 7; and

-> '138 patent, claims 1 (and dependent claims 4, 5, 9, and 10), 13 (and dependent claim 15), 16 (and dependent claims 17, 19, 21, 23, 24, and 28), 31 (and dependent claims 32, 34, 36, 38, 39, and 43), 46 (and dependent claims 47 and 50), and 51 (and dependent claims 53 and 54).

The construction of "block" in the '997 and the '051 patents does not appear to be in dispute. Therefore, the Court construes the claim term only in the '638, '918, and '314/'138 patents.

B. Construction

i. "block" in the '638 patent

Lexar's proposed construction:	**Toshiba's proposed construction:**	**Pretec's proposed construction:**
erasable storage for one or more sectors	a portion of memory that is separately programmable and erasable; those portions of memory containing data cannot be programmed.[FN6]	a set of like items handled as a unit.

FN6. In its brief, Toshiba did not explicitly propose a construction for "block" in the '638 patent but offered a construction of the term within its proposed construction for the '638 patent term "non-volatile storage blocks." The Court treats this as Toshiba's proposed construction for the '638 claim term "block." Toshiba's presentation at oral argument was consistent with this conclusion.

All three parties have proposed completely different constructions for "block" in the '638 patent. Lexar contends, as it does for the term in all patents in which it appears, that the claim term should be construed as "erasable storage for one or more sectors." Lexar suggests that the dispute (between Lexar and Toshiba) over the term "block" boils down to Toshiba's "insistence that the term 'block' cannot be anything that stores less than two sectors of data." While the Court notes that the debate here is about more than just the number of sectors contained in a block, the Court begins its analysis there.

Lexar proposes that a "block" in the '638 must contain one or more sectors and Toshiba maintains that because the '638 patent is the earliest of the patents-in-suit, a block in the '638 could not be understood by a person skilled in the art as containing more than a single sector. The parties agree, then, that a "block" in the '638 can contain a single sector. The dispute lies in whether a "block" can contain more than one sector in this patent. The lone reference to "sectors" in the '638 patent explains that in one preferred embodiment, a "multi-sector erase is necessary ...." ('638 patent, 4:62-65.) This strongly suggests that a block can be made up of more than one sector. The Court therefore finds that Lexar is right, that a "block" in the '638 contains one or more sector.

The Court now turns to evaluate the rest of the parties' respective constructions. Pretec accurately argues that Lexar's proposed cross-patent construction does not fit for "block" in the '638 patent. However, rather than suggest a construction of "block" specific to the '638 patent, Pretec, like Lexar, proposes a cross-patent construction. Pretec proposes a construction based on the non technical American Heritage dictionary definition of "block:" "a set of like items handled as a unit." But this construction is overly broad. Because a disputed claim term is to be given its ordinary meaning as understood by those skilled in the relevant art, "a general dictionary definition is secondary to the specific meaning of a technical term as it is used and understood in a particular technical field." Hoechst Celanese Corp. v. BP Chems. Ltd., 78 F.3d 1575, 1580 (Fed.Cir.1996). Here, "block" is a technological computer-related term having to do with data and memory storage. Pretec's general definition is out of place in this context.

The remaining dispute as to the proper construction of the term "block" is between Toshiba and Lexar. The Court first disposes of Toshiba's "those portions of memory containing data cannot be programmed" language. This portion of Toshiba's proffered construction is simply redundant. The language appears in the claims themselves and the Court need not load up a claim term with surrounding language. To do so would render the surrounding claim language superfluous. The Court therefore rejects this portion of Toshiba's proffered construction.

Toshiba and Lexar also disagree about the functions a block performs and whether such functions should be described in the construction of the claim term. Toshiba urges the Court to construe "block" as both "erasable" and "programmable." Toshiba contends that claim 1, which recites that "each block is selectively programmable and erasable" supports its construction. Lexar proposes that "block" be construed as erasable but not programmable. Lexar contends that a person of ordinary skill in the art would not construe "block" to be programmable as only sectors can be programmed. Toshiba agrees that sectors are what is programmable but contends that here, in the '638 patent, the earliest of the patents-in-suit, block and sector are functionally equivalent. This ties in with Toshiba's argument that a block in the '638 contains only a single sector. Because the Court has found that a block in the '638 can contain multiple sectors and because the parties agree that a block itself is not programmable, the Court finds that Toshiba's proposed "programmable" language is not properly part of the construction of the term "block." Therefore, the Court construes "block" in the '638 patent as: erasable storage for one or more sectors.

ii. "block" in the '918 patent

Lexar's proposed construction:	**Toshiba's proposed construction:**[FN7]

FN7. Pretec offers no proposed construction here. Pretec only proposes constructions for disputed terms in

the '638 and '051 patents.

erasable storage for one or more sectors	the smallest uniquely addressable physical group of nonvolatile memory cells that can be erased within a single nonvolatile memory device

The technology in the '918 patent concerns "super-blocks," larger groupings of single blocks to increase the speed with which blocks can be erased and freed up for programming new data. Lexar's briefs on "block" in the '918 patent are decidedly unhelpful. Lexar again proposes its one-size-fits-all construction for "block" and offers no citations from the '918 patent to support its construction. Instead, Lexar relies on the claim language of other unrelated patents to support its construction. The Court declines to examine those patents to construe a disputed claim term in the '918 patent.

As an initial matter, the Court notes that unlike the parties' dispute over "block" in the '314/'138 and the '638 patents, whether a block in the '918 contains one or more sectors does not appear to be in dispute. At oral argument, Lexar conceded that its proposed "one or more" language was intended to account for the older '638 patent, which expressly allows a block to contain only a single sector. The Court finds, then, that in the '918 patent, a block contains a plurality of sectors.

Toshiba's proposed construction is much narrower than Lexar's. Toshiba believes it important to acknowledge in the construction that a block (one part of a super block) is the smallest physical group of uniquely addressable nonvolatile memory cells that can be erased within a single nonvolatile memory device. As Lexar points out in its opening brief, Toshiba proposes to add limitations to the construction of "block" that speak to how a block might be used, not to what a block actually is. Moreover, the portion of the patent upon which Toshiba relies to support the "uniquely addressable" language, column 2, lines 32-40, refers to past inventions and does not support such a limitation in the construction of "block" in the '918. The additional limitations proposed by Toshiba are not warranted and the Court declines to incorporate them into the construction of "block."

For the foregoing reasons, the Court construes "block" in the '918 as erasable storage for a plurality of sectors.

iii. "block" in the '314/'138 patent

Lexar's proposed construction:	**Toshiba's proposed construction:**[FN8]

FN8. Pretec offers no proposed construction here. Pretec only proposes constructions for disputed terms in the '638 and '051 patents.

erasable storage for one or more sectors	a plurality of sectors identified by a virtual physical block address and expanding between two memory devices

Lexar again proposes its one-size-fits-all construction for "block." And again, the dispute between the parties on "block" in the '314/'138 patent turns, in large part, on the number of sectors a block contains. In its briefs, Lexar contends that a block can contain a single sector or more than one sector while Toshiba

proposes that "block" must, by definition, contain more than one sector. However, the independent claims in the '314/'138 recite that each block includes "a plurality of sectors" or "two or more sectors." ('314 patent, claims 1 & 7.) This language suggests that a block must contain more than one sector and that Lexar's proposed construction ignores the plain language of the claims. Nothing in the specification suggests that the inventor intended to act as his own lexicographer and define "block" differently. Indeed, Lexar admitted at oral argument that "we are not disputing or claiming that it can be one [sector] in the context of the '314 patent." The Court therefore agrees with Toshiba that "block" in the '314/'138 must contain a "plurality of sectors."

Toshiba suggests that the construction of "block" should account for the distinction made in the specification between a "sub-block" as that which is contained in a single nonvolatile memory device and a "block," which expands between two nonvolatile memory devices. The Court disagrees. To construe "block" as expanding between two nonvolatile memory devices would exclude a preferred embodiment. At column 4, lines 48-53, an embodiment of the invention is disclosed in which a block is contained within "a single nonvolatile memory device" rather than expanding across two such devices. The Court therefore declines to include that portion of Toshiba's proposed language in the construction.

The Court must now determine whether the proper construction of "block" in this patent is "identified by a virtual physical block address" as proposed by Toshiba. The Court finds that this portion of Toshiba's proposed construction is unnecessary. That a block is identified by a virtual physical block address need not be incorporated into the construction of the claim term. The additional verbiage is unnecessary and would improperly import a limitation from the preferred embodiment into the construction of the claim term.

For these reasons, the Court construes "block" in the '314/' 138 as erasable storage for a plurality of sectors.

IV. "sector"

A. Preliminaries

The claim term "sector" appears in four of the six patents-in-suit as follows:

-> '051 patent, claims 3 (and dependent claims 4, 6, 7, 9, and 17) and 18 (and dependent claims 19, 21, 24, 25, and 26);

-> '918 patent, claims 1, 10, and 17;

-> '314 patent, claims 1, 2 (and dependent claims 5 and 6), and 7; and

-> '138 patent, claims 1 (and dependent claims 2, 3, 4, 5, 7, 9, and 12), 13 (and dependent claims 14 and 15), 16 (and dependent claims 21, 22, 23, 24, 26, and 27), 31 (and dependent claims 36, 37, 38, 39, 41, and 42), 46 (and dependent claims 47, 48, and 49), and 51 (and dependent claims 52 and 53).

B. Construction

i. "sector" in the '051 patent

Lexar's proposed constr:	**Toshiba's proposed constr:**	**Pretec's proposed constr:**
a unit of 512 bytes or more,	a subdivision of the nonvolatile	the smallest unit of memory that can

including user data and/or overhead.	memory or the data stored therein	be read or written to at one time in a system

The parties' dispute over "sector" in the '051 patent centers around the amount of data a "sector" can contain. Lexar contends that a sector must contain at least 512 bytes while Pretec and Toshiba suggest that a sector can be much smaller. Toshiba and Pretec contend that Lexar's proposed construction is not supported by the '051 claim language. Indeed, the actual language of the claims at issue in the '051 patent do not provide a numeric limitation on the size of a sector. Toshiba argues that the '051 specification confirms that no numeric limitation was intended. In support of its argument, Toshiba points to that part of the specification describing the preferred embodiment which states that "a preferred sector size of 512 bytes is used in these examples whereas **other sectors sizes may be employed without departing from the scope and spirit of the present invention."** ('051 patent, 12:54-57 (emphasis added).) There is no indication that by "other sector sizes," the patentee only meant "larger sector sizes." Nothing in the patent indicates that the patented technology can only be used with an operating system in which the sector size is 512 bytes. Therefore, a sector, as recited in the '051 patent, can contain 512 bytes, fewer than 512 bytes, or more than 512 bytes and, accordingly, the Court rejects this aspect of Lexar's proposed construction.

Having resolved the question of the size of a "sector" in the '051, the Court must now address the remaining portions of the parties' proposed constructions. Lexar's proposed construction does not actually articulate a definition of the term "sector." Lexar does not explain whether a "sector" is a unit of memory or of data or some other type of "unit." Toshiba and Pretec do each provide an actual construction of "sector," but neither party provides the Court with any support for the language it chose. Toshiba contends that a "sector" is a "subdivision of the nonvolatile memory or the data stored therein;" Pretec argues that a "sector" is the "smallest unit of memory that can be read or written to at one time in a system." Toshiba's proposed construction is overly broad. Pretec's proposed construction does not appear to match how a person of ordinary skill in the art would understand "sector" here. As Lexar argued at the claim construction hearing, the smallest unit of memory that can be read or written at one time here is a byte and no one skilled in the relevant art would ever equate a "sector" with a byte. At oral argument, Pretec did not rebut Lexar's argument, instead focusing on the number of bytes in a sector. The Court therefore rejects Pretec's proposed construction and construes "sector" in the '051 as follows: a unit of memory containing user data and overhead.

ii. "sector" in the '918 patent

Lexar's proposed constr:	**Toshiba's proposed constr:**[FN9]

FN9. Pretec offers no proposed construction here. Pretec only proposes constructions for disputed terms in the '638 and '051 patents.

a unit of 512 bytes or more, including user data and/or overhead.	a subdivision of the nonvolatile memory or the data stored therein

The parties' dispute over the term "sector" in the '918 patent is the same. Lexar suggests that a "sector" is only those units that are 512 bytes in size or greater while Toshiba suggests that a sector can be any "subdivision of the nonvolatile memory." Lexar points to technical dictionary definitions to support its

contention that a person of ordinary skill in the art would have understood a sector, at the time of the invention, as 512 bytes in size. While the Court notes that the proffered dictionary definitions indeed indicate that a sector is "typically" 512 bytes, the claim language of the '918 patent does not describe a "sector" as having only 512 bytes of data or more nor does the specification indicate that the inventor intended to so limit the meaning of "sector." In fact, the '918 specification teaches that although "[i]n PC applications, a block of information is typically a sector as employed in conventional hard disk drives, with each sector typically having 512 bytes of data, ... **other-sized sectors may be similarly employed.**" ('918 patent, 6:61-64 (emphasis added).) To limit "sector" to 512 bytes or more would exclude an embodiment of the invention discussed in the specification. The Court declines to limit "sector" to 512 bytes.

Toshiba proposes that "sector" in the '918 be construed as "a subdivision of the nonvolatile memory or the data stored therein ." As discussed with regard to the '051 patent *supra,* Toshiba's proposed construction seems as if it could encompass the claim term "block," which is also a "subdivision of the nonvolatile memory." Therefore, the Court rejects it as overly broad. The Court instead construes "sector" as it did in the '051 patent: a unit of memory containing user data and overhead.

iii. "sector" in the '314/'138 patent

Lexar's proposed construction:	**Toshiba's proposed construction:**[FN10]

FN10. Pretec offers no proposed construction here. Pretec only proposes constructions for disputed terms in the '638 and '051 patents.

a unit of 512 bytes or more, including user data and/or overhead.	a subdivision of the nonvolatile memory or the data stored therein

Again, the parties disagree about how much data a sector can contain. And again, Lexar proposes to improperly limit a "sector" in the '314/'138 patent to a unit of 512 bytes or more when the claim language does not so limit sector size and when the specification does not reflect an intent on the part of the patentee to act as his own lexicographer. The '314/'138 specification notes that "[i]t is common in the industry for each sector to include 512 bytes of user data plus overhead information." ('314 patent, 7:42-44; '138 patent, 7:34-36.) However, as in the '051 and '918 patents, the '314/'138 specification explains that although the preferred embodiment employs sectors of 512 bytes of user data and 16 bytes of overhead, "a sector may include other numbers of bytes of information." ('314 patent, 7:44-47; '138 patent, 7:36-40.) That the Preferred Embodiment section permits sectors sizes other than the 512 bytes counsels against limiting a sector's size to 512 bytes plus overhead. Therefore, the Court construes "sector" in the '314/'138 as a unit of memory containing user data and overhead.

V. "super-block"-'918 patent

The claim term "super-block" appears in only one of Lexar's patents-in-suit: the '918 patent, in independent claims 1 (and dependent claims 3, 4, 5, 7, and 9), 10 (and dependent claims 13, 14, and 15), and 17. Lexar and Toshiba respectively propose that "super block" be construed as follows:

Lexar's proposed	**Toshiba's proposed**

construction:	**construction:**[FN11]

FN11. Pretec offers no proposed construction here. Pretec only proposes constructions for disputed terms in the '638 and '051 patents.

Two or more blocks that are used to store data, the two or more blocks having addresses that are correlated with a group of logical block addresses that is determined by the number of sectors in the blocks.	A number of blocks that are in like locations of the different nonvolatile memory devices and residing in parallel with respect to each other.

In the Preferred Embodiment section of the '918 patent, a particular embodiment of the invention is described and then the following language appears:

In this respect, a 'super' block is defined by a number of blocks that are in like locations of the different nonvolatile memory devices and residing in-parallel with respect to each other.

('918 patent, 9:11-15.) Toshiba contends that this language is an expression of the patentee's intention to act as his own lexicographer regarding "super block" and that it should serve as the construction of the term throughout the patent. Indeed, where an inventor defines a claim term "with reasonable clarity, deliberateness, and precision," that definition is understood to control the construction of the claim term. Teleflex, Inc. v. Ficosa N. Am. Corp., 299 F.3d 1313, 1325 (Fed.Cir.2002). Here, however, the language relied upon by Toshiba, at column 9, lines 12-15 of the patent, is not such a definition. The "in this respect" language indicates that what follows is relevant only to a preferred embodiment of the invention and to adopt it as the universal construction of "super block" would be too restrictive as it would improperly import limitations from the preferred embodiment into the construction of the claim term itself. The Court therefore rejects Toshiba's proposed construction of "super block." The Court also notes that, as Lexar points out, to adopt Toshiba's construction would exclude a preferred embodiment, represented in Figure 5, which shows blocks positioned vertically, not "in parallel" with one another. This the Court declines to do.

The Court finds that Lexar's proposed construction here is the correct one. The Court therefore construes the term "super-block" as follows: two or more blocks that are used to store data, the two or more blocks having addresses that are correlated with a group of logical block addresses that is determined by the number of sectors in the blocks.

VI. "program"

A. Preliminaries

The parties identified "program" as one of the disputed terms to be construed by the Court. The Court first notes that the term "program," as such, does not appear in any of the patents. However, variations on the term ("programmable," "programmed," "unprogrammed," and "programming") appear in three of the six patents-in-suit as follows:

-> '638 patent, claims 1 (and dependent claims 8 and 9), 14 (and dependent claims 20 and 21), 27, 37;

-> '997 patent, claims 5 and 11; and

-> '314 patent, claims 1 and 7.

There appears to be no dispute regarding the construction of "program" in the '997 patent. The Court therefore only construes the claim term in the ' 638 and the '314.

B. Construction

i. "program" in the '638 patent

Lexar's proposed construction:	**Toshiba's proposed construction:**	**Pretec's proposed construction:**
the operation of injecting electronsonto the floating gate of the memory cell.	-none-	Write

Only Lexar and Pretec disagree about the proper construction of "program" in the '638; Toshiba does not propose a construction. Pretec proposes that "program" should simply be construed as "write." Lexar, however, argues that programming is just one part of the write cycle and that the two terms are not synonymous. Lexar relies on the IEEE treatise for its proposed construction, arguing that the IEEE provides the ordinary meaning of the term "program" and that the patent itself provides no indication that a different meaning was intended. The Court agrees with Lexar here.

Both the 1991 and 1998 versions of the IEEE Standard Definitions and Characterization of Floating Gate Semiconductor Arrays indicates that "program" means "the operation of injecting electrons onto the floating gate of the memory cell." The IEEE definition is relevant, then, to the construction of "program" in the '638 patent, the application for which was filed in 1993. Additionally, Lexar relies on Figure 5, which indicates that programming is one part of the write cycle but is not synonymous with "write." The Court agrees with Lexar. Pretec's proposed construction, "write," is incorrect. Column 2, lines 48-52 indicate that in the erase cycle, each bit is programmed and then the bits are erased in a block. This suggests that writing is something different from programming and that Lexar is right. The Court therefore construes "program" as the operation of injecting electrons onto the floating gate of the memory cell.

ii. "program" in the '314 patent

Lexar's proposed construction:	**Toshiba's proposed construction:**[FN12]
the operation of injecting electrons onto the floating gate of the memory cell.	issuing a write command, followed by address and data

FN12. Pretec offers no proposed construction here. Pretec only proposes constructions for disputed terms in the '638 and '051 patents.

Toshiba has failed to propose a construction for the disputed claim term "program" in the '314. However, Toshiba *does* propose a construction for the disputed claim term "programming ... simultaneously." The Court therefore considers "issuing a write command, followed by address and data," the first portion of

Toshiba's proposed construction of "programming ... simultaneously," to be Toshiba's proposed construction for "program" here.

Lexar again urges the Court to adopt the meaning of "program" offered in the IEEE treatise. Toshiba contends that because the '314 contains no discussion of injecting electrons onto floating gates as "programming," the IEEE definition is inapplicable. Toshiba instead proposes that the proper construction is "issuing a write command, followed by address and data." The Court first rejects the "followed by address and data" portion of Toshiba's construction. This excess verbiage is simply unnecessary and the Court declines to include it in the construction. Toshiba's remaining language, "issuing a write command," is, as in the '638, not the proper construction. Claim 1 of the '314 patent discusses programming and Claim 2 discusses writing. If the two processes were synonymous, there would be no need for the two separate claims. Programming is clearly a phase of the larger write cycle. The Court therefore agrees with Lexar and construes "program" as follows: the operation of injecting electrons onto the floating gate of the memory cell.

VII. "writing ... simultaneously" - '314 patent **claim 2**/'138 patent **claims 16, 31, 46**

Lexar's proposed constr:	**Toshiba's proposed constr:**[FN13]
initiating a write command to two or more blocks at the same time.	issuing a write command, followed by address and data for two or more sectors at the same time and exactly coincident

FN13. Pretec offers no proposed construction here. Pretec only proposes constructions for disputed terms in the '638 and '051 patents.

The parties' dispute over "writing ... simultaneously" is similar to the "program" dispute. Lexar simply proposes that the claim phrase should be construed as "initiating a write command to two or more blocks at the same time." Toshiba, however, like its proposed construction of "program," suggests that "writing ... simultaneously" means "issuing a write command, followed by address and data for two or more sectors at the same time and exactly coincident."

First, the Court notes that again, Toshiba's proposed "followed by address and data" language is superfluous and need not be included in the construction of the term. Second, the "exactly coincident" language proposed by Toshiba is a limitation that is not required by the "simultaneously" portion of the disputed claim term. Lexar is right that while the initial issuance of a write command must occur simultaneously in both write cycles, each and every step of the write cycles need not occur simultaneously. Specifically, as Lexar persuasively explained at oral argument, the programming phase of the write cycle, represented by the cross hatches in Figure 9, can take varying amounts of time depending on what is being programmed. Each phase of the write cycle, therefore, need not occur simultaneously. The cycles need only start at the same time.

The parties' proposed constructions also differ in that Lexar suggests that the write command is issued "to two or more blocks," while Toshiba suggests the write command is issued "for two or more sectors." Neither party addressed this particular difference between their proposed constructions in their briefs or at oral argument and therefore, the Court, in construing this term, opts to include a portion of the language used by

the claim itself. The language represented by the ellipsis, as it appears in the claims themselves, is "writing two or more sectors of information to a row of the nonvolatile memory unit simultaneously." Therefore, the Court construes "writing ... simultaneously" as follows: initiating a write command to two or more sectors within two or more (row) blocks at the same time.

VIII. "logical block address"

A. Preliminaries

The claim phrase "logical block address" or "LBA" appears in four of the six patents-in-suit as follows:

-> '638 patent, claims 1 (and dependent claims 12, 13, and 14) and 25 (and dependent claim 26, 27), 37, and 41;

-> '051 patent, claims 1 (and dependent claims 2, 3, 5, and 12) and 18 (and dependent claims 20, 21, and 23);

-> '314 patent, claim 7; and

-> '138 patent, claims 1 (and dependent claim 2), 13, 21, and 36.

There appears to be no dispute over this claim phrase as it appears in the ' 638 and the '314/'138 patents since Toshiba has not offered a proposed construction. The Court therefore only construes "logical block address" in the '051 patent.

B. Construction of "logical block address" in the '051 patent

Lexar's proposed construction:	**Toshiba's proposed construction:**	**Pretec's proposed construction:**
A value provided by the host for addressing a sector	Logical address provided by the host to the controller for identifying information blocks	none

The parties' dispute over "logical block address" in the '051 patent, like "controller," focuses more on that with which the LBA interfaces rather than the LBA itself. Lexar contends that the LBA identifies sectors while Toshiba argues that the LBA identifies blocks. In its Opening Brief, Lexar cites claim language from the '314 patent to support its construction. As explained above, '314 patent claim language is inapposite in construing a common term in the '051 patent. Although the two patents share, at least in part, the same parent application and each patent's prosecution history may be relevant for the construction of common terms, common terms are not necessarily construed consistently. Toshiba contends that the LBA identifies information blocks and directs the Court to the language of claims 1 and 18 of the '051 which expressly says that a group of LBAs "identif[ies] one or more information blocks." ('051 patent, 18:42-43; 20:29-30.) In its Reply Brief and at oral argument, Lexar suggested two reasons that Toshiba's proffered construction is incorrect. First, the claim language referenced by Toshiba is incomplete in that what follows the cited language clarifies that what an LBA really identifies is a sector. And second, the host, from which the LBA issues, communicates only in terms of sectors, not blocks. The Court agrees in part.

Indeed, the language that follows that cited by Toshiba reflects that what an LBA identifies is more complex than the initial phrase suggests. LBAs "identify [ ] one or more information blocks to be accessed in the

nonvolatile memory, each of the information blocks including a plurality of N sectors." Additionally, the Court agrees that the host, which provides the LBA, speaks in terms of sectors, not blocks. Lexar's contextual argument in this regard is useful, but not dispositive because it would be improper to ignore the claim language itself which does say that the LBA identifies information blocks. Therefore, the Court construes "logical block address" in the '051 as: address provided by the host to the controller for identifying blocks which contain a plurality of N sectors.

IX. "physical block address"-'051 patent

Although the disputed claim phrase, "physical block address" or "PBA" appears in several of the patents-in-suit, the parties appear only to disagree about its proper construction in the context of the '051 patent. Their respective proposed constructions for the claim phrase are as follows:

Lexar's proposed constr:	**Toshiba's proposed constr:**	**Pretec's proposed constr:**
physical addresses of sectors of data in the nonvolatile memory	physical addresses of sectors of data	-none-

Lexar and Toshiba nearly agree on the proper construction of "physical block address." The parties only disagree with respect to the phrase Lexar adds to the end of the otherwise identical construction: "in the nonvolatile memory." Pretec offers no construction for this "disputed" claim term (although it appears that Pretec must have construed this term at some point because Toshiba references Pretec's proposed construction). Toshiba argues that because sectors are, by definition, in the nonvolatile memory, the construction of PBA need not include the phrase. The Court agrees and notes that Lexar, in its Reply Brief, appears to have dropped the proposed excess verbiage. The Court therefore construes "physical block address" as physical addresses of sectors of data.

X. "virtual block address"-'051 patent

The claim term "virtual block address" appears in claims 2, 3, and 18 of the '051 patent. The parties propose constructions of the disputed claim phrase as follows:

Lexar's proposed construction:	**Toshiba's proposed construction:**	**Pretec's proposed construction**
Value to indicate a block location	*[NOTE: Toshiba actually construes "first virtual block address"].* An address of a physical block in the nonvolatile memory where original information of an information block is stored.	The address of a simulated block that holds the address of a physical block.

The Court finds that Lexar's proposed construction is the correct one for this term.. Toshiba's construction is flawed in that the use of the word "address" does not clarify what an "address" in the disputed claim phrase is. The Court finds that Lexar's proposed language, "value to indicate," is more useful here. The Court also finds that much of Toshiba's proposed language, such as "in the nonvolatile memory," is surplusage that fails to clarify what a "virtual block address" is. Additionally, referencing "a physical block" provides an overly narrow construction of "virtual block address" because the VBA does more than indicate a physical block. As Lexar discussed at oral argument, the VBA puts the information block back together and to limit its

function to a physical block "depriv[es] it of some part of its function." (Claim Construction Hearing Transcript at 96:17-18.)

The Court also rejects Pretec's proposed construction of "virtual block address." Again, using "address" to define "address" is not helpful. Additionally, Pretec's proposal to include "simulated" adds a limitation to the claim phrase that does not exist in the claims themselves. Therefore, the Court adopts Lexar's proposed construction of "virtual block address:" value to indicate a block location.

XI. "information block"-'051 patent

The disputed claim term "information block" appears only in the '051 patent. The parties propose constructions of "information block" as follows:

Lexar's proposed construction:	**Toshiba's proposed construction:**	**Pretec's proposed construction:**
initial construction: data organized into units of blocks *compromise construction offered at hearing:* a plurality of sectors that are logically associated with a group of LBAs	an amount of data logically associated with a host provided LBA	an individually erasable unit of data that may be larger than one sector in size

The invention contemplated in the '051 patent links, using an LBA, already-programmed sectors that have been designated for erasure into a single "information block" so that the ready-for-erasure sectors can be erased together. The parties propose three separate constructions for this claim phrase and here, the Court finds that a combination of the three proposed constructions best defines the term at issue here.

As Lexar points out, Toshiba's proposed language "an amount of data" adds nothing to the construction of the claim phrase because the *amount* of data is simply not at issue. Furthermore, the construction of "information block" need not explain that the LBA is provided by a host. To do so is unnecessary as it is made clear by surrounding claim language as well as in the construction of LBA itself Pretec's proposed construction is a better fit because an "information block" is made up of sectors that contain data to be erased. But as Lexar points out, Pretec's construction can equally encompass a mere "block." The portion of Pretec's construction that accounts for the information block's erasability should be included but the rest of the proffered construction does not accurately define the term.

The Court now turns to Lexar's proposed construction. Lexar initially proposed that the claim phrase "information block" should be construed as "data organized into units of blocks," but at oral argument, Lexar offered a compromise construction: "a plurality of sectors that are logically associated with a group of LBAs." The Court agrees with Toshiba that Lexar's original proposed construction provides no meaning. (Claim Construction Hearing Transcript at 105.) However, Lexar's compromise construction deserves further scrutiny even though neither Toshiba nor Pretec directly addressed it at oral argument. The proposed compromise construction accounts for the portions of data included in the information block and explains how they are linked to one another. Lexar's proposed construction is better in that regard. However, Lexar's construction does not account for the erasability of the "information block." Because the purpose behind the organization of such a block is erasure, it would appear significant to include this limitation in the construction itself as well, as Pretec does. The Court finds that Lexar's proposed compromise construction,

with the erasure function added in as discussed *supra,* works best. The Court therefore construes "information block" as a plurality of sectors that are logically associated with a group of LBAs for erasure.

XII. "avoids transfer"-'051 patent

The disputed claim phrase "avoids transfer" appears in claims 1 and 18 of the '051 patent. The parties propose that the disputed claim phrase be construed as follows:

Lexar's proposed constr:	**Toshiba's proposed constr:**	**Pretec's proposed constr:**
none-[*but contests Toshiba's proposed construction*]	The controller never transfers the original sectors of the information block during a host rewrite request.	Prevents transfer from happening.

For the most part, Toshiba and Pretec agree on the construction of "avoids transfer" and although Lexar disputes Toshiba's construction as the proper one, it does not offer its own proposed construction. The Court finds, however, that Lexar is right in that "avoids transfer" should be construed in accordance with its ordinary meaning. Pretec's proposed construction, "prevents transfer from happening," does not illuminate the meaning of "avoids transfer" in the context of the claim at issue. Toshiba's proposed construction is not consistent with the ordinary meaning of the claim phrase because its use of "never transfers" is likewise inaccurate regarding the meaning of the claim language in context. Claim 1 says that the controller "avoids transfer of a particular information block from one location to another block location each time the host requests that a portion of the particular information block be re-written." ('051 patent, 18:54-57 (emphasis added).) The claim language does not say that transfer cannot occur or that it never occurs; it says that transfer is avoided each time the host requests a re-write. That way, as Lexar argued at the claim construction hearing, the invention is more efficient and prevents wearing out the nonvolatile memory device. (Claim Construction Hearing Transcript at 100). Moreover, the description of the preferred embodiment explains that "the overhead associated with an erase cycle is avoided for each write to the memory except for periodically." ('051 patent, 8:8-10 (emphasis added).) While the court is not to import limitations from a preferred embodiment into the claims themselves, a construction that excludes a preferred embodiment is rarely, if ever, correct. Vitronics, 90 F.3d at 1538-84. Therefore, the court rejects Toshiba's proposed construction. Having considered the claim language in context, the court construes "avoids transfer" to mean: the controller, at times, avoids the transfer of a particular information block during a host rewrite request.

XIII. "being operative to access portions of an information block stored in more than one block locations"-'051 patent

Pretec contends that this claim is invalid. The Court declines to determine the validity of the claim at this juncture. In the alternative, Pretec argues that the claim is a means-plus-function claim and offers a proposed construction of the claim in conformity therewith. FN14 Lexar disagrees.

FN14. Toshiba took no position on the construction of this claim in its brief, but at oral argument, Toshiba represented to the Court that it "agree[s] with Pretec's position." (Claim Construction Hearing Transcript at 29.)

A means-plus-function claim is a special type of patent claim provided for in 35 U.S.C. section 112, paragraph 6, which provides:

An element in a claim for a combination may be expressed as a means or a step for performing a specified function without the recital of structure, material, or acts in support thereof, and such claim shall be construed to cover the corresponding structure, material, or acts described in the specification and equivalents thereof.

35 U.S.C. s. 112, para. 6. Under this provision, an inventor can describe an element of the invention by the result accomplished or the function served, rather than by describing the item or element to be used. Warner-Jenkinson Co., Inc. v. Hilton Davis Chemical Co., 520 U.S. 17, 27, 117 S.Ct. 1040, 137 L.Ed.2d 146 (1997). When using means-plus-function language, "[t]he applicant must describe in the patent specification some structure which performs the specified function." Valmont Industries, Inc. v. Reinke Mfg. Co., Inc., 983 F.2d 1039, 1042 (Fed.Cir.1993). A structure disclosed in the specification is only deemed to be "the corresponding structure" if the specification clearly links or associates that structure to the function recited in the claim. Kahn v. General Motors Corp., 135 F.3d 1472, 1476 (Fed.Cir.1998). The duty to link or associate structure in the specification with the function is the *quid pro quo* for the convenience of employing the means-plus-function format. *Id*.

Generally, means-plus-function claims use the word "means" and doing so "invokes a rebuttable presumption that section 112, paragraph 6 applies." Apex Inc. v. Raritan Computer, Inc., 325 F.3d 1364, 1371 (Fed.Cir.2003) (citation omitted). "By contrast, a claim term that does not use 'means' will trigger the presumption that section 112, paragraph 6 does not apply" and that the claim is not a means-plus-function claim. *Id*. "The term 'means' is central to the analysis." *Id*. at 1372 (citation omitted). Where "means" language is not used, the presumption that the claim is not a means-plus-function claim is rebutted if it is shown, by a preponderance of the evidence, that "the claim term fails to 'recite sufficiently definite structure' or else recites a 'function without reciting sufficient structure for performing that function." *Id*.

Here, Pretec argues that this claim is a means-plus-function claim even though the claim does not contain the "means" language. Lexar argues that the claim is not means-plus-function because the claim properly recites a structure to perform the function of accessing portions of an information block. The parties' proposed constructions are as follows:

Lexar's proposed construction:	**Toshiba's proposed constr:**	**Pretec's proposed construction:**
[*not a means-plus-function claim*]	none	[*a means-plus-function claim*]
the controller can access portions of data organized into units of blocks stored in more than one location of a block		*function:* functioning to read portions of an information block that are stored in various block locations *associated structure:* '051 patent, 8:57-64; '051 patent, 10:05-13; '051 patent, 12:05-11 and Fig 12; '051 patent, 12: 29-42 and Fig 12.

Pretec suggests that the claim language at issue fails to recite sufficiently definite structure that a person of ordinary skill in the art would recognize and that the claim must therefore reference a structure in the

specification to give the claim meaning. Lexar argues that this is not a means-plus-function claim because the language just before the language at issue references "the controller" as the structure that performs the function described in the language at issue and Lexar contends that a controller is undisputedly a device. The question is, however, whether the controller would be understood by a person of ordinary skill in the art as providing the structure for performing the functions described in the claim. For the following reasons, the Court finds that it would and that the claim at issue is not a means-plus-function claim.

Pretec has the burden, here, of rebutting the presumption that the claim is not means-plus-function and Pretec has failed to meet that burden. First, as Lexar points out, both Pretec and Lexar agree that the controller, one of the disputed claim terms construed in this Order, is, at its core, "a device," and the Court agrees. (*See* "controller" discussion *supra*.) Second, Pretec's argument that the claim would be invalid if the controller were the claimed structure because the claim would be "in effect a prohibited single means claim because the controller is the structure that performs each and every functional limitation in the claim" fails. Lexar properly contends that this presupposes that the claim is a means-plus-function claim so that Pretec's reasoning is circular. Third, Pretec contends that prior art controllers did not perform the claimed function so the presumption should not apply. This argument has no merit because, as Lexar argues, the fact that the claimed invention is novel and nonobvious does not render it a means-plus-function claim. The presumption is that the claim is not means-plus-function and Pretec has not met its burden of rebutting the presumption. Therefore, the Court finds that the presumption prevails and that the claim at issue is not a means-plus-function claim. However, having determined that the claim language at issue is not a means-plus-function claim, the Court is unable to provide a construction of this term because the briefs submitted by the parties do not meaningfully assist the Court in arriving at a proper construction. Should the parties seek further construction of this term, the Court will permit supplemental briefing on this issue.

XIV. "directly correlating"-'638 patent **claim 37**

Lexar's proposed constr:	**Toshiba's proposed construction:**	**Pretec's proposed construction:**
without any intermediate mapping or calculation	a logical address assigned to a single block containing superseded data must be directly associated with the physical address of the block containing the corresponding updated data in one map, without any intermediate mapping or calculation, where the map is not uniquely addressable by the logical address	linking, in one map, without any intermediate mapping or calculation

Lexar first suggests that this term need not be construed. In the alternative, Lexar proposes the simple construction "without any intermediate mapping or calculation." Pretec, citing the '638 prosecution history, proposes a similar construction but with two additional limitations: first, to include the word "linking" and second, that the linking occur "in one map." The Court addresses "linking" first. Lexar's proposed construction does not provide an explanation of the word "correlating" (presumably because it finds the term needs no additional construction). To substitute Lexar's proposed construction into claim 37 would make it incomprehensible. "Linking" should therefore be included in the construction of "directly correlating."

With respect to Pretec's proposed "in one map" limitation, Lexar argues that the Examiner said nothing in the Office Action (wherein "directly" was added to claim 37 reciting the step of "correlating a logical address assigned to a block of superseded data to a physical address of a corresponding block of updated data") that would require direct correlation to occur in one map. The Court agrees. The amendment to claim

37, adding "directly," distinguished the prior art of Ban and Wells because that prior art required an intermediate mapping step. Adding "directly" satisfied the Examiner that the intermediate mapping step was unnecessary in the patentee's invention and thereby distinguished from the prior art. The Examiner explained that "[w]ith directly correlating, no intermediate address mapping or table walking is required ... which contrasts with the teachings of Ban and Wells et al." ('638 file history, paper 12 at 3-4.) Neither the Examiner nor the patentee suggested that the direct correlation occur in one map and that that feature is what sets the patentee's invention apart from prior art. The mere fact that there is no intermediate step is what makes this patented invention different. The Court rejects Pretec's proposed "in one map" limitation.

Toshiba proposes a complex 47-word construction for "directly correlating." Pretec does not address Toshiba's construction at all and Lexar only addresses it in its Opening Brief. There, Lexar disagrees with Toshiba's construction but only on the grounds that the construction is too long and includes restrictions and requirements that are not present in the claim. Toshiba contends that its construction is the proper because the specification and prosecution history in an unrelated patent, the '313 patent, distinguished the '638 patent by explaining that the '638 "includes a programmable map" and "does not disclose a correlation map that is addressable by logical block addresses." Toshiba's reliance here on a wholly unrelated patent and its file history is misplaced and the Court fins that the '313 patent does not limit the construction of this term. The '638 patent claim language and its own prosecution history explain adequately that the proper construction of "directly correlating" here is as follows: linking without any intermediate mapping or calculation.

CONCLUSION

For the foregoing reasons, the Court construes the disputed claim terms as follows:

1. "controller"-'638 patent: *a device that interfaces between a host and nonvolatile memory*

2. "controller"-'997 patent: *a device that interfaces between a host and flash memory*

3. "controller"-'051 patent: *a device that interfaces between a host and nonvolatile memory*.

4. "controller"-'314/'138 patent: *a device that interfaces between a host and nonvolatile memory*

5. "host"-'997 patent: *interfaces, through the controller, with flash memory*

6. "host"-'051 patent: *interfaces, through the controller, with nonvolatile memory*

7. "host"-'314/'138 patent: *interfaces, through the controller, with nonvolatile memory*

8. "host"-'918 patent: *interfaces, through the controller, with nonvolatile memory*

9. "block"-'638 patent: *erasable storage for one or more sectors*

10. "block"-'918 patent: *erasable storage for a plurality of sectors*

11. "block"-'314/'138 patent: *erasable storage for a plurality of sectors*

12. "sector"-'051 patent: *a unit of memory containing user data and overhead*

13. "sector"-'918 patent: *a unit of memory containing user data and overhead*

14. "sector"-'314/'138 patent: *a unit of memory containing user data and overhead*

15. "super-block"-'918: *two or more blocks that are used to store data, the two or more blocks having addresses that are correlated with a group of logical block addresses that is determined by the number of sectors in the blocks.*

16. "program"-'638 patent: *the operation of injecting electrons onto the floating gate of the memory cell*

17. "program"-'314 patent: *the operation of injecting electrons onto the floating gate of the memory cell*

18. "writing ... simultaneously"-'314/'138 patent: *initiating a write command to two or more sectors within two or more (row) blocks at the same time.*

19. "logical block address"-'051 patent: *address provided by the host to the controller for identifying blocks which contain a plurality of N sectors*

20. "physical block address"-'051 patent: *physical addresses of sectors of data.*

21. "virtual block address"-'051 patent: *value to indicate a block location*

22. "information block"-'051 patent: *a plurality of sectors that are logically associated with a group of LBAs for erasure*

23. "avoids transfer"-'051 patent: *the controller, at times, avoids the transfer of a particular information block during a host rewrite request.*

24. "being operative to access portions of an information block stored in more than one block locations"-'051 patent: NOT A MEANS-PLUS-FUNCTION CLAIM

25. "directly correlating"-'638 patent: *linking without any intermediate mapping or calculation.*

IT IS SO ORDERED.

N.D.Cal.,2005.
Toshiba Corp. v. Lexar Media, Inc.