United States District Court,
N.D. California.

SILICONIX INCORPORATED, a Delaware corporation,
Plaintiff.
v.
ALPHA AND OMEGA SEMICONDUCTOR INCORPORATED, a California corporation, and Alpha and Omega Semiconductor Limited, a Bermuda corporation,
Defendants.

No. C 03-4803 WHA

Sept. 10, 2004.

David Eiseman, Albert P. Bedecarre, Patrick C. Doolittle, Quinn Emanuel Urquhart Oliver & Hedges, LLP, San Francisco, CA, for Plaintiff.

Duo Chen, George Hopkins Guy, III, Bas De Blank, Stephen N. Adams, Orrick Herrington & Sutcliffe LLP, Menlo Park, CA, for Defendants.

CLAIM CONSTRUCTION ORDER

WILLIAM ALSUP, **District Judge.**

INTRODUCTION

This is the claim-construction order for the two patents in suit, United States Patent Nos. 4,767,722 and 5,034,785. This order addresses the six disputed terms and phrases selected by the parties. A technology tutorial, a full round of briefing and a *Markman* hearing preceded this order,

STATEMENT

Plaintiff Siliconix Incorporated claims to be the world's leading manufacturer of power MOSFETs (metal-oxide-semiconductor, field-effect transistors). Defendants Alpha and Omega Semiconductor, Incorporated, and Alpha and Omega Semiconductor, Limited, (collectively "AOS") manufacture competing MOSFETs. Siliconix contends that AOS infringes Claim 10 of the '722 patent and Claims 1, 2, 3, 8, 14, 15, 16, and 17 of the '785 patent.

The '722 patent, entitled "Method for making Planar Vertical Channel DMOS Structure," claims the methods of making a particular type of semiconductor device, a DMOS transistor with a vertical gate and a planar surface (Col.2:16-20). The purported improvement was that this method provided a flat surface for all masking steps thereby facilitating the manufacture of multiple DMOS transistors.

The '785 patent, entitled "Planar Vertical Channel DMOS Structure," claims the devices produced by using

the methods described in the '722 patent. The '785 patent is a continuation-in-part of an abandoned divisional of the '722 patent. Thus, the '785 patent shares virtually identical specification and figures with the '722 patent. The only major difference is the addition of a Figure 10 and a paragraph describing this figure. The '785 patent purportedly improves over the prior art by reducing the space between the gate regions as to allow for higher packing density, *i.e.,* the same number of cells takes up less space than in the prior art (Col.5:17-19).

ANALYSIS

Though parties disagree over many terms in the two patents in suit, they have jointly selected six disputed terms or phrases to be construed at this time. They are: (1) "planar," (2) "etching a plurality of grooves so that each groove extends through an associated one of said regions within said plurality of semiconductor regions, through said second region and into said first region," (3) "insulating layer formed over said gate structure, said insulating layer being substantially coplanar with the top surface of said third region," (4) "second insulating layer formed over said gate structure, said second insulating layer being substantially coplanar with a top surface of said second plurality of semiconductor regions," (5) "groove laterally surrounding said first and second plurality of semiconductor regions," and (6) "means for electrically contacting the top surface of said third region."

1. "planar"

The term "planar" is used throughout the specification and claims of the ' 722 patent. For example in Claim 10, the pertinent language states (emphasis added):

forming an insulating layer on said conductive material so that the top surface of said semiconductor device is **planar;** and ...

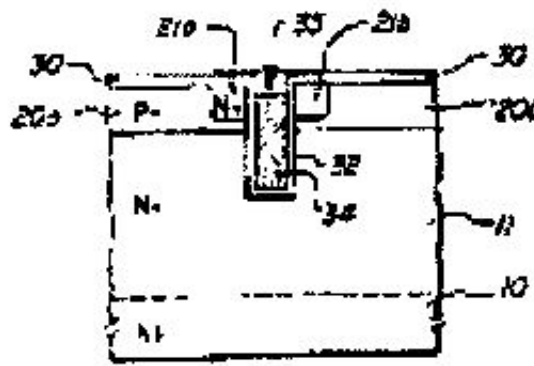
Siliconix proposes that "planar" should be construed as "an essentially flat surface, meaning flat enough for any subsequent masking steps while still allowing contact to be made to the gate region." AOS contends that the disputed term means absolutely flat.

This order holds that "planar" means as flat as practicable. This construction is grounded in the specification and the prosecution history. The patentee may act as his own lexicographer and use the specification to supply implicitly or explicitly definition for terms. Beckson Marine, Inc. v. NFM, Inc., 292 F.3d 718, 723 (Fed.Cir.2002). The specification provides that "the top surface of the oxidized portion 35 above gate 34 forms an essentially flat (planar) surface" (Col.4:40-43). With such use of parenthetical, the specification attempts to define "planar" as meaning "flat."

Yet, the specification and the prosecution history depict planar surfaces which are not absolutely flat. For example, Figure 4f reveals that the "planar" surface is not absolutely or geometrically flat. Instead, the surface has a slight bump over the gate structure 35. Though limitations from the specification should not be imported into the claim, claims must be read in view of the specification and the diagrams. *See* Leibel-Flarsheim Co. v. Medrad, Inc., 358 F.3d 898, 904 (Fed.Cir.2004). A claim construction excluding a preferred embodiment "is rarely, if ever correct and would require highly persuasive evidentiary support." Vitronics Corp. v. Conceptronic, Inc., 90 F.3d 1576, 1583 (Fed.Cir.1996).

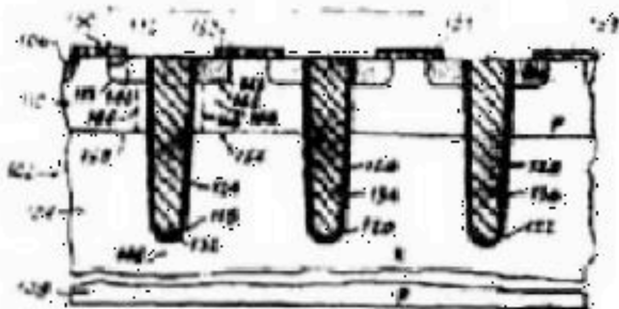
FIG_4f

'722 Patent

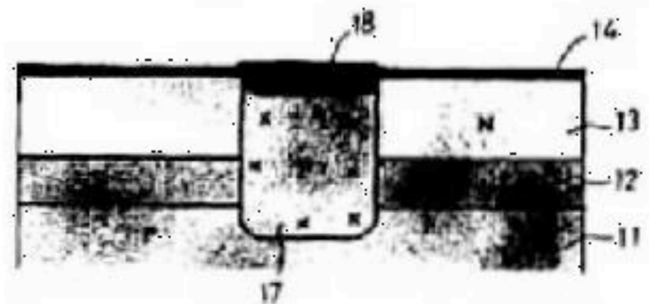


The prosecution history is also consistent with the '722 patent specification in describing surfaces with minimum deviation as "planar" surfaces. The Ogura Patent contains the only figure that depicts a flat surface that is described as having "a second dielectric region 24 having a planar top surface" (Eiseman Decl. Exh. B at 336). The other figures show a top surface with minor bumps that has been described by the applicant as a "planar" surface.

Ogura Patent ('785 Patent Prosecution History at Eiseman Decl. Exh. B at 335-36)



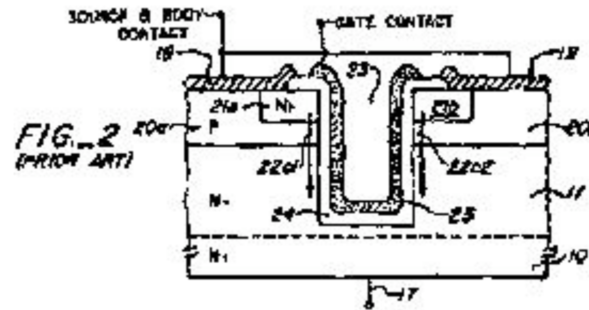
Schutten Patent Figure 13 ('722 Patent Prosecution History at Eiseman Decl. Exh. A at 80)



Kurahashi Patent ('785 Patent Prosecution History at Eiseman Decl. Exh. B at 258)

In contrast, the specification described Figure 2 as a "nonplanar" surface" in describing the U-shaped gate structure of the Ueda prior-art reference (Col. 1:47-55; 2:10-14). Unlike the other figures in the

specification or the aforementioned figures from the prosecution history, the U-shaped depression in Figure 2 clearly departs from any minor deviation of flatness. Thus, the specification and the prosecution history reveal a range of minor deviation from flatness that limit the range of planar surfaces.



AOS's construction of absolutely flat is rejected because it is not supported by the diagrams in the specification or the prosecution history. Figure 4f which is described as having a top surface forming an essentially flat (planar) surface is not truly flat. The prosecution history also characterizes figures in the prior art as "planar" when they are not absolutely flat (Eiseman Decl. Exh. A at 80 and Exh. B at 258, 276).

Siliconix' construction is also rejected. Under Siliconix' construction, "planar" would mean "essentially flat surface, meaning flat enough for any subsequent masking steps." *First,* this construction would render meaningless phrases in the specification and claims where "planar" has been further modified by some word of approximation. For example, the phrase "essentially flat (planar) surface" would mean "essentially essentially flat." In a similar vein, Claim 1 of the '785 patent contains a phrase "a second dielectric region having a *substantially planar* top surface" (Col.7:3-4) (emphasis added). This phrase would be rendered meaningless as substantially essentially flat surface (Col.7:4). This cannot be. Substantially planar then would equate to essentially planar.

Second, Siliconix' construction would cover the Ueda prior-art reference when its own specification has described as "nonplanar." Under Siliconix' proposed construction, a planar surface is flat enough for any subsequent masking step. A corollary, however, would be that a nonplanar surface would *not* be flat enough to allow any subsequent masking step. In the specification of the ' 722 patent, Figure 2 was described as the gate structure explained in the Ueda prior-art reference and that had a "nonplanar surface." Yet, Siliconix concedes that the Ueda reference described a subsequent masking step over the nonplanar surface. Siliconix now contends that its construction does not preclude subsequent masking steps for nonplanar surfaces. Rather, its construction supposedly suggests that subsequent masking steps are merely "easier" if there was a planar surface. The ordinary meaning of Siliconix' proposed construction does not in any way indicate facility or difficulty of the subsequent masking step. It simply states that planar means "essentially flat surface, meaning flat enough for any subsequent masking step." This construction would cover the Ueda prior-art reference that was specifically distinguished in the specification. Accordingly, it is not supported by the specification. Instead, planar equates to as flat as practicable.

2. "etching a plurality of grooves"

The parties dispute another phrase in Claim 10 of the '722 patent. The disputed phrase is "etching a plurality

of grooves so that each groove extends through an associated one of said regions within said plurality of semiconductor regions, through said second region and into said first region" (emphasis added):

10. A method for making a semiconductor device comprising the steps of:

providing a first region of semiconductor material of a first conductivity type;

forming a second region of semiconductor material of a second conductivity type of said first region;

forming a plurality of semiconductor regions of said first conductivity type within said second region;

etching a plurality of grooves so that each groove extends through an associated one of said regions within said plurality of semiconductor regions, through said second region and into said first region;

AOS contends that this method claim requires that the "steps" be undertaken in the sequential order as written. Thus, AOS construes the disputed phrase as "removal of semiconductor material such that two or more narrow channels are formed in the device, each narrow channel is formed deep enough to extend through *the two previously formed groups* of the sources and body regions and into the *previously provided* drain region" (Opp.27-28) (emphasis added). In contrast, Siliconix does not require the written order of sequence. Siliconix construes the phrase as "etching two or more grooves so that each groove extends through and is adjacent to at least one source region, and extends through the body region into the drain region."

This order construes the disputed phrase as etching two or more grooves so that each groove extends through the two previously formed regions of the source and body regions and into previously provided drain region. Although a specific sequence is not always required, in this case, the language and grammar of the Claim 10 requires that the steps occur in the order it was written. Loral Fairchild Corp. v. Sony Electronics Corp., 181 F.3d 1313, 1321-22 (Fed.Cir.1999) (holding that the language of the claim required performance of the steps in the order written); Interactive Gift Express, Inc. v. Compuserve Inc., 256 F.3d 1323, 1342-43 (Fed.Cir.2001) ("Unless the steps of a method actually recite an order, the steps are not ordinarily construed to require one. However, such a result can ensue when the method steps implicitly require that they be performed in the order written"). Claim 10 first requires "providing a first region." Then, it provides a step of "forming a second region ... *on said first region*." By literal language of the claim, the second region (jointly construed by parties as the body region) must form *on* the first region (jointly construed as drain region). Thus, formation of the body region had to be the second step in the process. Next, the language "forming a plurality of semiconductor regions ... *within said second region* " requires that the second region had been already formed before it could be segmented.

This sequence is not undermined by nor exclude an alternative embodiment described in the specification as Siliconix contends. The specification supports the sequential steps in Claim 10. For example, Siliconix references this provision in the specification (Col.2:24-31) (emphasis added):

An upward opening rectangular groove *extends downward through* the source and body regions and *into* the drain region so that a first source region *in* a first body region lies on one side of the rectangular groove and a second source region *in* a second body region lies on the other side of the rectangular groove.

This text clearly assumes the body regions were formed prior to the source regions as to allow the source

regions to lie *in* the body regions. It also presumes the existence of the source and body regions prior to the groove since the groove extends "through" the source and body regions. The specification supports the construction for etching the grooves as "etching two or more grooves so that each groove extends through the two previously formed regions of the source and body regions and into previously provided drain region."

Siliconix argues that since Claim 11 sets forth a sequential order and since it is dependent on Claim 10, Claim 10 cannot impose such an order under the doctrine of claim differentiation. This doctrine is applicable when the limitation in dispute is the *only* meaningful difference between the dependent and independent claims. *See* Wenger Mfg., Inc. v. Coating Mach. Sys., Inc., 239 F .3d 1225, 1233 (Fed.Cir.2001). This is not the situation here. Claim 11 provides an additional limitation requiring that the grooves "laterally surround said plurality of semiconductor regions of" drain, body and source regions (Col.8:61-63). With respect to the related '785 patent, Siliconix admitted that this phrase was the key in distinguishing between an open-cell MOSFET and a close-cell MOSFET. The same can be said as the key difference between Claims 10 and 11 of the parent '722 patent. Accordingly, both Claims 10 and 11 could require a specific order of sequence.

AOS seeks in addition the construction of the term "groove" as a "narrow channel." The parties, however, have jointly construed the drain, source, and body regions using also the word "channel" but this time to describe the electrical current flow that passes through the regions. For example, the drain region has been jointly construed as "the region that collects charge carriers flowing from the source through a *channel* during operation" (Joint Claim Construction Statement Exh. C). The use of the same word "channel" in two different phrases would unnecessarily confuse the jury. The term "groove" is sufficiently clear in its ordinary meaning such that it need not be further construed.

3. "substantially coplanar" in two of the disputed phrases

Three phrases from the '785 patent have been selected by the parties for claim construction. Two of the disputed phrases have practically the same language containing the term "substantially coplanar." One of them appears in Claim 14 (emphasis added):

an insulating layer formed over said gate structure, **said insulating layer being substantially coplanar with the top surface** of said third region.

The other disputed phrase appears in Claim 15 (emphasis added):

a second insulating layer formed over said gate structure, **said second insulating layer being substantially coplanar with a top surface of** said second plurality of semiconductor regions.

The parties have jointly construed the phrase "gate structure," "third region," and "second plurality of semiconductor regions." FN1 With respect to the remaining words, Siliconix contends that only the term "substantially coplanar" needs to be construed among the remaining terms for both of the disputed phrases. It construes "substantially coplanar" as "lying in largely the same plane."

FN1. The parties construed "gate structure" as a structure filling the groove to which voltage is applied to control the flow of charge carriers from the source region through the channel to the drain region during operation. "Third region" has been jointly construed as "the source region that supplied charge carriers that

may flow through a channel to the drain region during operation." "Second plurality of semiconductor regions" has been construed as two or more source regions that supply charge carriers that may flow through channels to the drain region during operation.

In contrast, AOS seeks to construe the entire phrase. It construes both of the disputed phrases to mean "the non-conductive, insulating material thermally grown over or above the gate structure results in the insulating material forming a planar or essentially flat top surface with the top surface of the insulating material over the source region." It appears from this proposed construction that AOS construes "substantially coplanar" as "forming a planar or essentially flat top surface." Yet, AOS proposes specifically that "substantially coplanar" should be construed as "a geometry where two or more flat two-dimensional surfaces form an essentially flat plane. Parallel surfaces are not coplanar." This expanded definition does not appear in AOS' proposed construction of the disputed phrase.

In comparing the parties' proposed construction of the disputed phrases, the parties' dispute revolves around two terms contained in the disputed phrases: "substantially coplanar" and "formed over." All other words in the two disputed phrases need not be construed as the parties apparently agree and their ordinary meaning is evident to the jury. *See* U.S. Surgical Corp. v. Ethicon, 103 F.3d 1554, 1568 (Fed.Cir.1997). Put differently, the ordinary meaning of the following terms are evident: "insulating layer," "second insulating layer," "being," and "top surface."

This order holds that the disputed term "substantially coplanar" means lying largely in the same plane. This disputed term should be given its ordinary meaning. Texas Digital Sys., Inc. v. Telegenix, Inc., 308 F.3d 1193, 1202-04 (Fed.Cir.2002), *cert. denied,* 123 S.Ct. 2230 (2003). Coplanar is defined as lying or acting in the same plane (Merriam-Webster' Ninth College Dictionary 1984). The Federal Circuit has already considered the term "substantially" and has defined it as "largely but not wholly that which is specified." LNP Eng'g Plastics, Inc. v. Miller Waste Mills, Inc., 275 F.3d 1347, 1354 (Fed.Cir.2001); *see also* Liquid Dynamics Corp. v. Vaughan Co., 355 F.3d 1361, 1368 (Fed.Cir.2004) ("words of approximation, such as 'generally' and 'substantially' are not descriptive terms commonly used in patent claims 'to avoid a strict numerical boundary to the specified parameter"). Thus, the combination of these definitions provides for the ordinary meaning of lying largely in the same plane.

This construction comports with the usage of the term in Claim 14 and 15. Nothing in the specification or prosecution history warrants a different construction. No relevant technical dictionaries define the term.

AOS contends that the specification requires a two-dimensional flat level based on their construction of the term "planar." AOS, therefore, suggests that "parallel surfaces are not coplanar." This construction, however, eliminates the word "substantially" from the claims. Both Claims 14 and 15 require the insulating layer to be "substantially coplanar" with the top surface of the source region. As discussed above, the specification does not require absolute flatness of the surface. The diagrams in the specification show that the top surface is not absolutely flat with surface of the source region. Thus, the term "substantially coplanar" does not require the two different regions to be on the exact same plane as to create a geometrically contiguous flat surface.

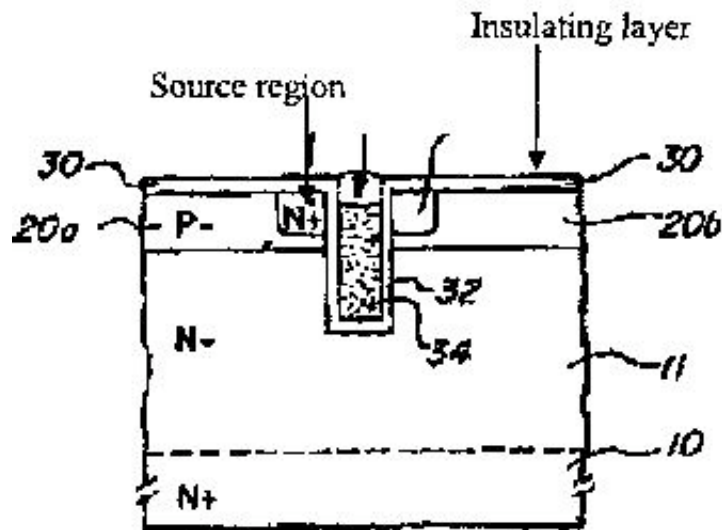


Figure 4f (slightly modified)

This order holds that the term "formed over" need not be construed. Its plain meaning is clear to the jury. U.S. Surgical Corp. v. Ethicon, 103 F.3d 1554, 1568 (Fed.Cir.1997).

AOS attempts to limit the term "formed over" to the preferred embodiment disclosed in the specification by construing the phrase as " *thermally grown* over or above the gate structure *resulting in* the insulating material forming a planar or essentially flat top surface with the top surface of the insulating material over the source region" (Opp.8, 12) (emphasis added). The specification describes multiple embodiments and, thus, the claims should not be limited to the preferred embodiment. The Federal Circuit has forbidden such importation. *See* Storage Tech. Corp. v. Cisco Sys., Inc., 329 F.3d 823, 831 (Fed.Cir.2003). Moreover, the claim at issue is from the '785 device patent and not the '722 method patent. One embodiment of creating the insulating layer pertinent to the method patent does not necessarily limit the device patent. Nothing in the prosecution history indicates clear disavowal of all other ways the insulating layer could be formed for the patent. Acco Brands, Inc. v. Micro Sec. Devices, Inc., 346 F.3d 1075, 3078 (Fed.Cir.2003). Finally, if such limitation was imported into the independent Claims 14 and 15, then dependent Claim 18 would be rendered meaningless as it requires the insulating layer to be thermally grown. The only distinguishing phrase in Claim 18 is the limitation of thermally-grown insulating layer (Col.10:7-9). Under doctrine of claim differentiation, these different claims must be given different meanings. *See* Clearstream Wasterwater Sys., Inc. v. Hydro-Action, Inc., 206 F.3d 1440, 1446 (Fed.Cir.2000).

Accordingly, this order holds that "an insulating layer formed over said gate structure, said insulating layer being substantially coplanar with the top surface of said third region" means an insulating layer formed over said gate structure, said insulating layer lying largely on the same plane with the top surface of the source region. Similarly, "a second insulating layer formed over said gate structure, said second insulating layer being substantially coplanar with a top surface of said second plurality of semiconductor regions" is construed as a second insulating layer formed over said gate structure, said second insulating layer lying largely on the same plane with the top surface of the source regions.

4. "groove laterally surrounding said first and second plurality of semiconductor regions"

The phrase "groove laterally surrounding said first and second plurality of semiconductor regions" exists in Claim 15 of the '785 patent (emphasis added):

15. A vertical MOS transistor comprising: a first region of semiconductor material of a first conductivity type;

a first plurality of semiconductor regions of a second conductivity type opposite said first conductivity type formed on said first region;

a second plurality of semiconductor regions of said first conductivity type, each region within said second plurality being formed on an associated region within said first plurality, each region with said second plurality and its associated region within said first plurality being separated from the other regions within said first and second pluralities by a groove, **said groove laterally surrounding said first and second plurality of semiconductor regions**

Siliconix construes the disputed phrase as "when viewed from above the major surface of the semiconductor device, the groove surrounds the source and body regions." AOS construes it as "a narrow channel or trench formed in the device, which encloses the source and body regions on at least two sides."

This order holds that "said groove laterally surrounding said first and second plurality of semiconductor regions" means when viewed from above the major surface of the semiconductor device, the groove encloses the source and body regions on all sides. The parties jointly construed the "first and second plurality of semiconductor regions" to mean the body and source regions, respectively. The specification does not define the terms "laterally" or "surround." Thus, the ordinary meaning will be adopted.

The ordinary meaning of the term "lateral" means coming from the side (Merriam-Webster' Ninth College Dictionary 1984). The ordinary meaning of the term "surround" requires enclosure on all sides (ibid.). Thus, the groove has to be all around the side of the source and body regions.

In contrast, AOS's construction goes against the ordinary meaning. The term "surround" cannot be limited to two sides. Nothing in the specification indicates that the patentee was its own lexicographer and gave a definition different from the ordinary meaning for the term "surround."

This specification confirms that the groove encloses the source and body regions on all sides. Figure 9 shows a top view of one embodiment of the invention. It shows a square source and body regions that are arranged in a "square gate grid" (Col.5:2-5). The source and body regions are surrounded on all sides by the groove. The prosecution history provides that "Claim 11 is supported, *inter alia,* by Figure 9" (Eiseman Decl. Exh. B at 406).

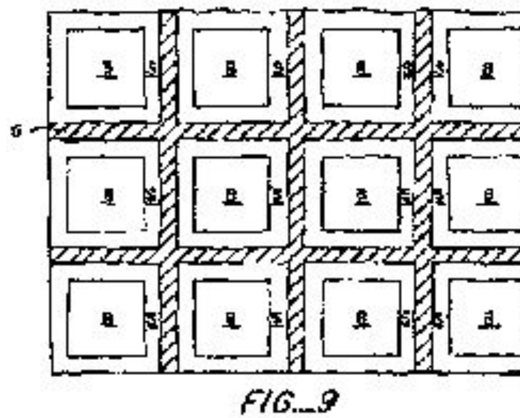


FIG._9

AOS contends that Siliconix' proposed construction would somehow obviate the term "a plurality of grooves" in Claim 10 of '722 patent. AOS' argument rests on its belief that Figure 9 could only exist where there is a plurality of grooves. This is incorrect. As shown in Figure 9, there can be a single, continuous groove. By contrast, a plurality of grooves is necessary for the interdigitated layout disclosed in the specification

5. "means for electrically contacting the top surface of said third region"

The phrase "means for electrically contacting the top surface of said third region" appears in Claim 14 of the '785 patent (emphasis added):

14. A vertical MOS transistor comprising a plurality of cells, each cell comprising:

a first region of semiconductor material of a first conductivity type;

a second region of semiconductor material of a second conductivity type formed on said first region;

a third region of said first conductivity type formed on said second region

* * *

an insulating layer formed over said gate structure, said insulating layer being substantially coplanar with the top surface of said third region;

means for electrically contacting the top surface of said third region; and

means for electrically contacting the bottom surface of said first region

Siliconix construes the phrase as "a layer of conductive material (such as a metal) that electrically connects to the top surface of the source region that permits electric current to flow to or from the source region, or equivalent thereof." AOS construes the phrase as "one or more contacts that connect to the top surface of the source region and permits electrical current to flow to or from the source region, or equivalents thereof."

This is a means-plus-function claim phrase which must be "construed to cover the corresponding structure, material, or acts described in the specification and equivalents thereof." 35 U.S.C. 112(6). In construing a

means-plus-function claim phrase, the recited function within that limitation must be first identified. ACTV, Inc. v. Walt Disney Co., 346 F.3d 1082, 1087 (Fed.Cir.2003). Then, the written description must be examined to determine the structure that corresponds to and perform that function. *Ibid.*

This order construes the means-plus-function phrase as one or more contacts that electrically connects to the top surface of the source region as to permit electric current to flow to or from the source region, or equivalent thereof. The parties agree that the claimed function is a means for electrically contacting the top surface of the source region. The specification of the '758 patent provides in pertinent part (Col.1:31-34, 1:69-2:3, 4:57-60).

Source regions 13a and 13b are electrically tied to body regions 12a and 12b by metal contacts 18 and 19 [referring to FIG. 1]

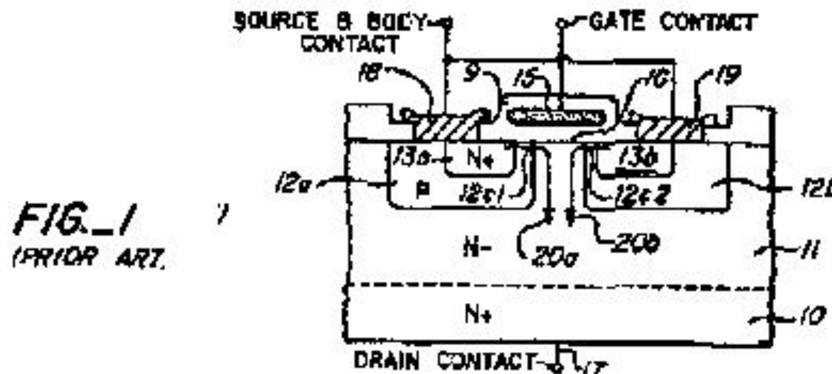
* * *

Source regions

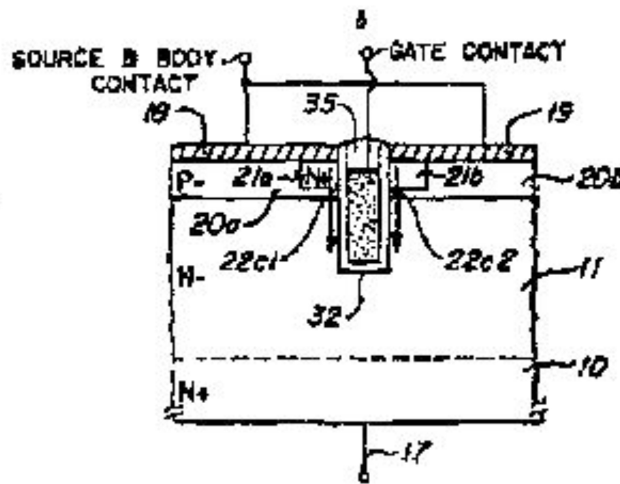
1a and 21b are electrically tied to body regions 21a and 20b, respectively, by metal contacts 18 and 19 which are also electrically tied together. [referring to FIG. 2]

* * *

The source/body contact shown schematically in FIG. 3 is fabricated using prior art techniques, and in cross section typically appear as shown in FIG. 1.



Figures 1-3 depict one or more contact points that is connected to the source region. The cross-section view of Figure 3 is described as typically shown as in Figure 1 where metal contacts were depicted as 18 and 19. Thus, 18 and 19 are presumably showing also metal contacts in Figure 3. Figure 3 depicts two metal contacts of forward-hatched area towards on top of the source and body regions.



Siliconix proposes that there is a metal layer overlying the gate structure. Nothing in the specification teaches a metal layer over the gate structure. Figure 3 is the closest to any layer of metal contact. Still, Figure 3 shows a disjunction between the two contact points; there is no metal layer over the gate structure. Nor does Figure 7 show a metal layer. Instead, layer 30 is described in the specification as a silicon dioxide layer (Col.3:63). The Court cannot change the specification at this time "to correct" any mistakes. Novo Indus. L.P. v. Micro Molds Corp., 350 F.3d 1348, 1354 (Fed.Cir.2003).

Siliconix contends that the specification incorporates prior-art techniques which include a unified metal layer over the gate structure. The specification, however, provides that: "[t]he source/body contact shown schematically in FIG. 3 is fabricated using prior art techniques, *and in cross section typically appears as shown in FIG. 1* " (Col.4:57-59). Figure 1 does not show a metal layer over the gate structure. The prosecution history cannot be used to expand the scope of a means-plus function claim, which can only be construed to cover structures described in the specification. 35 U.S.C. 112 para. 6.

CONCLUSION

The foregoing claim-construction ruling shall govern all subsequent proceedings herein.

IT IS SO ORDERED.

N.D.Cal.,2004.
Siliconix Inc. v. Alpha and Omega Semiconductor Inc.

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