United States District Court,
E.D. Texas, Marshall Division.

INTERGRAPH HARDWARE TECHNOLOGIES COMPANY,
v.
HEWLETT-PACKARD COMPANY.

Civil Action No. 2:02-CV-312

July 1, 2004.

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MEMORANDUM OPINION AND ORDER

T. JOHN WARD**, District Judge.**

1. Introduction.

The court issues this memorandum opinion and order to construe the claims of the three patents in suit. The three patents, U.S. Patent No. 5,091,846 ("'846 Patent"), U.S. Patent No. 4,933,835 ("2C835 Patent"), and U.S. Patent No. 4,899,275 ("'275 Patent) are related generally to cache memory management in computing systems. The court has considered the parties' briefs and arguments, the applicable law, and the intrinsic record and is persuaded, for the reasons assigned below, to construe the terms at issue as set forth in this opinion.

2. Legal Principles Applicable to Claim Construction.

"A claim in a patent provides the metes and bounds of the right which the patent confers on the patentee to exclude others from making, using or selling the protected invention." Burke, Inc. v. Bruno Indep. Living Aids, Inc., 183 F.3d 1334, 1340 (Fed.Cir.1999). Claim construction is an issue of law for the court to decide. Markman v. Westview Instruments, Inc., 52 F.3d 967, 970-71 (Fed.Cir.1995) (en banc), *aff'd,* 517 U.S. 370, 116 S.Ct. 1384, 134 L.Ed.2d 577 (1996).

To ascertain the meaning of claims, the court looks to three primary sources: the claims, the specification, and the prosecution history. Markman, 52 F.3d at 979. Under the patent law, the specification must contain a written description of the invention that enables one of ordinary skill in the art to make and use the invention. A patent's claims must be read in view of the specification, of which they are a part. Markman, 52 F.3d at 979. For claim construction purposes, the description may act as a sort of dictionary, which explains the invention and may define terms used in the claims. *Id.* "One purpose for examining the specification is to determine if the patentee has limited the scope of the claims." Watts v. XL Sys., Inc., 232 F.3d 877, 882 (Fed.Cir.2000).

Nonetheless, it is the function of the claims, not the specifications, to set forth the limits of the patentee's claims. Otherwise, there would be no need for claims. SRI Int'l, v. Matsushita Elec. Corp., 775 F.2d 1107, 1121 (Fed.Cir.1985) (en banc). The patentee is free to be his own lexicographer, but any special definition given to a word must be clearly set forth in the specification. Intellicall, Inc. v. Phonometrics, 952 F.2d 1384, 1388 (Fed.Cir.1992). And, although the specifications may indicate that certain embodiments are preferred, particular embodiments appearing in the specification will not be read into the claims when the claim language is broader than the embodiments. Electro Med. Sys., S.A. v. Cooper Life Sciences, Inc., 34 F.3d 1048, 1054 (Fed.Cir.1994).

To assess the ordinary meaning of terms used in a patent claim, a court may properly rely on dictionary definitions. The Federal Circuit has noted that "[i]t has long been recognized in the precedent of our predecessor court, the Court of Customs and Patent Appeals, that dictionaries, encyclopedias and treatises are particularly useful resources to assist the court in determining the ordinary and customary meaning of claim terms." Texas Digital Systems, Inc. v. Telegenix, Inc., 308 F.3d 1193, 1202 (Fed.Cir.2002). The court reasoned that such sources are objective resources that serve as reliable sources of information on the established meanings that would have been attributed to the terms of the claims by those of skill in the art. Id. at 1202-03. According to the court, dictionaries, encyclopedias and treatises "constitute unbiased reflections of common understanding not influenced by expert testimony or events subsequent to the fixing of the intrinsic record by the grant of the patent, not colored by the motives of the parties, and not inspired by litigation." Id. at 1203.

Several of the claim terms at issue in this case are conceded by all parties to be drafted in means-plus-function format; therefore, a discussion of the rules pertaining to such terms is appropriate. Title 35, section 112, paragraph 6 of the United States Code provides:

An element in a claim for a combination may be expressed as a means or step for performing a specified function without the recital of structure, material, or acts in support thereof, and such claim shall be construed to cover the corresponding structure, material, or acts described in the specification and equivalents thereof.

35 U.S.C. s. 112 para. 6.

Claim elements drafted under this statutory section are commonly referred to as means-plus-function or step-plus-function limitations. Through use of means-plus-function limitations, patent applicants are allowed to claim an element of a combination functionally, without reciting structures for performing those functions. Envirco Corp. v. Clestra Cleanroom, Inc., 209 F.3d 1360, 1364 (Fed.Cir.2000), The trade-off, however, for the use of this technique, is that the applicant is limited to the structure disclosed in the

specification and equivalents. The statute specifically provides its own rule of claim construction when it states that "such claim shall be construed to cover the corresponding structure, material, or acts described in the specification and equivalents thereof." 35 U.S.C. s. 1121 para. 6.

Once it is determined that a particular limitation is drafted in means-plus-function form, claim construction of the element is a two-step process. First, the court must identify the claimed function. *Telemac Cellular Corp. v. Topp Telecom, Inc.,* 247 F.3d 1314, 1324 (Fed.Cir.2001). The court must construe the function to include only the limitations contained in the claim language. Lockheed Martin Corp. v. Space Sys/Loral, Inc., 249 F.3d 1314, 1324 (Fed.Cir.2001). General principles of claim construction govern the interpretation of claim language used to describe the function.

After the court identifies the claimed function, the court must then determine what structure, if any, disclosed in the specification corresponds to the claimed function. *Id.* To qualify as corresponding structure, the structure must not only perform the claimed function, but the specification must clearly associate or "link" the structure with the performance of the function. Medtronic, Inc. v. Advanced Cardiovascular Systems, Inc. ., 248 F.3d 1303, 1311 (Fed.Cir.2001). The court undertakes this task from the perspective of a person of ordinary skill in the art. Amtel Corp. v. Info. Storage Devices, Inc., 198 F.3d 1374, 1378-79 (Fed.Cir.1999). The determination of what constitutes corresponding structure can be difficult. Corresponding structure, it must be remembered, need not include all things necessary to enable the claimed invention to work. But corresponding structure must, however, include all structure that actually performs the recited function. Asyst Techs., Inc. v. Empak, Inc., 268 F.3d 1364, 1371 (Fed.Cir.2001). Bearing these standards in mind, the court will construe the relevant terms in the three patents in suit.

3. Discussion.

A. Agreed Terms

The parties have agreed to constructions of certain terms. Those terms, and the parties' agreed constructions, are set forth below.

1. "Comprising"

Comprising means "including the following but not excluding others."

2. "Bus"

Bus means "one or more conductors in a computer along which information is transmitted from any of a plurality of sources to any of a plurality of destinations."

3. "System Bus"

System bus means "a bus to which the first data processing element, the cache memory management means, and the primary memory, as well as potentially numerous other system elements including multiple I/O processors, can be coupled."

4. "I/O Requests"

I/O requests means "reads and writes from, or on behalf of, I/O devices."

5. "Signal"

Signal means "a variation of a physical quantity, used to convey data."

B. Disputed Terms

The parties dispute the construction of several terms. Those terms, and the court's construction of those terms, are set forth below. In general, the court has addressed the terms in the order in which the parties addressed them at the claim construction hearing. The court has also construed those terms addressed in the parties' briefing but not in oral argument, to the extent the court has determined that construction of those terms is necessary.

1. "Primary memory means"

The term "primary memory means" as used in claim 1 of the '835 patent is drafted pursuant to 35 U.S.C. s. 112 para. 6, and it is not disputed that it is a means plus function limitation. The function recited in the claim is "storing data at storage locations therein." As is the case in many of the disputed terms, the parties sharply disagree over the extent to which certain structure disclosed in the patent is necessary to perform the claimed function.

The parties disagree on the corresponding structure because they disagree on whether the whether the word "storing" is used in the passive or active sense. The plaintiff suggests in its brief that the court should consider the context of the claim in which the term is used before determining whether the patentee invoked the passive or active sense of the word. The plaintiff argues that when the court is considering the term in the context of a memory related device which is intended to retain data, the court should construe the claim term in the passive sense. The plaintiff points out, however, that the term "storing" is sometimes used in other claims in connection with control devices. These devices are used to control writing to and reading from a memory device. In those claims, the plaintiff suggests that the term should be construed in the active sense of transferring data to storage.

The defendant disagrees. The defendant argues that in certain claims, the patentee clearly used the term "storing" in its active sense. According to the defendant, this usage requires the court to interpret the term throughout all claims in its active sense. *See* Claim Construction Hearing Transcript, at 94-95. Because the active sense of storing includes the activity of transferring data to a storage location for later extraction and use, the defendant urges the court to include as corresponding structure the structure necessary to effect a transfer of data-here the drivers, receivers and interfaces disclosed in the patent specification.

Although it is a close question, the court agrees with the plaintiff. In the context of these claims and in the light of the patent disclosures, the patentee used the term in two different ways-both actively and passively. The "primary memory means" limitation of claim 1 of the '835 patent is used in the context of a storage device; therefore, the court therefore construes the term "storing" to be used in the passive sense (i.e. to retain). The court is mindful of the general rules governing claim construction and in particular the rule requiring claim terms to be construed consistently throughout the claims. Southwall Technologies, Inc. v. Cardinal IG Company, 54 F.3d 1570 (Fed.Cir.1995). Nevertheless, that rule is not as absolute as the defendant suggests, especially where, as here, the claims read in light of the specification reveal that the applicant used the same word in both its passive and active sense. Cornell University v. Hewlett-Packard Co., 2004 WL 737071 (N.D.N.Y. March 26, 2004) (construing the term "dispatch stack" multiple ways

depending on the claim context in which patentee used the words); Angelo Mongiello's Children, LLC v. Pizza Hut, Inc., 70 F.Supp.2d 196, 205 (E.D.N.Y.1995) (observing that claim terms must be interpreted consistently "unless there is a clear indication to the contrary.").

The specification identifies main memory 140 as containing the primary memory storage for the system, which may be comprised of a read-write memory (e.g. DRAM or SRAM). *See* '835 Patent, Col. 3, ll. 49-52; col. 14, 1. 49: "primary main memory 140;" and 1.62: "primary memory 140." The specification further specifies the main memory 140 as including the additional structure of a read-write memory array error correction and drivers-receivers and bus interface circuitry. The function of the additional structure is bus coupling and interface protocol handling for transfers between the main memory and the system bus. *See* '835 Patent, Col. 14, ll.18-26. The specification does not clearly link the additional structure to the specified function of "storing data at storage locations therein."

The court has also considered, but ultimately rejects, the plaintiff's suggestion that the corresponding memory structure should be limited to the DRAM/SRAM structure within the memory 140. The "at storage locations therein" recitation of the claim language identifies structure within the primary memory means where data is retained, which is illustrated as Dynamic Memory (DRAM or SRAM). As such, the corresponding structure is main memory 140 and its read-write memory array. Given the court's construction that the term "storing" is used in the passive tense, and because the specification links the error correction, drivers/receivers, and interface structures to other functions, the court necessarily rejects the defendants' argument that the corresponding structure to the primary memory means must include the Drivers/Rcvers and Interface and DRAMC ECC components of the main memory 140.

2. "Pages of data"

The court construes the term "pages of data" to mean "fixed size blocks of data." The court rejects the plaintiff's proposed construction because it includes an additional requirement of "fixed alignment." The court is persuaded that one of ordinary skill in the art would understand the term to connote the meaning ascribed to the term by the court.

3. "Virtual address"

The court now considers the term "virtual address." The parties' dispute over this term primarily involves the incorporation of the word "application" as used in the defendants' definition. According to the plaintiff, these patents disclose *hardware* inventions. The plaintiff's argument is that because the patents are hardware patents, use of a definition that includes "application" improperly incorporates a software limitation into the claims. The defendant, for its part, points to several dictionary definitions of the term "virtual address" which suggest that the term itself implies a software limitation. After considering the parties' positions, the court construes the term "virtual address" to mean "a memory address provided by the CPU in executing an application software program and that is translated into a real memory address by hardware." *See* '846 Patent, Col. 6 11. 50-53.

4. "Cache memory"

The court defines the term "cache memory" to mean "a high speed memory that bridges main memory and the CPU." The court rejects the plaintiff's argument that no definition of this term is required and, at the same time, rejects the defendant's argument that the patentee expressly limited the scope of this term in an exchange with the examiner. In the pertinent correspondence, the patentee remarked that the cache memory

was by definition, "a memory having a higher speed than the local memory and which is disposed between the local memory and the processor." This statement must be read in the context in which it was made. The applicant was distinguishing the Kaplinsky reference from the present invention, and the court is not persuaded that this statement has the effect of incorporating a concept of "local memory" into the claims of these patents.

5. "Cache memory means"

Claim 1 of the '835 patent recites a "cache memory means" term. This term is drafted according to s. 112 para. 6. The claimed function is "storing data from main memory." Again, the parties dispute whether "storing" is used in the passive or active sense and this dispute affects the parties' positions on the appropriate corresponding structure. The court concludes that "storing data" in the context of this claim is used in the passive sense and means "retaining" data. The cache memory 320 is the corresponding structure. '835 Patent, Col. 14, ll. 42-46; col. 19, ll. 34-36, ll. 40-42, ll. 65-66; col. 20, ll. 38-42; Figs. 9 and 10A.

6. "Processing data"

The term "processing data" means the execution of a systematic sequence of mathematical and/or logical operations.

7. "System bus means"

This term is drafted according to s. 112 para. 6. The claimed function is "communicating data with the primary memory means." The court agrees with the plaintiff that the claimed function is communicating *data;* therefore, the court has limited the corresponding structure which is linked to the function of data communication. The structure identified by defendants transmits other information that facilitates communication among the system components; however, given that the only function recited by the claim is that for communicating data, the corresponding structure is the AD<31:0>: address/databus. '835 Patent, Col. 10, ll. 7-13, Fig. 5.

8. "Coupled"

The court defines the term "coupled" to mean "electrically connected, directly or indirectly."

9. "Cache data storage mode"

This term is used in claims 1 and 9 of the '846 patent. The plaintiff urges the court to construe the claim term to mean "caching strategies defining whether, in response to a CPU read operation, the cache controller initiates copying data to its cache memory, and whether, in response to a CPU store operation, the cache controller initiates writing data to its cache memory and/or primary memory." The defendants argue that the court should construe the claim term to mean "different ways of performing or operating with respect to data stored in the cache." A careful review of the patent reveals that the defendants' proposed construction actually excludes a third data storage mode disclosed in the patent. As such, the defendants' construction would be rarely correct under general rules governing claim construction. The patents describe three storage modes: write through, copyback, and cache/non-cache. The third mode, absent from the defendants' proposed definition, describes the concept of operations on data *not stored* in the cache. Given the disclosure of the patents of the third mode, the court defines "cache data storage mode" to mean "strategies for writing data to cache and to primary memory."

10. "Immediately stores said modified data in said primary memory"

This term is part of the recitation in claim 4 of the '846 patent of the write-through data storage mode, which the patentee defines in the specification as a simultaneous write operation to cache memory and main memory. See '846 Patent, Col. 30, ll. 37-42. The court defines the term "immediately stores said modified data in said primary memory" to mean "the CPU executes a write operation to main memory simultaneously with the writing of data to the cache memory."

11. "System tag means"

This term is drafted according to s. 112 para. 6 and is used in claims 1 and 9 of the '846 patent. The claimed function is "storing a system tag which identifies one of a plurality of cache data storage modes." Again, in the context of this claim, the term "storing" is used in the passive sense. The corresponding structure is the memory 350 in the Translation Lookaside Buffer ("TLB") 270 that stores a system tag ST field of control bits. See '846 Patent, Col. 22, ll. 29-31; col. 23 ll. 40-46; Figs. 9, 11A and 11B.

12. "Cache mode effecting means"

This term is drafted according to s. 112 para. 6. The claimed function is "effecting the cache data storage mode indicated by the system tag." The corresponding structure is the microengine 650 programmed and configured to perform the disclosed state transitions of the copyback, write-through or cache/non-cache modes as specifically illustrated in Figure 18 of the '846 Patent. Figure 18 shows a state diagram defining the state-to-state transitions of the computer system. The microengine 650 is a microprogrammed controller that executes instructions from ROM 700 (Fig.22) to provide control signals that implement the cache data storage mode state transitions shown in Figure 18. *See* Col. 36, ll. 33-36; WMS Gaming, Inc. v. International Game Technology, 184 F.3d 1339, 1348 (Fed.Cir.1999) ("The structure of a microprocessor programmed to carry out an algorithm is limited by the disclosed algorithm. A general purpose computer, or microprocessor, programmed to carry out an algorithm creates a new machine, because a general purpose computer in effect becomes a special purpose computer once it is programmed to perform particular functions pursuant to instructions from program software.") (intemal quotation omitted).

13. "Data consistency means"

The data consistency means term is drafted according to s. 112 para. 6. The claimed function is "ensuring shared data consistency between the first and second data processing elements." The patent specification discusses a multiple processor embodiment and notes the problem of data consistency in the description at column 13, lines 6-20. As described there, the system bus is monitored and for certain types of bus transactions an internal cache cycle is performed. Control of the cache MMU is provided by microengine 650. See Fig. 20; Col. 33, ll. 27-28 and 31-32; Fig 23, Col. 36, ll. 54-58. As shown, microengine 650 is coupled to System Bus Control 840, which includes Bus Watch Detector 1250. *See* Figs. 23 and 27.

The corresponding structure includes system bus control 840 and microengine 650 programmed to execute a set of instructions to perform an internal cycle to determine whether to purge the cache of its data and supply data from an addressed location or to supply its data instead of supplying data from an addressed location.

The court has carefully reviewed the defendants' argument that the corresponding structure must prohibit

shared data from being designated as copyback. While it is true that copy-back mode does not assure data consistency between main memory and cache memory, the specification does not link a prohibition of the copyback mode with overcoming the problem of data consistency in a multiple processor embodiment. All that is linked to the function of "ensuring data consistency between the first and second data processing elements" is performance of the described internal cycle upon occurrence of a bus transaction that could affect the consistency of data in the system. The court ultimately concludes that the additional structure sought to be included is in some instances linked to functions other than that of "ensuring shared data consistency between the first and second data processing elements" and in other instances more appropriately characterized as enabling structure that is not necessary to perform the function of "ensuring data consistency."

14. "System bus monitoring means"

This claim term is drafted according to s. 112 para. 6. The claimed function is "monitoring I/O requests over the system bus." Again, the parties disagree on the corresponding structure. The defendants assert that certain structure should be included to enable the invention to distinguish I/O requests from other types of transactions. The defendants argue, therefore, that certain "filtering" structure is required. The court disagrees. It bears emphasis, in light of the parties' arguments over corresponding structure, that the function claimed is one of *monitoring*. The bus watch detector 1250 is the structure linked to this function.

15. "Primary memory access detecting means"

This term is drafted in means-plus-function format. The claimed function is "detecting when the primary memory means is being accessed by the first data processing element." Here, the court holds that the corresponding structure is the bus watch detector 1250 and control register 1260. The plaintiff admits that "detecting" involves identifying a circumstance or occurrence. *See* Intergraph's Opening Claim Construction Brief at 41. The register 1260 is necessary structure for performing the function of "detecting" which must necessarily include an identification of a particular type of bus transaction, i.e., the memory means is being accessed by the first data processing element.

16. "Translation means"

This claim term is also drafted according to s. 112 para. 6. The claimed function is "providing an associative map of translations of virtual addresses to real addresses corresponding to data stored in said primary memory." The corresponding structure is Array 352/354 of TLB 350 (Fig.9).

17. "Cache interface means"

The term "cache interface means" is drafted according to s. 112 para. 6. The claimed function is "selectively coupling data between said processor and said cache memory." The corresponding structure disclosed in the patent is the CPU interface registers, 210, 230 and 240. *See* '846 Patent, Col. 19 ll. 57-59 ("The CPU interface is comprised of an address input register 210, a cache output register 230, and a cache input register 240.").

18. "Cache controller means"

This term is drafted according to s. 112 para. 6. The language sets forth two functions: (1) selectively communicating data between primary memory and cache memory and (2) communicating data between

cache memory and second data processing element.

As to the first function, the specification describes that microengine 650 coordinates system bus transfers after a cache miss. *See* '835 Patent, Col. 32, ll. 65-68. If there is a cache miss, the real address is sent over the system bus to main memory and data is returned to the cache. *See* '835 Patent, Col. 20, ll. 20-25; col. 32, ll. 26-32. The corresponding structure linked to the first function is system interface 640 (Fig.21) and micro engine 650 programmed to execute instructions to provide control signals that implement bus transfer of the real address to main memory and the return of data to the cache.

As to the second function, the specification describes that data is exchanged between the cache and the CPU. This is illustrated, for example, in the state diagram of Figure 18. As shown in Figure 20, the cache is coupled to the processor by CPU Interface 600. *See* '835 Patent, Col. 32, 11. 37-39. Control of transfers between the cache and the CPU is provided by CPU interface and control circuit (CPCTL) 810 and microengine 650. *See* '835 Patent, Col. 35, ll. 64-68. The corresponding structure linked to the second function is CPU Interface 600, CPU interface and control circuit (CPCTL) 810, and microengine 650 programmed to implement the state transitions shown in Figure 18 for data exchange between the cache and the CPU.

19. "Cache inquiry means"

This term is drafted according to s. 112 para. 6. The claimed function in the ' 835 Patent is "determining whether a storage location being accessed in the primary memory means corresponds to data stored in the cache memory means." The '835 Patent describes that a virtual address is applied to the cache memory buffer 320 selection logic to select a line therein and is also applied to the TLB 350 to access array 352/354, which outputs the real address of the primary memory page corresponding to the virtual address presented. The real address is gated out to comparators 332/334 for comparison to the cache real address tag outputs 322/326. The comparators compare the real address from the TLB with the real address tags 322/326 from the cache data buffer. *See* '835 Patent, Col. 19, ll. 34-57. If there is a match, then the appropriate word is gated out to Cache Output Register COR 230. *See* '835 Patent, Col. 20, ll.4-8. Against this backdrop, the structure necessary to perform the function of determining whether a storage location being accessed in the primary memory means corresponds to data stored in the cache memory means is TLB 350 and comparators 332/334 shown in Figure 9.

20. "Primary memory interface means"

The court construes this means-plus-function limitation to specify the function of coupling data between said primary memory and said cache memory. According to the '846 patent, "[t]he system bus interface is comprised of a system bus input register 260 and a system bus output register 250." *See* ' 846 Patent, Col. 19, ll. 59-61. The corresponding structure is, therefore, SIR 260 and SOR 250 as disclosed in Figure 8 and SIR 643 and SOR 644 as disclosed in Figure 21.

21. "Access indicating means"

The court construes this s. 112 para. 6 limitation to claim the function of "indicating when the primary memory is being accessed." The corresponding structure in the '835 patent is MS<4> lines on the system bus and the AC line. *See* '835 Patent, Col. 10, ll. 34-36; col. 11, ll. 15-17.

22. "Access control means"

This claim term is drafted according to s. 112 para. 6. The claimed function is "selectively allowing and inhibiting access to the primary memory." The corresponding structure is the primary memory drivers/receivers and interface coupled to the system bus 141. *See* '835 Patent, Fig. 1; col. 14, ll. 18-23 ("which provide for bus coupling and interface protocol handling for transfers between the main memory 140 and the system bus 141").

23. "Inquiry indicating means"

This term is drafted in means-plus-function format. The claimed function is "providing a first cache inquiry signal to the system bus means." The corresponding structure is the Bus Watch Detector 1250 (Fig.27) issuing the Cache Busy ("CBSY") signal.

24. "Read indicating means"

This term is drafted in means-plus-function format. The function is "providing a read indicating signal." The corresponding structure is the bus line conveying CT<2> Cycle Type control bit. *See* '835 Patent, Col. 10, ll. 15-17.

25. "Write indicating means"

This term is drafted in means-plus-function format. The function is "providing a write indicating signal." The corresponding structure is the bus line conveying CT<2> Cycle Type control bit.

26. "Cache memory management means"

With respect to the term "cache memory management means," as used in claim l [e] of the '846 patent, the parties dispute whether the limitation is drafted according to s. 112 para. 6. The claim language certainly uses the word "means" and therefore, under well-settled Federal Circuit precedent, invokes a presumption that s. 112 para. 6 applies. The court notes, however, that there is no recitation of function following the word "for." Instead, the claim language proceeds to recite various structure that comprises the "cache memory management means." Inparticular, the language of the claim recites a cache memory and cache controller, which effectively takes the limitation out of the scope of s. 11216. TurboCare Division of Demag Delval Turbomachinery Corp. v. General Electric Co., 264 F.3d 1111 (Fed.Cir.2001). Given that the language of the claim itself recites sufficient structure, the court finds that the presumption of 112 para. 6 drafting is overcome. The court's conclusion in this regard requires the court also to reject the defendant's corollary argument that this claim is indefinite and therefore invalid.

27. "Provided for the variable"

Claim 9 of the '846 patent recites a limitation of "system tag means for storing a system tag which indicates one of a plurality of cache data storage modes, each cache data storage mode being *provided for the variable* for each page of data stored in said primary memory." (emphasis added). The defendants contend that the terms "provided for the variable" are vague, rendering the claim indefinite. The plaintiff argues that this claim term is an obvious typographical error, amenable to correction by this court. According to the plaintiff, the claim language should have read "provided for *and* variable for each page of data stored in said primary memory."

The court has carefully reviewed the '846 patent and in particular this term in the light of the specification. Under Novo Industries, L.P. v. Micro Molds Corp., 350 F.3d 1348, 1357 (Fed.Cir.2003), a district court can correct a typographical error in a patent only if (1) the correction is not subject to reasonable debate based on consideration of the claim language and the specification and (2) the prosecution history does not suggest a different interpretation of the claims. Although the better practice is for the patentee to apply to the Patent Office for a certificate of correction, the court is persuaded that "provided for the variable" as used in Claim 9[h] is an obvious typographical error as the correction is not subject to reasonable debate based on the court's consideration of the claim language and the prosecution history does not suggest a different interpretation of the claims. The court therefore construes this term to mean "provided for and variable for each page of data stored in said primary memory."

28. "Cache memory management means"/"Cache management means"

The defendants assert that claims 11-13 of the '846 patent are indefinite because the claim terms cache memory management means and cache management means in those claims lack a clear antecedent basis. In determining whether the claim is sufficiently definite, the court must analyze whether one skilled in the art would understand the bounds of the claim when read in light of the specification. Allen Engineering Corp. v. Bartell Industries, Inc., 299 F.3d 1336 (Fed.Cir.2002). The court has reviewed the parties' summary judgment briefing on this point and concludes that, in the context of claim 11, that the patentee's use of the term "cache memory management means" would be understood by one of ordinary skill in the art to refer to the "integrated cache memory system" recited in claim 9. Moreover, one of skill in the art would understand the bounds of claim 11 to merely add another element of "primary memory control means" to the integrated cache memory system described in claim 9. Claim 11 is therefore not indefinite.

Turning next to claim 13, the court concludes that the patentee's use of the term "cache memory management means" would be understood by one of ordinary skill in the art to refer also to the "integrated cache memory system" recited in claim 9. Moreover, one of skill in the art would understand the bounds of claim 13 to be the specifying of further operational behavior of the integrated cache memory management system. Claim 13 is therefore not indefinite.

4. Conclusion.

The court has construed the claim terms in dispute. To the extent the court has not specifically set forth a definition for a claim term raised in the parties' briefing and/or oral arguments, the court has concluded that the term either needs no definition or is otherwise adequately implied by the reasoning of the court.

So **ORDERED** and **SIGNED** this *30th* day of June, 2004

E.D.Tex.,2004.
Intergraph Hardware Technologies Co. v. Hewlett-Packard Co.