United States District Court,
W.D. Texas, Austin Division.

VIA TECHNOLOGIES, INC. and,
v.
INTEL CORPORATION.

No. A-01-CA-602-SS

March 17, 2003.

A. Joy Arnold, Birch M. Harms, Bryan J. Vogel, David G. Lindenbaum, Derek M. Kato, Franciscus A. Ladejola-Diaba, Gene W. Lee, Jeffrey D. Blake, John M. Hintz, Khue V. Hoang, Laurence S. Rogers, Robert C. Morgan, Sasha G. Rao, Theresa A. Moehlman, W. Edward Bailey, Fish & Neave, New York, NY, Christa P. Worley, Fish & Neave, Jennifer A. Ochs, Wilson, Sonsini, Goodrich & Rosati, Norman H. Beamer, Fish & Neave, Robert P. Feldman, Rodney G. Strickland, Jr., Wilson Sonsini Goodrich & Rosati PC, Palo Alto, CA, Lin Hughes, Patton G. Lochridge, McGinnis, Lochridge & Kilgore LLP, Austin, TX, Richard L. Rainey, Roderick R. McKelvie, Fish & Neave, Washington, DC, for Plaintiffs.

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ORDER

SAM SPARKS**, District Judge.**

BE IT REMEMBERED on the *17th* day of March 2003 the Court reviewed the file in the above-styled cause, specifically Via Parties' Motion for Summary Judgment that Intel's '423 Patent is Invalid as Indefinite [# 107], Intel's opposition thereto [# 134] and Via's reply [# 148]; Via Parties' Motion for Summary Judgment that Intel's '043 Patent is Invalid as Indefinite [# 108], Intel's opposition thereto [# 135] and Via Parties' reply [# 147]; the Special Master's Report and Recommendation [# 295]; and the parties objections thereto [# 333, # 337]. Having considered the motions and responses, the Report and Recommendation of the Special Master and objections thereto, the *Markman* testimony and evidence, the case file as a whole and the applicable law, the Court enters the following opinion and orders.

I. Summary Judgment Standard

VIA Technologies, Inc. (Taiwan), Centuary Technology, Inc., VIA-Cyrix, Inc. and VIA Technologies, Inc. (US) (collectively, "VIA") move for summary judgment that Intel Corporation's ("Intel") U.S. Patent No. 5,201,043 ("the '043 patent") and U.S. Patent No. 5,555,423 ("the '423 patent") are invalid as indefinite

under 35 U.S.C. s. 112, para. 2. Section 112, paragraph 2 of the Patent Act states: "The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention." 35U.S.C. s. 112, para. 2. The Federal Circuit has identified the following standard for determining whether a patent claim is sufficiently definite to satisfy s. 112, para. 2: "If one skilled in the art would understand the bounds of the claim when read in light of the specification, then the claim satisfies section 112 paragraph 2." Exxon Research & Eng'g Co. v. United States, 265 F.3d 1371, 1375 (Fed.Cir.2001). In other words, courts must determine whether the claims are" 'sufficiently precise to permit a potential competitor to determine whether or not he is infringing.' " Exxon Research, 265 F.3d at 1375 (quoting Morton Int'l, Inc. v. Cardinal Chem. Co., 5 F.3d 1464, 1470 (Fed.Cir.1993)). Indefiniteness is a question of law. Atmel Corp. v. Information Storage Devices, Inc., 198 F.3d 1374, 1378 (Fed.Cir.1999).

In deciding whether a claim is invalid for indefiniteness, courts must acknowledge the presumption of validity that applies to all patents. 35 U.S.C. s. 282. To rebut that presumption, the party seeking summary judgment must prove facts establishing invalidity by clear and convincing evidence. Apple Computer, Inc. v. Articulate Sys., Inc., 234 F.3d 14, 20 (Fed.Cir.2000).

Section 112, paragraph 2 has a special application to means-plus-function terms to which s. 112, para. 6 applies. Section 112, paragraph six states: "An element in a claim for a combination may be expressed as a means or step for performing a specified function without the recital of structure, material, or acts in support thereof, and such claim shall be construed to cover the corresponding structure, material, or acts described in the specification and equivalents thereof." 35 U.S.C. s. 112, para. 6. The claims at issue in VIA's summary judgment motions contain means-plus-function terms that invoke s. 112, para. 6. The Federal Circuit has interpreted this paragraph as a *quid pro quo:* inventors may use a generic "means for" expression in a claim so long as the specification indicates what structure constitutes the means for performing the claimed function. Atmel, 198 F.3d at 1381. For a means-plus-function term to meet the definiteness requirement of s. 112, para. 2, "the corresponding structure(s) of a means-plus-function limitation must be disclosed in the written description in such a manner that one skilled in the art will know and understand what structure corresponds to the means limitation." Atmel, 198 F.3d at 1382. If there is no corresponding structure disclosed in the specification, the claim is indefinite under paragraph 2.

II. '043 Patent

VIA contends the claim element "system for generating memory requests with alignment checking ..." in claim 8 of the '043 Patent is indefinite. The Court construed this term as a means-plus-function term invoking s. 112, para. 6 because, even though the term does not contain the "means for" language, the term "relies on functional terms other than structure or material to describe performance of the claimed function." Micro Chem. Inc. v. Great Plains Chem. Co., 194 F.3d 1250, 1257 (Fed.Cir.1999). Use of the word "means" creates a rebuttable presumption that s. 112, para. 6 applies, whereas failure to use the word "means" creates a presumption that it does not apply. Personalized Media Comm., LLC v. Int'l Trade Comm'n, 161 F.3d 696, 703-04 (Fed.Cir.1999). In deciding whether either presumption has been rebutted, courts focus on "whether the claim as properly construed recited sufficiently definite structure to avoid the ambit of s. 112, para. 6." Personalized Media, 161 F.3d at 704.

This claim element does not recite sufficiently definite structure; it merely refers to a "system" that is within a microprocessor device and the functions the system performs. A "system" for performing a certain function is no more structural than a "means" for performing a system, as VIA's expert testified: "I don't see

a difference and one of ordinary skill would not see a difference between the word 'system,' and the word 'thing,' or the word 'means.' Itjustmeans something, and it does not connote structure." *Markman* Transcript ("Tr."), Vol. 4, at 57. Likewise, the expert testified, the functional language following "system" adds no structure. Tr. Vol. 4, at 57-58. The Court agrees the phrase "system for" in the context of claim 8 is as inherently functional as the phrase "means for." Intel's argument in its summary judgment response that the term connotes structure because one of ordinary skill would understand the system as "a group of circuitry," simply because it is located within a microprocessor device, is not persuasive. Intel's Response, at 8. Likewise, Intel's expert's testimony at the *Markman* hearing that the system's location within a microprocessor and its inputs and outputs (*i.e.* its functions) constitute sufficient structure is unpersuasive: "I know it's of the firmware, or circuitry, or microcode style, because it's contextually dealing with the microprocessor device. I know what it receives as its inputs, and I know what it generates as its output ...." Tr. Vol. 4, at 19. Even if Intel's expert were correct that a person of ordinary skill would know the "system" is "of the firmware, or circuitry, or microcode style," that is not sufficient structure to avoid invocation of s. 112, para. 6. Accordingly, the Court finds VIA has overcome the presumption that s. 112, para. 6 does not apply to terms without the "means for" language.

When applying s. 112, para. 6 to a term, a court construes the term by first identifying the claimed function in the claim limitation and then determining what structure disclosed in the specification is associated with that function. *Cardiac Pacemakers,* 296 F.3d at 1113. If the court determines, from the perspective of one of ordinary skill, no embodiment in the specification discloses corresponding structure, the claim is invalid as indefinite under s. 112, para. 2. *Cardiac Pacemakers,* 296 F.3d at 1113-14. The Court identified four functions of the term "system for generating memory requests with alignment checking of said memory requests": (1) generating memory requests, defined as generating a signal on a bus connected to memory, which signal contains a memory address, control information (*i.e.,* whether it is a read or write request and how many bits are desired), and if it is a write request, the data to be written; (2) alignment checking, explained as detecting misaligned data references (*i.e.,* the data address is not a multiple of its length); (3) receiving an enable signal, which is present when the alignment control bit and the masking bit are set; and (4) generating an alignment fault if a misaligned memory request occurs and the enable signal is present, which means generating a signal indicating a fault if the memory request is misaligned and the enable signal is present.

VIA and Intel agree the specification discloses structure to perform functions (2) and (3), but VIA contends the structure disclosed in the specification to perform functions (1) and (4) is indefinite. Intel asserts the specification discloses the segmentation unit 14 and control unit 19, depicted in Figure 4, as the structure for generating memory requests. The specification states: "Misaligned data reference faults are generated within the segmentation unit 14, which also generates linear addresses." '043 Patent, 7:67-8:1. The control unit 19, which is coupled to the segmentation unit 14, stores microcode instructions and provides sequences of control signals to the microprocessor. ' 043 Patent, 6:15-21. As Intel's expert testified, "In the late 1980's around 1989, one of ordinary skill would have understood that the segmentation unit in combination with the control unit generates memory requests. The control unit generates the control signals to generate a memory request and the segmentation unit converts the address to a linear address." Intel's Response, Rhyne Declaration at para. 13.

VIA contends a block diagram of a microprocessor, such as that in Figure 4, is insufficient structure and a person of ordinary skill would not have known the structure of the segmentation unit 14. The specification states, "For purposes of understanding the present invention, segmentation unit 14 may be assumed to be the same as that used in the commercially available Intel 80386 microprocessor. The segmentation and paging

units for the Intel 80386 microprocessor are described in co-pending application, Ser. No. 744,389 .... " '043 Patent, 5:67-6:6. Intel's expert testified "segmentation units, and the structure of those devices, were well-known to one of ordinary skill in the art during [the late 1980s around 1989], and had a well understood meaning in the art." Intel's Response, Rhyne Declaration at para. 9. Additionally, he stated "the reference to the segmentation unit of Intel's commercially available 80386 processor would be understood by one skilled in the art as structure capable of performing that function." *Id*. at para. 11; *see also* Tr. Vol. 4, at 49; Intel's Post-Markman Brief, Kudlac Ex. C-E. VIA's expert testified the structure of the 80386 processor was not known to people of ordinary skill in April 1989 and he could not find any structure of a segmentation unit described in computer architecture or microprocessor design textbooks from the late 1980s and early 1990s. Tr. Vol. 4, at 63-64. However, given Intel's evidence to the contrary, VIA has not presented the clear and convincing evidence necessary to declare a claim invalid. Accordingly, the Court finds the specification discloses sufficient structure for the function of generating memory requests.

VIA also argues the specification does not disclose structure for the function of "generating an alignment fault if a misaligned memory request occurs and the enable signal is present." The specification states: "AND gate 65 produces a signal called SINTR (segmentation unit interrupt) on line 67, which is coupled to control unit 19, whenever all of the above conditions are met. On receiving SINTR, the control unit immediately halts all execution and takes steps to service this alignment check fault.' " '043 Patent, 9:3-9. Figure 5 depicts AND gate 65 receiving an input from gate 63 and producing a SINTR signal on line 67. The specification describes the involvement of other gates in Figure 5 in the generation of the S I NTR signal. '043 Patent, 8:53-55; 8:64-9:6. VIA argues Figure 5 cannot be the structure for performing this function because Figure 5 will not generate an alignment fault unless four other conditions, in addition to the conditions "if a misaligned memory request occurs and the enable signal is present," are present. Intel's expert testified even if Figure 5, the preferred embodiment, had six conditions, it would still be appropriate structure to perform the function without the other conditions present. Tr. Vol. 4, at 27. The claim language identifying two conditions that must be present does not preclude other conditions from being present as well. Additionally, as both Intel's and VIA's experts testified, a person of ordinary skill reading the specification and examining Figure 5 could discern how to adapt it to a structure with only two conditions. Tr. Vol. 4, at 27, 90-91. Accordingly, the Court finds the specification and Figure 5 disclose adequate structure for the function of "generating an alignment fault if a misaligned memory request occurs and the enable signal is present," and VIA's motion for summary judgment on the '043 patent is denied.

III. '423 Patent

VIA also moves for summary judgment that the '423 patent is invalid as indefinite. In particular, VIA challenges the lack of structure disclosed to perform the means-plus-function terms "means for halting the microprocessor" (claim 1) (and, similarly, "means ... for halting operation of the microprocessor" (claim 7) and "transition means ... including means ... for halting operation of the microprocessor" (claims 2 and 7)); "means for re-initializing registers selected to place the microprocessor in its initial mode of operation" (claim 1); and "means for maintaining the contents of the floating point registers" (claim 2). The parties agree these are means-plus-function terms invoking s. 112, para. 6.

A. "means for halting the microprocessor"

VIA contends the specification fails to disclose any structure for performing the function of halting the microprocessor. Intel claims the specification discloses the circuitry within control unit 16. The term "halting" does not appear in the specification. The prosecution history reveals Intel inserted the term "means for halting" in response to the Patent Examiner's comment that: "In claims 1 and 14 responding to interrupts

... is vague and indefinite. If the function of responding is or includes halting the operation of the microprocessor as claimed in claim 18 (In.10-11) the function should be defined as such." VIA's Motion, Ex. A3, at 3. According to VIA's expert, the plain meaning of "halting" to a person of ordinary skill is "to cease execution in the microprocessor and go into a state where the only way to begin execution again would be to receive an enabled interrupt, such as a non-askable interrupt, or a reset." Tr. Vol. 3, at 174. VIA contends the specification discloses no structure for performing this halting function.

Intel asserts halting the microprocessor means the processor responds to a high-priority interrupt, and points to the specification's discussion of a high-priority interrupt performed by the INIT pin 14 and processed in the control unit 16. '423 Patent, 5:58-59 ("When asserted, the INIT pin 14 performs a high-priority interrupt within the control unit 16 after it is recognized."); Fig. 3; *see also* Tr. Vol. 3, at 100-01. In explaining "halting" as responding to a high-priority interrupt, Intel essentially replaces the word "halting" with "suspending," as its expert did at the *Markman* hearing: "that standard approach [to responding to interrupts] would include *suspending* the current operating program in favor of responding to the interrupt." Tr. Vol. 3, at 102 (emphasis added). However, Intel has not supported its unilateral decision to redefine "halting" as "suspending" after representing to the Examiner that "halting" is the correct word to describe the claimed function. Intel's expert conceded "suspending" is the word people commonly use to describe a response to an interrupt. *Id*. at 134. He also testified a "halt" instruction in a microprocessor has a result distinct from a response to an interrupt and "effectively stops the whole process" until the microprocessor receives a new interrupt or reset. *Id*. at 135. Likewise, VIA's expert testified "an interrupt is a request for service and halting the microprocessor essentially freezes the microprocessor." *Id*. at 174-75. Intel cannot now alter its position from that it took in the prosecution history and maintain the microprocessor does not actually halt in response to the interrupt. Additionally, Intel cannot subsequently alter the ordinary meaning of "halting" to be "suspending." Because the specification discloses no structure to perform the function of "halting" operation of the microprocessor but only discloses structure for performing a high-priority interrupt and suspending operation of the microprocessor, Intel did not satisfy its burden under the *quid pro quo* of s. 112, para. 6. Accordingly, claims 1 and 7, as well as dependent claims 2, 5 and 9, are invalid as indefinite under s. 112, para. 2.

B. "means for re-initializing registers selected to place the microprocessor in its initial mode of operation"

VIA contends the specification identifies no structure for performing the function of re-initializing registers selected to place the microprocessor in its initial mode of operation and therefore claim 1 is invalid as indefinite. Intel claims the specification points to the "program for converting from second m o de to initial mode" within microcode programs 26 in Figure 2. '423 Patent, 6:13-15 ("In operation, the INIT re-initialization process accesses some of the microcode 26 that is programmed for RESET initialization."). The control unit 16 executes these microcode programs to re-initialize the registers and place the microprocessor in its initial mode of operation.

However, aside from asserting the means for re-initializing is a microcode program and pointing to a box in a diagram titled "program for converting from second mode to initial mode," the specification gives no further guidance as to the structure of that microcode other than it is "a relatively small amount of additional code." '423 Patent, 4:40-41. In the description of the preferred embodiment, the specification states: "Thus, the INIT re-initialization microcode program 54 can be implemented utilizing RESET microcode program 56 already provided therein, with some additional control microcode programming." '423 Patent, 6:40-43. However, none of the figures in the patent depict programs 54 or 56, and the specification does not refer to

them at any other point. The prosecution history indicates the programs are from a different application in the same chain of applications that did not issue as a patent and the programs were included at some point in Figure 2 but not in the final Figure 2 issued in the patent. Moreover, the reference to the RESET microcode program does not add structure to the otherwise mysterious box for microcode program 26 in Figure 2, because Intel represented to the Examiner that resetting the register is hardware-oriented in this patent, unlike re-initializing the registers, which is microcode-oriented. VIA's Markman Appendix, Hughes Affidavit Ex. F, at 94-95. Without a meaningful reference to known microcode, Intel provides no structure in the specification for microcode program 26. VIA's expert testified creating that microcode would be a complicated project. Tr. Vol. 3, at 181-82. While Intel's expert testified a person of ordinary skill would understand the program as connoting specific structure, this conclusory assertion does not explain where that structure is described in the specification. Tr. Vol. 3, at 92-93. The Court finds Intel did not disclose sufficient structure to perform the function of re-initializing registers and, therefore, did not meet its burden under s. 112, para. 2. Accordingly, claims 1, 2 and 5 of the '423 patent are invalid as indefinite.

C. "means for maintaining the contents of the floating point registers"

VIA contends the patent does not disclose sufficient structure to perform the function of maintaining the contents of the floating point registers. Again, Intel relies on the structure provided by the "program for converting from second mode to initial mode" in microcode program 26 in Figure 2 of the patent. FN1 However, as discussed above, the patent does not disclose the structure of the microcode program but merely explains the functions it performs. Although Intel's expert testified one of ordinary skill would understand how to implement the structure, that conclusion is contradicted by VIA's expert and unsupported by the specification. Tr. Vol. 3, at 112-13. Accordingly, claim 2 of the ' 423 patent is invalid as indefinite.

FN1. The Court need not reach the question of whether the specification actually discloses microcode 26 as structure for this function, although the reference in the specification is vague at best: "In operation, the INIT re-initialization process accesses some of the microcode 26 that is programmed for RESET initialization. For the floating-point registers 25, a value is maintained that is identical to the value prior to applying the electrical signal to the INIT pin 14 ...." '423 Patent, at 6:13-16. The use of passive voice in the specification complicates the search for structure even further.

In accordance with the foregoing:

IT IS ORDERED that the Report and Recommendation of the Special Master [# 295] is ACCEPTED;

IT IS FURTHER ORDERED that Via Parties' Motion for Summary Judgment that Intel's '423 Patent is Invalid as Indefinite [# 107] is GRANTED;

IT IS FINALLY ORDERED that Via Parties' Motion for Summary Judgment that Intel's '043 Patent is Invalid as Indefinite [# 108] is DENIED.

W.D.Tex.,2003.
Via Technologies, Inc. v. Intel Corp.