United States District Court,
N.D. California.

LG ELECTRONICS, INC,
Plaintiff and Counterclaim Defendant.
v.
ASUSTEK COMPUTER, INC., and Usus Computer International,
Inc.
Bizcom Electronics, Inc., Compal Electronics, Inc., and Sceptre Technologies,
Inc.
First International Computer, Inc. and First International Computer of America,
Inc.
Q-lity Computer, Inc., Quanta Computer, Inc., and Quanta Computer USA,
Inc.
Everex Systems, Inc,
Defendants and Counter claimants.

Nos. C 01-00326 CW, C 01-02187 CW, C 01-01375 CW, C 01-01552 CW, C 01-01594 CW

Aug. 20, 2002.

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ORDER CONSTRUING DISPUTED TERMS AND PHRASES

CLAUDIA WILKEN**, District Judge.**

Plaintiff LG Electronics, Inc. (LGE) has sued Defendants Asustek Computer, Inc. and Asus Computer International, Inc. (Asustek); First International Computer, Inc. and First International Computer of America, Inc. (First International); Bizcom Electronics, Inc., Compal Electronics, Inc. and Sceptre Technologies, Inc. (Compal); FN1 Q-Lity Computer, Inc., Quanta Computer, Inc. and Quanta Computer USA, Inc. (Quanta) and Everex Systems, Inc. (Everex) alleging infringement of six patents held by LGE: U.S. Patent Nos. 4,918,645 ('645 patent); 4,939,641 ('641 patent); 4,926,419 ('419 patent); 5,077,733 ('733 patent); 5,379,379 ('379 patent); 5,892,509 ('509 patent).

In general, these patents may be divided into three groups. The first group includes the '645 patent, the '641 patent and the '379 patent. These patents relate to computer memory access and management. In particular, the ' 645 patent discloses a high-speed memory access technique involving "page mode memory access;" the '641 patent involves a structure for maintaining data consistency between a high speed "cache" memory that is subject to continuous updating and a computer's main memory; and the '379 patent presents a technique for transmitting simultaneous read and write requests in a manner the prevents the "reading" of data from main memory when that data is the subject of a pending write request.

The second group includes the '419 patent and its continuation in part, the '733 patent. These patents disclose a system that permits multiple computer devices alternating access to a system bus. These patents address a problem caused by the constant transmission of data by a frequently used system component. So long as the frequently used component is transmitting data, it can prevent other system components from carrying out necessary functions that require the transmission of data. These patents address this problem through a rotating priority scheme wherein a component with access to the system bus must relinquish access to a waiting component when predetermined criteria are satisfied.

The final patent is the '509 patent. This patent discloses a system that allows remote access to shared memory in a computer system. The '509 patent purports to allow multiple computer users in multiple locations to work simultaneously on the same computer document.

The parties dispute the proper definition of several terms and phrases that are used in the patents. LGE, the AFC Defendants, and Quanta each ask the Court to adopt its proposed construction of the disputed terms and phrases. Everex has not submitted any proposed constructions. The matter was heard on June 28, 2002. Having considered the parties' papers, the evidence cited therein and oral argument, the Court construes the disputed terms and phrases as set forth herein.

DISCUSSION

I. Legal Standard

The interpretation of patent claims is a question of law to be decided by the Court. *See* Markman v. Westview Instruments, Inc., 517 U.S. 370, 371-73, 116 S.Ct. 1384, 134 L.Ed.2d 577 (1996). To interpret the claims of a patent, the Court must consider the language of the claims, the patent specification and the prosecution history. *See* Markman v. Westview Instruments, Inc., 52 F.3d 967, 979 (Fed.Cir.1995) (citations omitted), *aff'd,* 517 U.S. 370, 116 S.Ct. 1384, 134 L.Ed.2d 577 (1996).

In construing a claim, the Court must look first to the specific words of the claim. *See* Vitronics Corp. v. Conceptronic, Inc., 90 F.3d 1576, 1582 (Fed.Cir.1996). Words in the claim are given their ordinary meaning unless the inventor gives special meaning to them in the specification or prosecution history. *See id*. The specification may act as a dictionary when it defines terms in the claims, whether expressly or impliedly. *See id*. However, if the inventor gives a term a special meaning, that meaning must be reasonably clear and used consistently within the patent itself. *See* Lear Siegler, Inc. v. Aeroquip Corp., 733 F.2d 881, 889 (Fed.Cir.1984).

Interpretation of a disputed claim term also requires reference to the other claims. *See* Southwall Techs., Inc. v. Cardinal IG Co. ., 54 F.3d 1570, 1579 (Fed.Cir.1995). Each claim term must be interpreted consistently in all claims. *See id*. Ordinarily, the language of one claim should not be interpreted so as to make another claim, such as a claim dependent on the first claim, identical in scope. Claims should be interpreted to render all of the limitations in the claim meaningful. *See* Unique Concepts, Inc. v. Brown, 939 F.2d 1558, 1562 (Fed.Cir.1991). Nevertheless, "[w]hether or not claims differ from each other, one can not interpret a claim to be broader than what is contained in the specification and claims as filed." Tandon Corp. v. United States Int'l Trade Comm'n, 831 F.2d 1017, 1024 (Fed.Cir.1987).

Claims must be read in light of the specification. *See* Markman, 52 F.3d at 979. Claims, however, are not limited to the preferred embodiment described in the specification. *See* SRI Int'l v. Matsushita Elec. Corp. of Am., 775 F.2d 1107, 1121 (Fed.Cir.1985) (*en banc,* plurality opinion).

If the language of the claims, the specification and the prosecution history do not provide a clear definition for a claim limitation, the notice function of the patent claim is best served by construing the claim narrowly. *See* Athletic Alternatives, Inc. v. Prince Mfg., Inc., 73 F.3d 1573, 1580-81 (Fed.Cir.1996).

II. Claim Construction

A. Patent No. 645

The '645 patent discloses a technique for retrieving and transferring large amounts of data over a system bus through a process called "page mode memory access." In conventional memory access, each memory cell is separately accessed by asserting its "row address" and its "column address." In page mode memory access, an entire row of data is asserted followed by the assertion and deassertion of multiple column addresses. In this way, data is retrieved and transferred faster than through conventional memory access because the row address is asserted only once and large blocks of data on that row are accessed when the column addresses are asserted.

Claims 1 and 12 are the independent claims of the '645 patent. The parties dispute the proper construction of several terms and phrases in these claims.

1. "requesting agent"

LGE contends that "requesting agent" refers to an agent that has entered arbitration for bus access and initiates a transaction over the bus. Joint Claim Construction Brief (JCC) at 3.

Quanta construes "requesting agent" as a device connected to a system bus that requests access to a memory located on a replying agent. The AFC defendants concur in Quanta's proposed construction, but also contend that "requesting agent" incorporates an additional limitation in that it must receive or send data in a page mode manner.

The plain language of claims 1 and 12 supports Quanta's construction of the term. Both of those claims disclose that a "requesting agent" is coupled to a system bus, requests access to memory on the replying agent and retrieves that data over the system bus. "645 patent 10 :17-23; 12 :10-16. Quanta's proposed construction tracks the claim language. "[I]f the claim language is clear on its face then [the Court's] consideration of the rest of the intrinsic evidence is restricted to determining if a deviation from the clear language of the claims is specified." Interactive Gift Express, Inc. v. Compuserve, Inc., et al., 256 F.3d 1323, 1331 (Fed.Cir.2001).

Both LGE and the AFC Defendants contend that a deviation from this claim language is necessary, though they assert different deviations and different rationales.

LGE argues that its proposed definition of "requesting agent" is expressly incorporated into the specification and, therefore, controls over the plain claim language. "A deviation [from the clear language of the claim] may be necessary if 'a patentee has chosen] to be his own lexicographer and use terms in a manner other than their ordinary meaning.' " *Id*. (citing Vitronics Corp. v. Conceptronic, Inc., 90 F.3d 1576, 1582 (Fed.Cir.1996)).

The portion of the specification relied on by LGE states

Although the method and apparatus of the invention will be described herein in the context of a Multibus II environment, it should be appreciated that the invention may be practiced in many digital computer systems ...

The operating characteristics of the Multibus II are described in a document entitled "High Performance 32-Bit Bus Standard P1296" which was produced by the IEEE microprocessor standards committee P1296 working group, June 20, 1996, draft 2.0, the disclosure of which is incorporated herein in its entirety.

'645 patent 3 :51-56. The document referred to above, "High Performance 32-Bit Bus Standard P1296" (Multibus II Disclosure), contains a definition section that defines requesting agent in accord with LGE's proposed claim construction. Appendix to LGE's Opening Claim Construction Brief, Volume V, Tab 15 (Multibus II Disclosure), Chapter 2 "Definitions."

The Multibus II is, apparently, an embodiment of the '645 patent. '645 patent 3 :45-47 ("the method and apparatus of the invention will be described herein in the context of a Multibus II environment"). However, the ' 645 specification states that the invention is broader than the Multibus II. The definition section of the Multibus II Disclosure, moreover, specifically states that the definitions apply "for the P1296 specification." Multibus II Disclosure at 2-1. Because the Multibus II is not identical to the patent at issue, the Court will not adopt definitions relevant to that embodiment when construing the broader '645 patent. Consequently, the reference to the Multibus II disclosure in the '645 patent specification does not alone suffice to

incorporate into the '645 patent claims the definitions contained in this reference.

LGE also takes issue with Quanta's proposed construction that the requesting agent be "connected" to the system bus. LGE contends that the claim requires only that the requesting agent be "coupled" to the system bus. At the hearing on this motion, Quanta abandoned its objection to the use of the word coupled in the construction of "requesting agent." Because the claim uses the word coupled, and Defendants do not object to inclusion of that word in the construction, the Court will not stray from the language in the claim.

The AFC Defendants, relying on the doctrine of prosecution history estoppel, contend that a "requesting agent" must also receive and send data in a page mode manner. The AFC Defendants argue that in prosecuting the '645 patent, the patentee distinguished prior art on the grounds that none of the prior art taught the use of page mode memory access. File History (FH) 645 at LGE 000102.

The prosecution history, in this case, does not justify inclusion of page mode memory access in the construction of the term "requesting agent." Contrary to the AFC Defendants' assertion, prosecution history estoppel is not applicable at claim construction. Ballard Medical Products v. Allegiance Healthcare Corp., 268 F.3d 1352, 1358 (Fed.Cir.2001) ("prosecution history estoppel does not apply to the determination of literal claim scope"). The Court may look to the prosecution history to determine whether "a particular interpretation of a claim term [was] disclaimed by the inventor during prosecution." *Id*. (citing Biodex Corp. v. Loredan Biomedical, Inc., 946 F.2d 850, 863 (Fed.Cir.1991)). However, in order for the patentee to relinquish a particular construction, it must do so with "reasonable clarity and deliberateness." *Nothern Telecom Ltd. v. Samsung Electronics Co., Ltd.,* 215 F.3d 1231, 1294 (Fed.Cir.2000).

The prosecution history to which the AFC Defendants refer does not clearly indicate the patentee's desire to limit the construction of the term "requesting agent" by incorporating the requirement of page mode memory access. In fact, in the prosecution history passage cited by the AFC Defendants, the patentee distinguishes its invention from prior art on two grounds. The' patentee contends that the prior art "does not teach the accessing of memory on a replying agent over a system bus from a requesting agent *nor* does this reference teach the use of a page mode type of memory access over a system bus." LGE 000102 (emphasis added). The patentee could have been distinguishing its invention on either of the two grounds cited. The prosecution history is therefore insufficient to show that the patentee incorporated page mode memory access into this claim term.

In sum, in accord with the plain language of claims 1 and 12, the Court construes the term "requesting agent" to refer to a device coupled to the system bus that requests access to a memory located on a replying agent.

2. "replying agent"

In support of their constructions of "replying agent," the parties largely repeat the arguments they made in support of their constructions of "requesting agent."

LGE argues that the definition of "replying agent" found in the Multibus IT Disclosure is incorporated into the '645 patent specification. For the reasons already stated, the Court holds that the definitions in the Multibus II description do not constitute intrinsic evidence with respect to the '645 patent. The AFC Defendants and Quanta argue that, based on representations made during the prosecution of the patent, page mode memory access should be incorporated into the construction of replying agent. Defendants contend

that "replying agent," therefore, refers to a device that receives requests from the requesting agent and sends or receives data in a page mode manner. For the reasons already stated, the Court finds that the statements in the prosecution history are not sufficiently clear or deliberate to support the inclusion of page mode memory access in the construction of the term "replying agent."

In support of incorporating page mode function into the construction of replying agent, Quanta also relies on the overall purpose of the patent, *citing* Gentry Gallery, Inc. v. Berklin Corp. ., 134 F.3d 1473, 1478 (Fed.Cir.1998). Under the heading "Summary of Invention," the patent states that "the invention facilitates the transfer of blocks of data across a system bus by providing for a memory page mode type of access between the requesting agent and the replying agent." '645 patent 2 :49-52. Quanta concludes that the "replying agent" must incorporate the page mode memory access in order to comply with the patent's purpose.

Gentry Gallery, however, is inapplicable here. In that case, the court relied on unusually clear language in the written description that "described the location of a claim element ... as 'the only possible location' and that variations were 'outside the stated purpose of the invention.' " Johnson Worldwide Associates, Inc. v. Zebco Corp., 175 F.3d 985, 993 (Fed.Cir.1999) (citing Gentry Gallery, 134 F.3d at 1479)). In this case, although the '645 patent teaches page mode memory access, it is not "crystal clear" that the page mode claim element must be incorporated into the construction of the term "replying agent." Id. (patent's disclosure in *Gentry Gallery* made "crystal clear" that a particular understanding of a claim term was an essential element of the invention). In fact, the page mode memory access limitation is recited elsewhere in the patent. '645 patent 10 :52-53, 12 :34-35.

In accord with the plain language of claims 1 and 12 of the '645 patent, the Court construes the term "replying agent" to refer to a device coupled to a system bus that stores and retrieves data from memory and receives a memory access request from the requesting agent over the system bus.

3. "a system bus"

LGE and the AFC Defendants agree that "a system bus" is, at a minimum, "a plurality of shared signal lines that interconnects more than two agents for transmission of data, address, and control signals." Joint Claim Construction Chart (JCC) at 8; AFC Defendants' Joint Memorandum Re: Claim Construction (AFC Claim Construction Brief) at 21:3-4. Both parties seek to include additional limitations in this term. Quanta differs from LGE and the AFC Defendants in that it argues that the system bus in this claim connects only the "replying agent" and the "requesting agent," not any plurality of agents.

The AFC Defendants seek to include several additional limiting phrases in the construction of "a system bus." First, they contend that a system bus "must provide three clock signal lines ... for providing sychronizing clocks to the agents coupled to the bus." This limitation is not recited in claim 1, but is recited in claim 10, which is dependent from Claim 1. '645 patent at 11:67-12:6. Thus, the AFC Defendants' construction is disfavored under the doctrine of claim differentiation because it construes claim 1 in such a way as to make language in claim 10 superfluous. Comark Communications, Inc. v. Harris Corp., 156 F.3d 1182, 1187 (Fed.Cir.1987) (each claim in a patent is presumptively different in scope).

The AFC Defendants' reliance on the prosecution history in support of the "three clock signal" limitation is unavailing. The patentee stated in the Information Disclosure Statement (IDS) for the '645 patent that prior art does not disclose three clock signal lines. However, this statement has no relevance in construing claims

that do not recite that limitation. This statement may be relevant to the construction of claim 10, but that claim is not at issue here.

The AFC Defendants also contend that "a system bus" in the '645 patent must connect "at least one CPU and the main memory controller" and that it "must exclude a memory bus, a bus internal to a chip, or an extension bus." JCC at 8. The AFC Defendants contend that this construction of a "system bus" is the construction that one skilled in the art would assume and the one the patent examiner understood when he allowed the patent. However, the intrinsic evidence supports a broad definition of "system bus." *See* '645 patent at 1:22-25.

LGE contends that the phrase "if multiple requesting agents are present, arbitration determines access to the system bus" should be included in the construction of system bus. LGE does not provide evidentiary support for including this limitation, and the Court declines to adopt it.

Consistent with the language of the specification, the Court construes a "system bus" to refer to a plurality of shared signal lines for transmission of data, address, and control signals between a requesting agent and a replying agent. '645 patent 1 :22-25; 10 :17-19.

4. "memory control apparatus"

The AFC Defendants seek to incorporate limitations from the prosecution history into this claim term. However, there is no basis for applying the statements in the IDS to this term in claim 1, rather than to the claims that actually recite the limitations referred to in the IDS. In fact, doing so would be contrary to the claim differentiation doctrine and constitute an impermissible application of the doctrine of prosecution history estoppel.

Therefore, the Court construes memory control apparatus in accord with its plan meaning as an apparatus that controls access to memory.

5. "page mode type of memory access"

The specification teaches that page mode type of memory access is a means to access memory by asserting RAS once to latch the row address within the device and asserting and deasserting CAS a plurality of times to store and retrieve data. '645 patent at 6:3-8. The specification further teaches that RAS "can be considered to define a page of data bits within the device." Id. at 6:9. Although the specification indicates that RAS and CAS should be asserted at low voltage, this voltage-specific detail is not required by the claims.

Based on the specification, the Court adopts LGS's construction of this term, but incorporates one of the limitations proposed by the AFC Defendants: that page mode memory access must access a page of data. Page mode type of memory access, therefore, refers to a means of accessing memory cells by asserting an RAS signal associated with a page of data and asserting and deasserting multiple CAS signals in order to store and retrieve data.

6. "a completion of the access to memory"

The Court adopts LGE's construction of this term, which is consistent with its plain meaning. "A completion of the access to memory" means "as an end to the access to the memory." *See* CCS Fitness, Inc. v.

Brunswick Corp., 288 F.3d 1359, 2002 WL 837593 at (Fed.Cir.2002) (reference to "preferred embodiment or other structures or steps disclosed in the specification or prosecution history" insufficient to overcome "heavy presumption" that claim term carries its ordinary or customary meaning).

B. Patent No. 641

Most computer systems contain both main memory and cache memory capacities. Cache memory provides faster access to data than main memory. Cache memory is accessed separately from main memory during the operation of the computer and is continually updated. Cache memory, therefore, may contain more up-to-date information than the original data in main memory.

There are two ways that cache memory updates main memory to avoid retrieving "stale" data from main memory.

In a "write through" cache memory, data is written into main memory at the same time it is written into the cache. Write through cache memory maintains data consistency at all times, but requires excessive amounts of bus traffic, which can slow the operation of the computer.

In a "write back" cache memory, cache memory is updated during the operation of the computer, but the updated data is not transferred to main memory. Instead, the computer indicates that the data in cache memory is different than the original data in main memory. The more up-to-date data in cache memory is called "dirty" data and the computer maintains data integrity by responding to requests for data by retrieving the "dirty" data.

Write back memory can be problematic when more than one central processor (CPU) uses the same main memory. In this circumstance, the multiple processors each have their own cache memory. If data in the cache memory for CPU A, for example, is updated, the cache memory for CPU B must be informed not to retrieve data with the same address from its cache memory. One approach to resolving this problem is to mark the stale data in cache memory for CPU B as invalid. If that data is requested by CPU B, the invalid data is not retrieved and the request is rerouted to retrieve the dirty data from the cache memory in CPU A.

The '641 patent discloses a way to maintain data consistency throughout a multi-processor computing system without requiring excessive access to main memory, and without using valid/invalid data indicators. '641 patent 3 :11-67.

1. "one or more central processing units" (claim 1) and "at least one central processing units" (claim 14)

LGE construes these terms from claims 1 and 14 consistent with their plain meaning as referring to one or more central processing units. Defendants contend that, despite the ordinary and customary meaning of these terms, the specification shows that in the context of the '641 patent, the claim requires more than one CPU.

Where the claim language is clear on its face, the Court's consideration of the specification is limited to determining if the patentee intended a deviation from that clear language. Defendants rely on the title of the '641 patent, "Multi-Processor System with Cache Memories, ..." the "Field of Invention" section of the specification, which states that "this invention relates to multiprocessor computing systems which employ cache memories ...;" and the "Background of the Invention" section, which describes the "object of this

invention" as relating to multiple CPU environments. '641 patent at 1:6-9, 53-64. Defendants argue that "one or more central processing units" should be interpreted consistent with these statements from the specification which refer to "multiple" CPUs. *See* Gentry Gallery, 134 F.3d at 1479 (if "clear statements in the written description" indicate that a patentee's construction is "outside the stated purpose of the invention," the construction consistent with the written specification should control).

However, a separate, independent claim in the patent specifically discloses multiple CPUs. *See* '641 patent 13 :21-22 (claim 5 discloses "a data processing system including at least first and second central processing units"). Claims should not be construed in a manner that renders some claim language redundant or meaningless. Unique Concepts. Inc., 939 F.2d at 1562. Nor do limitations in the specification necessarily apply to every claim in the patent. At the claim construction hearing, LGS noted that cache coherency problems could arise in a single CPU environment because a device other than a CPU, such as a modem, could request data from main memory, or a single CPU could utilize multiple caches. The patent, therefore, has utility for a device containing only one CPU.

Therefore, because the multiple CPU limitation described in the specification is explicitly incorporated into Claim 5 of the patent, the disputed terms unambiguously refer to "at least one" CPU, and the specification does not indicate that the inventor intended all of the patent's claims to be limited to multiple CPUs, the Court adopts LGE's construction of these terms which is consistent with their ordinary and customary use.

2. "cache memory means" (claims 1, 5) "cache memory" (claim 14)

Title 35 U.S.C. s. 112 para. 6 provides,

An element in a claim for a combination may be expressed as a means or step for performing a specified function without the recital of structure, material, or acts in support thereof, and such claim shall be construed to cover the corresponding structure, material, or acts described in the specification and equivalents thereof.

"[I]f the word 'means' appears in the claim element, there is a presumption that it is a means-plus-function element to which s. 112 para. 6 applies. This presumption is overcome if the claim itself recites sufficient structure or material for performing the claimed function or when it fails to recite a function associated with the means." Seal-Flex, Inc. v. Athletic Track and Court Constr., 172 F.3d 836, 848 (Fed.Cir.1999) (Rader, J. concurring).

Both the AFC Defendants and Quanta argue that the term "cache memory means" should be construed as a means-plus-function claim element and, therefore, the Court should rely on the structure identified in the specification in interpreting this term. However, the presumption that s. 112 para. 6 applies is rebutted with respect to this claim term because there is no specific function associated with the "cache memory means" recited in the claim. "Without an identified function, the term 'means' in this claim cannot invoke 35 U.S.C. s. 112 para. 6." York Prods., Inc. v. Cent. Tractor Farm & Family Ctr., 99 F.3d 1568, 1574 (Fed.Cir.1996). Rather, the term "cache memory means" is followed by a description of its location (i.e. "coupled between the central processing unit and said bus means"). '641 Patent 12:43-44. Unlike "cache memory means," the remaining terms in claim 1 all recite a "means ... for" performing a specific function. This is in contrast to "cache memory means, indicating that no function is associated with that term. Because the claim recites a location for the "cache memory means," but no associated function, the term cannot be construed pursuant to s. 112 para. 6.

LGE argues that "cache memory" and "cache memory means" should be given their dictionary definition: "a small high speed memory located close to the CPU of a computer to give the CPU faster access to blocks of data than could be taken directly from the larger, slower main memory." *McGraw-Hill Electronics Dictionary,* 5th Ed., p. 68 (1994). LGE contends that the dictionary definition of cache memory is used throughout the specification. However, the portion of the specification relied on by LGE does not refer to the "cache memory" of the '641 patent, it describes prior art. '641 patent 1 :28-31 (describing how traditional "write-back cache" operates); *compare id.* at 1:41-66 (explaining how '641 patent resolves problems presented by traditional "write-back cache" memory).

Defendants contend that the "cache memory" claimed in the '641 patent differs from the dictionary-defined cache memory in two respects. First, Defendants argue that the '641 patent's "cache memory" never uses "valid" or "invalid" indications. The AFC Defendants further argue that "cache memory" refers to one of at least two cache memories.FN2

Under the heading "Background of the Invention," the patent specification describes the operation of a traditional write-back cache memory. Specifically, the specification states that when more than one cache memory is present, "each entry position in a cache is provided with a valid/invalid bit." '641 patent 1 :44-46. The limitation of using valid/invalid bits is then identified in the specification. "Thus, when a CPU accesses its cache at that particular data address, it finds an invalid entry and is redirected to main memory, a time consuming process." *Id.* at 49-52. One of the objects of the invention, therefore, is "to provide a cache memory system wherein the use of valid/invalid data indicators are avoided." *Id.* at 66-67.

Other portions of the specification provide further support for Defendants' construction limiting "cache memory" to a system that avoids the use of valid/invalid bits. Under the heading "Detailed Description of the Invention," the specification provides,

It should be kept in mind during the following description, that the invention maintains data integrity by assuring the cache data is always the most up-to-date in the system. Thus, there never is a 'valid' or 'invalid' indication with respect to any cache data as it is always assured that if data is provided by a cache, that it invariably is valid.

'641 patent 3 :28-34; *id.* at 3:40-43 ("The invention ... avoids the need for any directory or other listing of valid and invalid data ...). Therefore, the specification teaches that the '641 patent's "cache memory" differs from previous write-back cache memory systems by avoiding the use of valid/invalid bits.FN3

In addition, the '641 patent improves upon earlier data coherency systems by avoiding problems associated with multiple CPU, multiple cache systems. ' 641 patent 1 :46-59. Thus, figures 2a and 2b, illustrating a "high level block diagram of the invention," show that each CPU has an associated cache. The invention, moreover, includes various components intended to monitor and maintain consistency among multiple cache memories. These components include the "shared bit register" which informs the associated cache when another cache in the system contains the same data, '641 patent 4 :48-52, and the "cache controller" which "knows whether the data being sought is present in cache data store ...; whether it is dirty or not; and whether it is shared or not ." *Id.* at 6:44-47.

In sum, the Court does not construe "cache memory means" and "cache memory" pursuant 35 U.S.C. s. 112 para. 6. "Cache memory means" in claims 1 and 5 of the '641 patent and "cache memory" in claims 1, 5 and

14 of the '641 patent denote one of at least two high speed memories located close to the CPU of a computer to give the CPU faster access to blocks of data than could be taken directly from the larger, slower main memory and never using valid/invalid bits.

3. "a hold signal," "asserting a hold signal," and "a HOLD signal line"

Claim 1 of the '641 patent describes "means ... for asserting a hold signal...." The parties agree that "hold j signal" should be construed, consistent with its description in the claim itself, as a signal "indicating to the bus connection requesting the data unit that another data unit may be transmitted over the requesting bus connection." LGE's Opening Claim Construction Brief at 17-18; AFC Defendants Joint Memorandum Re: Claim Construction at 30; *see also* FH641 patent at LGE001077 (scope of the claims "has been more succinctly set forth by including language descriptive of the function of the hold line ...").

The AFC Defendants contend that an additional limitation found in the specification should be incorporated into the construction of "a hold signal." Specifically, the AFC Defendants argue that a hold signal not only indicates the presence of another data unit, but also informs the requesting bus connection not to release the bus. "When a cache controller asserts its hold line, all other potential users of the system bus are kept off the bus until the hold line is released." '641 patent 5 :22-24.

The inclusion of this limitation in the construction of "hold signal" would contravene the claim differentiation doctrine. Dependant claim 2 differs from claim 1 only in that the bus connection, "in response to sensing the assertion of said hold signal, maintains an interaction with said bus means...." '641 patent 12 :66-13 :3. The limitation Defendants wish to include in claim 1 is, therefore, explicitly included in claim 2 and the doctrine of claim differentiation counsels that these claims should be read differently. *See* Unique Concepts, Inc. v. Brown, 939 F.2d 1558, 1562 (Fed.Cir.1991). In sum, because the term "hold signal" is defined in the claim itself and the adoption of Defendants' additional limitations would violate the claim differentiation doctrine, the Court adopts LGE's construction of "hold signal."

Similarly, a "HOLD signal line" in claim 14 is construed in accord with the definition within the claim as a signal line that "indicat[es] to the bus connection initiating the read operation that at least one of the data units associated with the address is stored within the cache memory and that the cache memory will, if the data unit is determined to be marked as dirty within the cache memory, transmit the stored data unit to the bus connection during a subsequent bus cycle." '641 patent 14 :50-56. The requirement that a "HOLD signal line" also indicate that the bus connection "not release the system bus" is not found in the claim and should not be imported from the specification.

4. "bus monitor means associated with said cache memory means and coupled to said bus means for detecting on said bus means an address associated with a data unit transferred from said main memory means to a bus connection requesting the data unit" (claim 1)

The parties agree that this term is a means-plus-function term that must be construed pursuant to 35 U.S.C. s. 112 para. 6. The parties also agree that the relevant structure for performing the functions described in this claim are Address Bus Interface 52, 52' and Cache Controller 40, 40'. JCC Tab C at 14. The function recited in the claim is "detecting on said bus means an address associated with a data unit transferred from said main memory means to a bus connection requesting the data unit." 641 patent 12 :46-49. LGE argues that the Court should adopt the language from the claim in construing the function of this term pursuant to s. 112 para. 6.

Defendant Quanta emphasizes that the "bus monitor means" monitors the bus means for an address sent *from* the system memory and does not monitor the bus means for *an* address sent *to* the system memory. Quanta Responsive Claim Construction Brief at 15. The construction proffered by LGE, however, states that the function of the "bus monitor means" is to detect "an address associated with a data unit *transferred from* said main memory means." JCC, Tab C at 14 (emphasis added). LGE's construction, therefore, incorporates the limitation sought by Quanta and no revision of that construction is necessary.

The AFC Defendants seek two additional limitations on the construction of this term. First, they assert that the "bus monitor means" must "continuously monitor" the system bus to detect an address of a transferred data unit. Second, the AFC Defendants argue that the "bus monitor means," in addition to detecting an address associated with a data unit transferred, must also "cause the physical address of the data return to be latched in the address bus interface of the cache memory means." AFC Defendants' Joint Memorandum at 29.

In support of the first limitation, the AFC Defendants rely on the specification, which states, "Each cache controller continuously monitors system bus 42 for two types of operations.... It is this continuous monitoring which greatly assists the system to maintain data integrity." '641 patent 7 :11-25. Because each cache controller constitutes part of the structure of this means-plus-function term, the AFC Defendants argue that functions performed by this structure, as detailed in the specification, should be included in the construction of the claim. Thus, they argue that the "bus monitor means" must "continuously monitor" the system bus.

The AFC Defendants also argue that this means-plus-function claim term includes the functional requirement of "causing the physical address of the data return to be latched in the address bus interface of the cache memory means." This limitation, like the proffered requirement that the "bus monitor means" "continuously monitor" the bus, is based on language in the specification describing functions performed by the structure disclosed in this term. Specifically, the specification states "cache controller 40 causes the physical address of the data being accessed to be latched in address bus interface 52." 641 patent 8 :36-38.

The Court declines to add additional functions to the clear functional language stated in the claim. In this case, the patentee has limited the functions relevant to this means-plus-function claim term by specifically identifying the relevant function in the claim. Therefore, other functions that may be performed by the same structure should not be incorporated into the construction of this term. The "bus monitor means" need not "continuously monitor" the bus means. It must only monitor the bus means in order to detect "an address associated with a data unit transferred from said main memory."

"Bus monitor means ..." in claims 1 and 5 is a means-plus-function claim term. The structure associated with this term is the structure agreed upon by the parties. The function associated with this claim term is "detecting on said bus means an address associated with a data unit transferred from said main memory." FN4

5. "data unit transferred"

LGE contends that a "data unit transferred" is a data unit "in the process of being transferred" or "in transit" from one system component to another. JCC, Tab C at 17. Quanta agrees that a "data unit transferred" is "being transferred." *Id*. The AFC Defendants, however, argue that a "data unit transferred" is a data unit "having already been transferred." The AFC Defendants rely on the plain meaning of the term transferred,

which is in past tense. However, the Court must construe each claim term consistently in all claims. Southwall Techs., Inc. v. Cardinal IG Co., 54 F.3d 1570, 1579 (Fed.Cir.1995).

The Court has already construed the term "bus monitor means." This term is used in claims 1 and 5. Claim 1 describes the function of "bus monitor means" as "detecting ... a data unit transferred from said main memory means." '641 patent 12 :46-48. Claim 5 describes the function of "bus monitor means" as "detecting ... a data unit being read from said main memory means." *Id*. at 13:29-31. Because the term "bus monitor means" must be construed consistently throughout the patent, "data unit transferred" as used in claim 1 must, at a minimum, encompass "being read from" as used in claim 5. This reading, moreover, is consistent with the specification which refers to data "being returned to another requester" and "being read from main memory." *See* ' 641 patent 5 :25-29, 7 :49-53. Therefore, a "data unit transferred" is construed as a data unit in transit from one system component to another.

6. "another data unit"

The construction of this term is plain from the *claims* in which it is recited. The claim refers to means "for determining if data having the same address as said transferred data unit is present in said cache memory." '641 patent 12 :51-53. If so, a hold signal indicates to the bus connection "that 'another data unit' may be transmitted over said bus means." *Id*. at 12:56-58. As noted above, "transferred data" refers to data being read from main memory. A "hold signal" indicates the existence of "another data unit." From this context, it is clear that "another data unit" refers to a data unit different from, but with the same address as, the data transferred from main memory. FN5

7. "bus means" and "system bus"

The AFC Defendants contend that "bus means" should be construed pursuant to section 112 para. 6. However, "bus means" as used in claims 1 and 5 of the ' 641 patent does not recite a specific function. Therefore, the presumption that the term is a means-plus-function claim term is rebutted.

The Court agrees with LGE and Quanta that "bus means" in claims 1 and 5 has the same meaning as "system bus" in claim 14. *See* JCC, Tab C at 6, 60. LGE relies on extrinsic evidence in support of its plain meaning construction of the terms "bus means" and "system bus." *See* Dictionary of Electrical and Electronics Terms (4th Ed.1988) at 116 ("a signal line or a set of lines used by an interface system to connect a number of devices and to transfer information"); JCC, Tab C at 6. However, the AFC Defendants have also presented extrinsic evidence that the plain meaning of the term "system bus" is more narrow than that proposed by LGE. *See The Everything Computer Book* at 65 (2000) ("system bus is the primary pathway between its CPU and its main memory").

Because the terms "system bus" and "bus means" are not clear from the claim language, the Court looks to the specification for clarification of the meaning of this term. Figures 2a and 2b show that the system bus for the '641 patent is comprised of three separate bus lines: the data bus, address bus, and control bus. *See* '641 patent, figures 2a, 2b; 5:8-12 ("Communications between the main elements of the system ... occur on system bus 42. In actuality, system bus 42 is comprised of three separate bus systems, i.e. data bus 102, address bus 104 and control bus 106."). Based on this portion of the specification, the AFC Defendants argue that a "system bus" in the '641 patent is "a set of lines shared by all bus connections that carries address, control and data between the bus connections." AFC Defendants Joint Memorandum at 32.

The AFC Defendants also argue, based on the specification, that limitations relevant to the control bus-that

it is comprised of main control lines, a shared line, a bus lock line, and hold lines-should be included in the proper construction of the terms "bus means" and "system bus" in the '641 patent. ' 641 patent 5 :12-19.

The specification provides a specialized meaning for the terms "bus means" and "system bus." The preferred embodiment and the "Detailed Description of the Invention" show that the "system bus" of the '641 patent is composed of three separate and specific bus lines which carry address, control and data to other bus connections. Claim 14 provides further support for this construction, describing the function of a "system bus" as "conveying ... address information and data units associated with addresses between the system memory and other bus connections coupled to the system bus ...." '641 patent 14 :31-34.

However, the added limitations with respect to the "lines" that comprise the control bus are not properly considered in construing the term "bus means." The AFC Defendants argue that without the inclusion of these various lines, the system disclosed by the '641 patent would be inoperable. *See* Talbert Fuel Systems Patents Co. v. Unocal Corp., 275 F.3d 1371, 1376 (Fed.Cir.2002) ("We agree that a construction that renders the claimed invention inoperable should be viewed with extreme skepticism.")However, as was the case in *Talbert,* Defendants have "not demonstrated inoperability." *Id*.

Therefore, the Court construes "bus means" in claims 1 and 5 and "system bus" in claim 14 as "a set of lines that carries address, control and data between the bus connections."

C. Patent No. 419

Information is shared among various components of a computer over a pathway called a bus. When multiple devices compete for access to a shared bus, *a* priority scheme must be employed to assure that no one device "hogs" the bus. The '419 patent is directed towards an apparatus for determining priority of access to the bus. The '419 patent discloses a priority scheme created by multiple nodes attached to a shared bus with each node representing at least one device. One of the nodes is initially selected as the anchor node. The anchor node has the highest priority to the bus and the priority of all other nodes is determined with reference to their position relative to the anchor node. Under the '419 patent, each time a component requests access to the bus, the anchor node changes, causing the priority of all the nodes to change. Therefore, the '419 patent discloses a rotating priority scheme in which the priority of each component changes with each use of the bus by any component.

1. "bus," "device," and "the highest priority"

LGE presents arguments in support of its claim construction for the terms "bus," "device," and "the highest priority." Neither the AFC Defendants nor Quanta oppose these constructions in their claim construction briefs. The Court, therefore, adopts LGE's constructions of these terms.

2. "priority line"

LGE contends that a "priority line" in claims 1 and 9 of the '419 patent is "one or more dedicated (i.e. not shared) lines instrumental in creating a priority configuration among a plurality of nodes and determining a node's priority for using the bus during bus arbitration."

Both the AFC Defendants and Quanta contend that the priority line is limited to a single line rather than "one or more ... lines." However, the portion of the prosecution history relied on to limit the "priority line" to a single line states, "[t]he priority line *may be* but a single signal line and *need not be* a multiple number

of signal lines...." FH419 at LGE 000756 (emphasis added). This language from the prosecution history supports LGE's construction that the "priority line" may be one or more lines.

Quanta also contend that the "priority line" must "pass through the nodes in the system to form a loop." The AFC Defendants similarly construe "priority line" to connect the nodes "serially together in a circular configuration." LGE does not dispute that the "priority line" passes through each of the nodes in a circular configuration, but argues that these limitations are sufficiently recited in the claim and need not be incorporated into the term "priority line." Nevertheless, it is to the claim language that the Court first refers in construing claims. Claims 1 and 9 specifically state that "the priority line couples the nodes together in a circular configuration." '419 patent 21 :6-7; 22 :45-46. Consequently, the "priority line" must pass through all the nodes in a circular configuration.

The AFC Defendants also argue that the "priority line" must pass through at least three nodes. They base this construction on language in the claim stating that each node receives the "priority line" from a "first adjacent node" and provides the "priority line" to a "second adjacent node." ' 419 patent 20 :54-57. The AFC Defendants argue that the plain language of the claim requires at least three nodes: the first adjacent node, the node receiving the priority line from the first adjacent node, and the second adjacent node, to which the priority line is passed. LGE notes that the terms "first adjacent node" and "second adjacent node" were added to these claims during prosecution of the patent. They argue that the additional language was added to distinguish the invention from prior art in which the nodes were directly coupled to the bus. The import of the language, therefore, was not to determine the minimum number of nodes, but to make clear that the '419 patent taught a bus arbitration scheme where the nodes are coupled to each other through the priority line. FH419 at LGE 000714 ("The amendment clearly distinguishes Applicant's priority line which passes through each node, from Szeto's arbitration bus 22, which does not pass through any node.").

LGE's reference to the prosecution history is unpersuasive. The natural reading of the claim language suggests the existence of three nodes. The embodiment in the specification supports this reading in chat it shows *an* apparatus with at least three nodes. '419 patent, Figure 6; 16:63-68. If the patentee intended to emphasize the coupling of the nodes to each Other, this could have been done in a manner that did not refer to three separate nodes (e.g. each node ... receiving the priority line from and providing the priority line to an adjacent node).

Quanta includes two additional limitations in the construction of the term "priority line." First, Quanta argues that the "priority line" is "not an arbitration bus." In support of this limitation, Quanta relies on statements in the prosecution history distinguishing the claimed invention from prior art. Although it is true that during the prosecution history, the patentee distinguished "the priority line" from a specific bus structure disclosed in a cited prior art reference, this evidence is insufficient to support Quanta's contention that the patentee abandoned a construction of priority line that includes any arbitration bus.

Quanta's second limitation-that the priority line "pass from node to node a designation indicating the highest relative priority" among the nodes-is substantively similar to LGE's contention that the "priority line" is "instrumental in creating a priority configuration among a plurality of nodes and determining a node's priority for using the bus." The AFC Defendants insert no such functional limitation in their construction of "priority line." The claim language and prosecution history provide support for incorporating into the construction of "priority line" its role in determining which node has priority to access the bus. '419 patent 21 :8-10; 22 :41-43; FH419 at LGE000691 ("the current priority of a node in Applicant's system ... is determined by the physical location of the node on a priority line relative to the node which presently has

the highest priority"). The language proffered by LGE for this limitation is more consistent with the intrinsic evidence than that proffered by Quanta.

The Court construes "priority line" in claims 1 and 9 of the '419 patent as one or more dedicated lines passing through at least three nodes and connecting them together in a circular configuration; the priority line is instrumental in creating a priority configuration and determining a node's priority for using the bus during bus arbitration.

3. "node"

LGE construes the term "node" in claims 1 and 9 as "a mechanism by which an associated device is afforded access to a bus." The AFC Defendants construe the term as "circuitry that represents an associated device for determining access priority to the bus, and that is not a central arbiter." JCC, Tab B at 10; AFC Defendants Joint Memorandum at 8. These constructions differ in three respects.

First, the parties disagree on whether a "node" is a mechanism or is circuitry. Second, they differ on whether a "node" "represents an associated device for determining access priority" or "affords access to a bus" by an associated device. Third, the AFC Defendants seek a construction that a "node" is not a central arbiter.

The preferred embodiment in the specification discloses a node with "four main components." These components are, "priority logic[ ], anchor logic[ ], request logic[ ], and node grant logic." '419 patent 17 :16-19. The AFC Defendants rely on this embodiment to argue that the "node" must be circuitry. Because a "node" as described in the specification has logic, it must be circuitry. Therefore, the Court adopts the AFC Defendants definition of "node" as circuitry.

The AFC Defendants and LGE also dispute whether a "node" "represent[s] an associated device for bus arbitration and device priority purposes" or "afford [s] access to the bus" to an associated device. LGE's construction is consistent with the specification. *See* 1:29-30; 16:46-48. It is true that access to the bus is determined through bus arbitration with reference to the highest priority node. However, these elements of the claim are separately recited elsewhere. *See e.g.* 20:61-66 ("priority logic means"); 20:67-21:4 ("highest priority node specification means").

The AFC Defendants also seek a construction of the term "node" that precludes a node from being "a central arbiter." The AFC Defendants rely on the same portion of the prosecution history that Quanta relied on to argue that the "priority line" is not an arbitration bus. The Court concluded that the prosecution history did not support Quanta's construction of priority line. For the same reasons, the prosecution history does not provide such a broad restriction on the construction of the term "node."

In sum, the Court a "node" is circuitry by which an associated device is afforded access to a bus.

4. "first adjacent node" and "second adjacent node"

Claims 1 and 9 disclose "a group of nodes, *each* node representing a device and receiving a priority line from a first adjacent node and providing the priority line to a second adjacent node." '419 patent 22 :27-30.

LGE contends that the terms "first adjacent node" and "second adjacent node" in claims 1 and 9 have identical meanings: "a physically adjacent node." This construction follows from LGE's contention that the invention discloses a priority line with one or more nodes. Because LGE contends that the patent may be

practiced by an apparatus with only two nodes, the "first adjacent node" and "second adjacent node" may be the same node in some circumstances.

The AFC Defendants and Quanta, although offering slightly different constructions, both agree that the "first adjacent node" and "second adjacent node" refer to separate and distinct nodes on the priority line. Consequently, under either of their constructions claims 1 and 9 disclose an apparatus with at least three nodes. As noted in reference to the parties' construction of the term "priority line," the plain meaning of the claim language indicates that at least three nodes are required to practice these claims. For the reasons already discussed, reading this claim consistent with its plain language is supported by reference to the preferred embodiment in the specification. LGE's reliance on the prosecution history for its alternative construction of these terms is unpersuasive because the terms are clear on their face and consistent with the specification.

Comparing Quanta's and the AFC Defendants' constructions, Quanta's construction is more consistent with the terms here construed and the Court's earlier construction of the term "priority line." Therefore, "first adjacent node" is construed as "a node physically connected, with no intervening node, to the present node by the priority line passing through both nodes." "Second adjacent node" is construed as "a second node, also physically connected with no intervening node, to the present node by the priority line passing through both nodes; the second adjacent node is different from the first adjacent node, so that the priority line passing through the nodes may form a circular configuration."

5. "highest priority node specification means"

This is a means-plus-function term that must be construed under 35 U.S.C. s. 112 para. 6. The Court construes this term according to the identical constructions proffered by LGE and Quanta. The function of this term is "specifying whether the node is presently the highest priority node, and, if the node is presently the highest priority node, dynamically giving the highest priority to another of the nodes in response to an access to the bus by one of the set of devices." The structure corresponding to this function is AL 615 as shown in figure 6.

D. Patent No. 733

The '733 patent is a continuation in part of the '419 patent. It, like the '419 patent, discloses a rotating priority scheme for determining bus access. As noted, the '419 patent discloses *an* apparatus that rotates the anchor node (i.e. the highest priority node) after each access of the bus. Generally, the '733 patent discloses a rotating priority scheme where a single bus access will not cause the relative priorities of the nodes to change. Rather, the '733 patent allows a node to remain the anchor node until the "programmable node grant counter" reaches a preset number. The parties disagree on whether the counter increases only after each separate access of the bus by the device or whether the counter also increases upon the transition of the clock signal.

1. "counting the number of accesses by the device to the bus"

The AFC Defendants contend that this claim terra should be construed as a step-plus-function terra under 35 U.S.C. s. 112 para. 6. The claim recites "steps of ... counting the number of accesses by the device to the bus." Because the claim uses the term "steps of" rather than "steps for," the Court presumes that s. 112 116 does not apply. *See* Seal-Flex, Inc., 172 F.3d at 850 (Rader J. concurring). However, this presumption can be rebutted if "the claim element recites only the underlying function of the element itself as opposed to an

act for performing it." *Id*. In this case, the preamble to the claim recites the function of "determining priority of access to a bus ...." ' 733 patent 24 :65-66. The fact that a function is recited in the preamble of a claim does not automatically convert the separate elements of the claim into acts for performing that function. Seal-Flex, 172 F.3d at 850. However, with respect to this claim term, the specification supports a construction of claim 15 wherein the function is determining access to the bus and the acts for performing that function include "counting the number of accesses by the device to the bus." '733 patent 21 :19-44. Accordingly, "because this claim limitation is not in explicit step-plus-function form" and reference to the specification reveals that it discloses "an act associated with an underlying function," section 112 para. 6 does not apply. Seal-Flex, 172 F.3d at 851.

Without reference to section 12 para. 6, LGE construes this term to mean "counting a number of clock signals, each clock signal indicating that an access by the device to the bus has occurred." The AFC Defendants and Quanta argue that the term should be construed as "counting the number of times a device gains use of the bus." Under LGE's construction, the invention monitors the duration of a device's use of the bus and, after a preset period of time, the invention passes the highest priority to a different node in the circular configuration. Under Defendants' construction, on the other hand, the invention monitors the number of times a device accesses the bus. Defendants contend that the number of clock signals will sometimes be greater than the number of accesses by the device to the bus because the clock signals will transition during certain times when no device has accessed the bus. Therefore, Defendants argue that by construing this term with reference to "clock signals," rather than accesses of the device, LGE is fundamentally altering the manner in which the invention functions.

The dictionary definition of "access" agreed to by the parties is "to make use of." Defendants contend that their construction of "counting the number of accesses ..." incorporates this definition of "access" and is the only construction consistent with the plain meaning of the disputed term.

LGE contends that the definition of access is not relevant to the proper construction of this claim term because the specification explicitly equates counting the number of accesses with counting the number of clock signals.

In the preferred embodiment of the patent, programmable node grant counter (NGCNT) 720(1) is preset to a certain value corresponding to how many bus accesses a device is permitted before the highest priority is passed to the next node in the circular configuration. '733 patent 21 :56-64. After a device is granted initial access to the bus, NGCNT 720(1) increments by one with each passage of the bus clock signal. *Id*. 21:33-38. Upon reaching a preset number on NGCNT 720(1), the highest priority is passed to another node.

LGE argues that the number of "accesses by the device to the bus" is measured by NGCNT 720(1). NGCNT 720(1), moreover, is responsive to the bus clock signal. It increments with each "clock signal transition." When the counter reaches a predetermined number, it passes the highest priority to another node. Consequently, LGE argues that in this claim, "counting *a* number of accesses to the device" refers to the act performed by NGCNT 720(1). NGCNT 720(1) does not count separate uses of the bus, it counts clock signals after a device has initially accessed the bus.

LGE's explanation of the specification is not sufficient to justify its claim construction. Every transition of the clock signal does not result in an increment to NGCNT 720(1). Only after a device has satisfied four conditions necessary to initially access the bus will NGCNT 720(1) become responsive to clock signal transitions. '733 patent 21 :24-31. However, LGE's proposed construction indicates that every clock signal

"indicate[s] that an access by the device to the bus has occurred." In fact, only some clock signals will increment NGCNT 720(1)-those that occur after an initial *access* by the device. LGE's construction fails to account for the initial access to the bus by the device and incorrectly states that the device will construe every clock signal as an access to the bus.

Consequently, Defendants' construction, which is consistent with the plain language of the claim, is proper. The Court, therefore, construes "counting a number of accesses by the device to the bus" as counting the number of times a device gains use of the bus.

2. "predetermined number of accesses to the bus

Consistent with the above construction of "counting a number of accesses ...," this term refers to the number of times a device is granted access to the bus. The number of clock signal transitions registered on NGCNT 720(1) is not equivalent to the number of accesses to the bus.

3. "node"

LGE argues that "node" should be construed the same in both the '419 and ' 733 patents. Defendants contend that the term "node" in the '733 patent includes an additional limitation not found in the '419 patent. Specifically, Defendants contend that a programmable node grant counter is disclosed as part of the "node" in the '733 patent. They therefore seek to incorporate the limiting phrase "and includes a programmable node grant counter" in the construction of the term "node" in the '733 patent. Defendants' only support for adopting different constructions of the same term in related patents is a reference to the preferred embodiment of the '733 patent. Defendants offer no reason why this particular aspect of the preferred embodiment should be read into this claim term. Consequently, the Court construes node as it did in the *419 patent as a "mechanism by which an associated device is afforded use of a bus."

E. Patent No. 379

A read request is a request from a device connected to a bus to read data from main memory. A write request is a request from a device connected to a bus to write data to main memory. The '379 patent teaches a way of controlling the order in which read and write requests to main memory are executed. It discloses allowing read requests to proceed ahead of write request unless doing so would result in "stale" data being returned from main memory.

In the '379 patent, read and write requests pass through a memory controller on their way to main memory. The memory controller includes read and write "buffers" which store read and write requests before transmitting them to main memory. The memory controller compares the targeted memory address of each incoming read request to the target addresses of all buffered write requests. A read address that does not have a match in the write buffer will be performed. However, if the memory controller finds a match, it will perform the buffered write request first, then the corresponding read request to assure that the device does not read "stale" data from main memory.

1. "system bus"

LGE argues in favor of a broad construction of "system bus" as "a set of signal lines in a computer that are used to connect a plurality of components within the computer and transfer information there between." The AFC Defendants seek a narrower construction of "system bus" as "a shared bus coupling the memory

control unit, a plurality of bus connections and a plurality of CPUs, and excluding I/O and memory buses." The AFC Defendants' construction is based on the structure of "System Bus 12" in the preferred embodiment in the specification. The numerous limitations suggested by the AFC Defendants, if adopted, would render superfluous or contradict other terms in the claims.

For example, claim 1 discloses a "second interface means for coupling said memory control unit to a system bus...." This claim language would be superfluous if the "system bus" incorporated the limitation of coupling the memory control unit. The claim would, in effect, read "second interface means for coupling said memory control unit to a shared bus coupling the memory control unit...." Although the "system bus" may, in fact, couple the memory control unit to a plurality of bus connections, these limitations are expressly cited elsewhere in the claim and it is therefore not necessary to include them in the construction of "system bus."

The AFC Defendants' contention that the "system bus" couples a plurality of CPUs and excludes I/O and memory buses finds no support in the intrinsic evidence. The fact that system bus 12 in the preferred embodiment is separate from the I/O and memory buses does not counsel that the broader term in the claim necessarily excludes these features. Similarly, there is no justification in the intrinsic evidence for incorporating into the claim language the multiple CPUs depicted in the preferred embodiment. In addition, the prosecution history cited by the AFC Defendants in support of the "multiple CPU" limitation is unpersuasive. In context, it is clear that the patentee was distinguishing prior art based on the distinction between the patent-in-suit, which was directed toward memory control of main memory, and the prior art, which taught a memory control system for cache memory. FH37 9 at LGE002022 ("[T]he teaching of Ziegler is directed to an intercleaved cache memory for connection to a plurality of parallel processors. In contradistinction, the teaching of the instant invention is directed to a novel memory control unit for interfacing a system main memory to a system bus and, thence, to a plurality of CPUs and other bus agents.").

The intrinsic evidence does not provide support for the construction of "system bus" advocated by the AFC Defendants. Consequently, the Court adopts LGE's construction of the term. A "system bus" in the '379 patent is a set of signal lines in a computer that are used to connect a plurality of components within the computer and transfer information there between.

2. means for controlling the execution of read and write requests, said controlling means being coupled to said comparing means output signal and being responsive to said comparing means output signal not being asserted for causing an execution of all buffered read requests before any buffered write requests, said controlling means further being responsive to said comparing means output signal being asserted for first causing an execution of only those buffered read requests which precede a buffered read request which caused the assertion of said comparing means output signal and then causing the execution of buffered write requests (claims 1 and 23)

The parties agree that this is a means-plus-function term that must be construed pursuant to 35 U.S.C. s. 112 para. 6. LGE identifies the structure for th is means-plus-function element as Memory Interface State Machine (MISM) 72 and the corresponding function as "controlling the execution of read and write requests." LGE argues that this construction is compelled by the plain language of the claim. However the "means for controlling ..." claim term discloses more than the broad function of executing read and write requests. Specifically, the claim discloses that the controlling means executes the buffered read requests before the buffered write requests if no match occurs, and executes all buffered read requests up to the matching read request and then executes buffered write requests if a match occurs.

While LGE's construction fails to fully identify the function disclosed in the claim, Quanta's construction errs in the other direction. Quanta construes the function of this term as not only executing read and write requests in the specified manner, but also performing the function of "comparing the two addresses." However, the claim recites a separate means, comparing means, which is coupled to the controlling means, and performs the function of comparing the two addresses. The controlling means are responsive to outputs from the comparing means. Quanta may be correct that the order in which the controlling means executes pending read and write requests depends on the output signal provided by the comparing means. The controlling means do not, however, perform the function associated with the comparing means. Therefore, Quanta's construction must be rejected because it includes in this claim term a function in addition to the one described in the claim.

Quanta's reliance on the prosecution history in support of its construction of this term is unpersuasive. Quanta emphasizes that this claim term was added during the prosecution of the patent to overcome the examiner's objections. It is true that a patentee who amends his or her claims in order to distinguish prior art may be precluded from arguing for the construction it disclaimed through amendment. However, Quanta has not provided any evidence that its construction was the one intended by the amendment. The fact that the claim language resulted from amendment, standing alone, does not favor adopting Quanta's construction.

The AFC Defendants argue that the "means for controlling ..." must execute all buffered write requests before the matching read request if a match occurs. This claim states that, if a match is found then the "means" shall "cause the execution of buffered write requests." The language of the claim is ambiguous in that it could refer to all buffered write requests, or only to buffered write requests up to and including the matching request. For the proposition that "causing the execution of buffered write requests" signifies executing *all* buffered write requests, the AFC Defendants rely *on* the specification.

The relevant portion of the specification states,

It should be noted that the assertion of the RAMTCH signal indicates that the Write Buffer contains at least one, and possibly more, write operations that must execute before the read request which caused the assertion of the RAMTCH can start. As has been stated, the state of the Write buffer contents must be frozen at this point. This is due to the fact that all pending Write requests are executed before the execution of the Read request which caused the match.

'379 patent 12 :36-44. Figure 8 in the specification, moreover, shows a flowchart of the read address match sequence. Figure 8 indicates that read requests up to a matched read will be carried out, r.hen all write requests, followed by the matched read request. '379 patent, Fig. 8.

Because the claim language is not clear and the AFC Defendants' construction is consistent with the specification, the Court adopts this portion of the AFC Defendants' construction.

Consequently, the function of this means-plus-function term is "executing the buffered read requests before the buffered write requests if no match occurs, and executing all buffered read requests up to the matching read request and then executing all buffered write requests if a match occurs."

Although Defendants' broader construction of the function for this means-plus-function term is correct, the Court does not fully adopt the corresponding structure identified by Defendants. In particular, the function

of Terminator State Machine (TSM) 74 is to transfer the selected request to the bus. The function of transferring the read or write request is separate from controlling the executing of that request. Consequently, the structure associated with the "means for controlling ..." claim term is MISM 72 and multiplexer 96.

3. means responsive to the operation of said write request receiving and buffer means and to said request executing means for determining, at least during a time that said read request executing means is executing a buffered read request, when a predetermined number of write requests are buffered within said write request buffer means, the predetermined number being less than a maximum possible number of buffered write requests (claim 22)

LGE construes the function of this means-plus-function term as "determining when a predetermined number of write requests are buffered within said write request buffer means." LGE identifies TSM 74 as the structure corresponding to this function. Quanta argues that language found in the claim, but omitted from LGE's construction, should also be included in the construction of this term. In other words, according to Quanta, the term should be construed as means 1) that is responsive to said read request executing means; for 2) determining at least during a time that said request executing means is executing a buffered read request when a predetermined number of write requests are buffered within said write request buffer means; and 3) the predetermined number is less than a maximum possible number of buffered write requests.

Although the language proffered by Quanta reflects the language of the term being construed, that language is collateral to the function described in the claim. The Court is construing individual terms and phrases, not the entire claim. Simply because a phrase appears in a claim does not mean that it must be incorporated into the construction of a different, but related term. The parties have not briefed the construction of the terms "responsive to said read request executing means," "at least during a time that said request executing means is executing a buffered read request," or "the predetermined number is less than a maximum possible number of buffered write requests." All of these terms, however, are collateral to the function of the means-plus-function term that is presently before the Court. Therefore, the Court adopts LGE'S construction of this term, which is limited to the function recited in the claim. The function of this means-plus-function term is "determining when a predetermined number of write requests are buffered within said write request buffer means." The corresponding structure is TSM 74.

4. "preventing a reception of further read or write requests"

LGE arques that this term need not be construed because it is plain on its face. *See* JCC, Tab E at 75 (LGE's construction is identical in all respects to the term being construed). Quanta argues that this term is vague on its face and should be construed, based on the specification, as "forcing other read/write requesters to hold their bus operations." '379 patent 11 :55-66. The Court does not find the claim language ambiguous. The dictionary definitions of "prevent" and "receive" give sufficient clarity to the claim's terms. JCC, Tab E at 75. Therefore, reference to the specification is unwarranted and "preventing a reception of further read or write requests" is construed according to its plain meaning.

5. "second interface means"

The parties agree on the function of this means-plus-function claim term, but they disagree on the structure corresponding to that function. The function is "coupling said memory control unit to a system bus." The parties further agree that System Bus (SB) decode 76, input data latch 78, input address latch 80, output data latch 82, and output address latch 84 all constitute the means for performing this function. Quanta contends

that ISM 70 and TSM 74 are additional structures that correspond to the claimed function. Although the ISM 70 and TSM 74 provide signals that are critical to other functions in the claim, Quanta provides no evidence chat these structures actually perform the function stated in this claim term. Asyst Techs., Inc. v. Empak, Inc., 268 F.3d 1364, 1370 (Fed.Cir.2001) ("Structural features that do not actually perform the recited function do not constitute corresponding structure and thus do not serve as claim limitations.").

6. "comparing when received each read address against buffered write addresses, if any, to determine if a received read address has an address value within a predetermined range of address values of a buffered write address"

This claim term recites an act and is not governed by 35 U.S.C. s. 112 para. 6. *See* Seal-Flex, Inc., 172 F.3d at 850 (use of the phrase 'steps of' carries presumption that section 112 para. 6 does not apply). The AFC Defendants advocate a construction of this term that is substantially similar to the language in the claim with one variation. The AFC Defendants argue that the language "comparing when received each read address ..." should be construed as "comparing an incoming read address (not a buffered read address)...." The remainder of the AFC Defendants' construction of this term tracks the claim language.

The AFC Defendants' alteration to the claim language is supported by the prosecution history. During prosecution, the patentee distinguished the claimed invention from prior art by arguing that the prior art did not show "means for comparing a received read address, as opposed to a buffered read address, to write addresses stored in the write buffer." FH379 at LGE001874-1375. It therefore appears from the prosecution history that the claim term "comparing when received each read address" was intended to describe the act of comparing an incoming rather than a buffered read address. Although the Court does not construe this term as a step-plus-function claim term, it does construe it according to the AFC Defendants' proffered construction as " *comparing an* incoming address (not a buffered read address) against buffered write addresses, if any, to determine if a received read address has an address value within a predetermined range of address values of a buffered write address."

F. Patent No. S09

The '509 patent describes *a* system that enables two computer users, working on two different computer systems, to view and edit a single document at the same time. Each user has his or her own "image processing system." The image processing system of each user is connected to the other image processing systems via a network. Each image processing system within the network contains both common and personal memory. Personal memory is accessible only to the user associated with the image processing system in which that memory is contained. Common memory may be accessed by users at other image processing systems connected by the network.

1. "image processing system"

LGE contends that "image processing system" should be construed as "any device, such as a notebook computer, desktop computer, or server, that is capable of displaying images from files, such as word processing documents, spread sheets, bit maps and other file types from which images *can* be generated." LGE's construction broadly encompasses any device capable of processing electronic images. The AFC Defendants, on the other hand, proffer a construction of "image processing system" which incorporates myriad limitations identified in the specification. Defendants contend that an "image processing system" is "a first image processing system having multiple purpose-optimized, windowing-less displays that are clustered under and controlled by a single transparent energized conductive surface operating as an input

device; a stylus operative via the conductive surface; and an integrated real time full-duplex communication capability."

Defendants rely on selected portions of the specification to justify their deviation from the broad construction of "image processing system" proffered by LGE. For example, under "Field of the Invention," the specification states, "The present invention relates ... to a workstation comprising functionally integrated multiple displays that are clustered under a single transparent energized conductive surface, which operates as an input device ...." '509 patent 1 :16-21. Similarly, the "Summary of the Invention" section of the specification identifies "the novel arrangement of the present invention" with reference to the fact that "multiple displays and function symbols are controlled by the stylus and conductive surface." '509 patent 4 :35-39.

Although the limitations in the AFC Defendants' proposed construction are found in the specification, limitations in the specification may be imported into a claim only in rare circumstances. Intel Corp. v. U.S. Intern. Trade Com'n, 946 F.2d 821, 836 (Fed.Cir.1991) ("Where a specification does not *require* a limitation, that limitation should not be read from the specification into the claims.") (emphasis in original, citations omitted). In this case, the AFC Defendants' construction of the term "image processing system" includes limitations that are explicitly recited in other claims. This fact counsels against reading these limitations into claims in which they are not specifically recited.

Claim 38 of the '509 patent, for example, recites the apparatus of claim 35 (including the "image processing system") with "at least first and second displays." '509 patent 19 :23-24. Defendants' proposed construction incorporates the requirement of multiple displays into the term "image processing system" thereby rendering claim 38 superfluous. Likewise, claim 42 of the '509 patent recites a "sensing system having a transparent surface" responsive to a stylus. This claim would also be superfluous if Defendants' construction of "image processing system"-which includes "a single transparent energized conductive surface" and "a stylus operative via the conductive surface"-were adopted. The doctrine of claim differentiation counsels against this result.

The final limitation found in the AFC Defendants' construction of "image processing center" is the inclusion of "integrated real time full duplex communication capability" into the term. As described in the specification, this capability "allows dispersed users to edit a single document as a simultaneous group activity." '509 patent 2 :11-16. This functional limitation is sufficiently described in claim 35 that it need not be incorporated into the term "image processing center." *See* '509 patent 18 :68-19 :9.

Quanta concurs in the AFC Defendants' construction of the term "image processing system." In addition to the claim language proposed by the AFC Defendants, Quanta also contends that *an* "image processing system" should be construed to exclude "video terminals." This proposed construction is based on a single sentence in the prosecution history in which the patentee apparently distinguished the image processing system from prior art video terminals. According to Quanta, the applicant for the '509 patent, in response to an examiner's rejection stated, "Switching video signals around a LAN to various 'video terminals,' for example, would appear to suggest little or nothing about capturing video images that may be stored in common workplace memory of. various workstations for simultaneous viewing/editing, etc...." Quanta has not directed the Court to the portion of the prosecution history in which this quotation is located. Consequently, the Court is unable to determine if the patentee explicitly disclaimed video terminals from the construction of "image processing system."

In sum, because Defendants improperly import limitations from the specification into the claim, the Court rejects their construction of the term "image processing system." The Court adopts LGE's broad construction of the term as "any device, such as a notebook computer, desktop computer, or server that is capable of displaying images from files, such as word processing documents, spread sheets, bit maps and other file types from which images can be generated."

2. "display"

LGE contends that "display" should be construed consistent with its established meaning to one skilled in the arts. Specifically, LGE contends that "display" in the '509 patent refers to "a device capable of displaying image information such as a CRT monitor or LCD display." The AFC Defendants argue "display" as used in the '509 patent has a specialized meaning as "one of multiple purpose-optimized windowing-less displays that is menu-less."

As was the case with respect to the AFC Defendants construction of "image processing system," several of the limitations they have incorporated from the specification are explicitly recited in subsequent dependent claims in the patent. Specifically, while claim 35 discloses a "display for displaying at least one image," dependant claim 36 discloses "the apparatus of claim 35 wherein the image processing system comprises at least first and second displays ...." '509 patent 19 :21-25. The "first and second displays" disclosed in claim 38 are, moreover, designated for graphic images and textual information respectively. *Id*. 19:25-26. Consequently, "multiple purpose optimized" displays are covered by dependant claim 38 and should not be read into the term "display" in claim 35. Rather, the portions of the specification relied on by the AFC Defendants in support of their "purpose-optimized" construction are more properly read in reference to disclosure of claim 38. *See* '509 patent 5 :44-48 ("[O]ne display is designed for high resolution black and white capabilities. This display is particularly suitable as a display for documents, other forms of text and other images that require a high degree of legibility....").

However, the AFC Defendants' other proposed limitations on this claim term-that the display be "menu-less" and "windowing-less"-are not encompassed by any claims dependant on claim 35. Consequently, the doctrine of claim differentiation is inapplicable in determining if these limitation are encompassed by the term "display" in claim 35.

Nevertheless, the specification does not support incorporating these limitations into the claim. In fact, the specification nowhere states that the "display" in the invention is either "menu-less" or "windowing-less." It does state that "frequently used menu and system control functions" are silkscreened on the work surface. '509 patent 4 :66-5 :10. These "frequently used" functions, therefore, need not be included in a screen-displayed menu. However, this reference cannot, support the AFC Defendants' contention that the "display" disclosed in claim 35 of the '509 patent must be "menu-less." Similarly, in support of their contention that "display" must be construed as "windowing-less, the AFC Defendants rely on the following excerpt from the specification.

The present invention can also simultaneously display directory listings (on the displays) eliminating the need for windowing and for printed directory listings.

'509 patent 5 :21-25. Although the specification states that the need for windowing is eliminated, it does not state that the "display" must be window-less. Consequently, this reference is too vague to support the AFC Defendants' construction of "display." The Court therefore adopts LGE's construction of display in its

entirety.

3. "control unit for ..."

Quanta contends that this term is a means-plus-function claim term that must be construed pursuant to 35 U.S.C. s. 112 para. 6. Because the term does not include the word "means," the Court presumes that s. 112 para. 6 does not apply. However, that presumption may be rebutted if the term "relies on functional terms rather than structure or material to describe performance of the claimed function." Micro Chem., Inc. v. Great Plains Chem. Co., 194 F.3d 1250, 1257 (Fed.Cir.1999).

Claim 35 recites a "control unit for controlling the communications unit, wherein the control unit comprises a CPU and a partitioned memory system...." Quanta argues that despite the absence of the words "*means for,*" this term is expressed in functional language and fails to recite sufficient structure or materials to perform the function.

LGE contends that by using the term "unit," the claim recites sufficient structure to support the presumption against construing this term under s. 112 para. 6. LGE relies on Personalized Media Communications, LLC v. International Trade Com'n, 161 F.3d 696, 704-705 (Fed.Cir.1998) where the Federal Circuit held that the use of the terra "detector" provided sufficient structure to avoid construction under s. 112 para. 6. However, in *Personalized Media,* the court noted that the term detector was "not a generic structural term such as 'means,' 'element,' or 'device.' " 161 F.3d at 705. Rather, detector "had a well-known meaning to those of skill in the electrical arts connotative of structure.... Even though the term 'detector' does not specifically evoke a particular structure, it does convey to one knowledgeable in the art a variety of structures known as 'detectors.' " *Id*. The term "unit," however, is a generic structural term more akin to "device." LGE relies on the Institute of Electrical and Electronics Engineers (IEEE) dictionary to contend that "control unit" has a well-known meaning to those skilled in the art. According to LGE, the IEEE defines "control unit" as

the parts of a computer that effect the retrieval of instructions in proper sequence, the interpretation of each instruction, and the application of the proper signals to the arithmetic unit and other parts in accordance with this interpretation.

JCC, Tab F at 24. This definition simply replaces the generic structural term "unit" with the equally generic structural term "parts." Consequently, because the Court concludes that the term "control unit for" is expressed in functional terms without recitation in the claim of sufficient structure for performing that function, the term should be construed as a means-plus-function claim term.

The Court adopts Quanta's construction of "control unit for ..." in claim 35 of the '509 patent. "Control unit for ..." is "control unit 58A/58B for controlling the communications unit."

4. "second image processing system coupled to the network may access the common memory of the image processing system" and "not capable of accessing the personal memory"

The parties dispute the meaning of the word "access" as used in these claim terms. LGE argues that "access" should be given its dictionary meaning of "make use of." Defendants, however, contend that in the context of the '509 patent, "access" means "view, control, edit and alter the contents of." Under LGE's construction, two image processing systems connected over a network would read on this claim term if the second image processing system was able to view an image stored in the common memory of the first image processing system. Defendants' construction would require that a user at the second image processing system be able to

alter the contents of the document in the common memory of its counterpart connected to the network.

LGE, arguing that the term is commonplace, does not rely on any intrinsic evidence in support of its construction. Defendants emphasize various portions of the specification and prosecution history to justify the their particular meaning of the term "access."

Under "Summary of the Invention," the specification states:

Two or more systems can link to allow fully-interactive real time distributed conferencing and editing wherein dispersed users can work cooperatively on images viewed by all of them. For example, users at various locations can interact with and simultaneously view the same images, while cooperatively manipulating the image with changes to the image made at one workstation instantaneously viewed by the users *at* all workstations.

'509 patent 6 :40-48. The invention's remote editing function is further described in the "Detailed Description of the Preferred Embodiment," which states:

in accordance with the present invention, the image processing systems [ ] are controlled in a manner to be able to access (control, alter the contents of, etc.) the common memory [ ] of both image processing systems and in a manner so as to be able to access only its respective personal memory and not the personal memory of the other image processing systems."

'509 patent 11 :5-12.

Defendants also note that during prosecution of the patent, the applicant distinguished a prior art reference on the grounds that the prior art did not teach "common/personal memory space for use in simultaneous viewing/editing of documents." FH509 at LGE002514.

The specification and prosecution history are consistent with the purported purpose of the invention as described by LGE. LGE notes in describing the technology at issue here that "the image stored in common memory can be edited by all users" on the network. Declaration of Alan Jay Smith (Smith Dec.) para. 41. LGE's broad construction of "access" would not only contradict the requirements detailed in the specification and prosecution history, but also undermine a fundamental purpose of the patent. Therefore, the Court agrees with Defendants that "second image processing system coupled to the network may access the common memory of the image processing system" means "the second image processing system coupled to the network may view, edit or alter the contents of data stored in the common memory." "Not capable of accessing the personal memory" correspondingly means "not capable of viewing, editing or altering the contents of data stored in personal memory." FN6

III. Motion to Preclude New claim Constructions

LGE moves to strike many of the proposed claim constructions offered in the AFC Defendants' "Joint Memorandum Re: Claim Construction" and in Quanta's "Responsive Claim Construction Brief." LGE argues that the constructions proposed by Defendants in these briefs substantively differ from the constructions detailed in the joint claim construction brief. LGE argues that the Court should strike the revised constructions because the revisions were made in violation of the Patent Local Rules and prejudiced LGE.

LGE's motion is denied (Docket # 203). The Court adopted LGE's or Quanta's JCC constructions for the following terms: node in the '733 patent; system bus in the '379 patent; requesting agent, system bus, and memory control apparatus in the " *GAS* patent; bus monitor means, data unit transferred, and a hold signal in the '641 patent; second image processing system ..., display, and image processing system in the '509 patent; and node, second adjacent node, counting a number of accesses .... and predetermined number of accesses ... in the '419 patent. LGE's motion to preclude constructions of these terms offered by the AFC Defendants is denied as moot.

The remaining constructions by the AFC Defendants that LGE moves to strike were not substantively changed from the constructions offered by the AFC Defendants in the JCC or were fairly encompassed by the constructions offered by co-Defendant Quanta in the JCC. In either case, LCE suffered no prejudice from the revised constructions in the AFC Defendants' memorandum.

LGE's motion to strike the revised constructions in Quanta's claim construction brief is denied for the same reasons. LGE objects to seven constructions proffered by Quanta in its claim construction memorandum. Two cf these objections (to the phrases "a system bus" and "a predetermined number of write requests") are moot. The remaining six objections are not well-taken because the constructions proffered in Quanta's responsive claim construction brief do not substantively differ from those presented in the JCC.

IV. Motion to Strike

The AFC Defendants object to and move to strike the Declaration of Alan Jay Smith (Smith Declaration) on the grounds that the submission of this declaration violated the Court's order with respect to page limits for claim construction briefs. The Court denies the AFC Defendants' motion to strike (Docket # 176). Quanta's alternative request to consider the Declaration of Jean-Luc Gaudiot is granted (Docket # 187).

CONCLUSION

For the reasons stated, the Court denies LGE's motion to preclude (Docket # 203), denies the AFC Defendants' motion to strike (Docket # 176), grants Quanta's request to consider the Declaration of Jean-Luc Gaudiot (Docket # 187) and construes the disputed terms and phrases in the foregoing manner.

FN1. Asustek, First International, and Compal are referred to collectively as the AFC Defendants throughout this order.

FN2. The AFC Defendants also argue that "cache memory" should be construed only to mean a "cache memory operating as a write-back cache when data is not shared and operating as a write through cache when data is shared." This limitation, however, is purely functional. Because this term is not a means-plus-function term, the Court declines to incorporate this functional language into the claim term.

FN3. LGE argues that the '641 patent initially encompassed two distinct patents and that one of those patents was abandoned during prosecution. LGE contends that the limitation on the use of valid/invalid bits was relevant to the abandoned patent. However, the specification is intended to enable one skilled in the art to practice the patent. The specification, therefore, must describe the claimed invention. As noted above, the specification makes clear that the "cache memory" claimed in the '641 patent does not use valid/invalid bits.

FN4. The term "transferred from" encompasses the phrase "being read from" used in claim 5.

FN5. LGE construes this phrase to mean "a data unit different than a corresponding data unit in main memory." The Court has, in substance, adopted this construction. However, the term "corresponding" in LGE's construction is unclear. Based on the specification, "corresponding" data units in LGE's construction appears to refer to data units with the same address, but located in different memory components.

FN6. Defendants contend that "access" also includes the ability to "control." In this context, "control" is vague and Defendants suggest that "control" is synonymous with the ability to "edit" or "alter the contents of" an image stored in common memory. The inclusion of the word "control" would add nothing to the construction established. Therefore, the word "control" need not be incorporated into the construction of this term.

N.D.Cal.,2002.
LG Electronics, Inc. v. Asustek Computer, Inc.