United States District Court,
N.D. California.

SYNOPSYS, INC,
Plaintiff and Counter-Defendant.
v.
NASSDA CORPORATION,
Defendant and Counter-Claimant.

No. C 01-2519 SI

Aug. 13, 2002.

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CLAIM CONSTRUCTION ORDER

SUSAN ILLSTON**, District Judge.**

On July 10, 2002, the Court heard argument from the parties regarding claim construction for U.S. Patent No. 5,878,053. Having considered the arguments of counsel and the papers submitted, the Court hereby construes the disputed patent terms as set out below.

BACKGROUND

Plaintiff Synopsys, Inc. ("Synopsys"), alleges infringement of U.S. Patent No. 5,878,053 ("the '053 patent") by defendant Nassda Corporation ("Nassda"). The '053 patent teaches a method for analyzing a semiconductor chip design for determining potential voltage drop and electromigration problems. '053 patent Abstract. The '053 patent has 22 claims, including three independent claims and nineteen dependent claims. At issue here is the meaning of claims 1-9 and 16 of the patent.

LEGAL STANDARD

Proper construction of patent claims is to be made by the trial court as a matter of law, with the claims being construed as understood by one skilled in the art. *See Markman v. Westview Instruments, Inc.,* 52 F.3 d 967, 979, 985 (Fed.Cir.1995) (en banc), *aff'd,* 517 U.S. 370, 116 S.Ct. 1384, 134 L.Ed.2d 577 (1996). In determining the proper construction of a claim, the Court begins with the intrinsic evidence of record, consisting of the claim language, the patent specification, and, if in evidence, the prosecution history. *See id.* (citing Unique Concepts, Inc. v. Brown, 939 F.2d 1558, 1561 (Fed.Cir.1991)).

"The appropriate starting point ... is always with the language of the asserted claim itself." Comark Communications, Inc. v. Harris Corp., 156 F.3d 1182, 1186 (Fed.Cir.1998). "[T]he language of the claim frames and ultimately resolves all issues of claim interpretation." Abtox, Inc. v. Exitron Corp., 122 F.3d 1019, 1023 (Fed.Cir.1997). However, claims are always read in view of the written description. *See* Vitronics Corp. v. Conceptronic, Inc., 90 F.3d 1576, 1582 (Fed.Cir.1996). A district court may look to the specification to aid its interpretation of a term already in the claim. *See* Wang Laboratories v. America Online, Inc., 197 F.3d 1377, 1382 (Fed.Cir.1999); York Prods., Inc. v. Cent. Tractor Farm & Family Ctr., 99 F.3d 1568, 1572 (Fed.Cir.1996) (intrinsic evidence may provide context and clarification about meaning of claim terms). "Such intrinsic evidence is the most significant source of the legally operative meaning of the disputed claim language." Vitronics, 90 F.3d at 1582; Renishaw PLC v. Marposs Societa'per Azioni, 158 F.3d 1243, 1250 (Fed.Cir.1998) ("a common meaning, such as one expressed in a relevant dictionary, that flies in the face of the patent disclosure is undeserving of fealty.").

In the absence of an express intent to impart a novel meaning to claim terms, an inventor's claim terms take on their ordinary meaning. Teleflex, Inc. v. Ficosa North America Corp., 299 F.3d 1313, 2002 WL 1358720 (Fed.Cir. June 21, 2002). There is a "heavy presumption" that a claim term carries its ordinary and customary meaning. CCS Fitness, Inc. v. Brunswick Corp., 288 F.3d 1359, 1366 (Fed.Cir.2002). "[A] court must presume that the terms in the claim mean what they say, and, unless otherwise compelled, give full effect to the ordinary and accustomed meaning of the claim terms." Johnson Worldwide Assoc., Inc. v. Zebco Corp., 175 F.3d 985, 989 (Fed.Cir.1999).

The Federal Circuit has described a number of circumstances in which straying from the ordinary and accustomed meaning of a term is appropriate. First, a patentee may choose to be his or her own lexicographer by clearly setting forth an explicit definition for a claim term. *See* In re Paulsen, 30 F.3d 1475, 1480 (Fed.Cir.1994). Where this is the case, the written description must describe "with reasonable clarity, deliberateness, and precision" the proposed definition for it to be adopted. *Id*. Second, the term or terms chosen by the patentee may "so deprive the claim of clarity that there is no means by which the scope of the claim may be ascertained from the language used." Johnson Worldwide Assoc., 175 F.3d at 990 (citing Eastman Kodak Co. v. Goodyear Tire & Rubber Co., 114 F.3d 1547, 1554 (Fed.Cir.1997)). Further, the patentee may demonstrate an intent to deviate from the ordinary and accustomed meaning of a claim term by including in the specification "expressions of manifest exclusion or restriction, representing a clear disavowal of claim scope." Teleflex, 299 F.3d 1313, 2002 WL 1358720.

In order to overcome the heavy presumption in favor of the ordinary meaning of claim language, "a party wishing to use statements in the written description to confine or otherwise affect a patent's scope must, at the very least, point to a term or terms in the claim with which to draw in those statements." Renishaw, 158 F.3d at 1248. Moreover, there must be an express intent by the patentee to impart a novel meaning in order to deviate from the normal meaning of claim language. *Id*. at1249. "This is so because the claims define the scope of the right to exclude; the claim construction inquiry, therefore, begins and ends in all cases with the actual words of the claim." *See Id*. at 1248; Thermalloy, Inc. v. Aavid Eng'g, Inc., 121 F.3d 691, 693 (Fed.Cir.1997) ("[T]hroughout the interpretation process, the focus remains on the meaning of the claim language.").

"That claims are interpreted in light of the specification does not mean that everything expressed in the specification must be read into all the claims." Raytheon Co. v. Roper Corp., 724 F.2d 951, 957 (Fed.Cir.1983). Limitations from a preferred embodiment described in the specification generally should not be read into the claim language. *See* Comark, 156 F.3d at 1187; Intervet America, Inc. v. Kee-Vet

Laboratories, Inc., 887 F.2d 1050, 1053 (Fed.Cir.1989) ("interpreting what is meant by a word in a claim 'is not to be confused with adding an extraneous limitation appearing in the specification, which is improper' "). "No matter how great the temptations of fairness or policy making, courts do not rework claims. They only interpret them." Autogiro Co. of America v. United States, 181 Ct.Cl. 55, 384 F.2d 391, 395-96 (Ct.Cl.1967).

A court may also consider the prosecution history of the patent, if in evidence. *See Markman,* 52 F.3d at 979. The prosecution history limits the interpretation of claim terms so as to exclude any interpretation that was disclaimed during prosecution. *See* Southwall Technologies, Inc. v. Cardinal IG Co., 54 F.3d 1570, 1576 (Fed.Cir.1995).

In most situations, analysis of this intrinsic evidence alone will resolve claim construction disputes. *See* Vitronics, 90 F.3d at 1583. Reliance on extrinsic evidence is unnecessary and improper when the disputed terms can be understood from how they are defined, even implicitly, in the specification or prosecution history. *See* id. at 1584. Judges may rely on extrinsic evidence, however, in the form of technical treatises and dictionaries at any time, "so long as the dictionary definition does not contradict any definition found in or ascertained by a reading of the patent documents." *See id.* at 1485. Thus, "under *Vitronics,* it is entirely appropriate, perhaps even preferable, for a court to consult trustworthy extrinsic evidence to ensure that the claim construction it is tending to from the patent file is not inconsistent with clearly expressed, plainly apposite, and widely held understandings in the pertinent technical field." Pitney Bowes, Inc. v. Hewlett-Packard Co., 182 F.3d 1298, 1309 (Fed.Cir.1999).

DISCUSSION

This case presents an example of the intersection between two familiar claim construction canons. Nassda, arguing for a narrow construction of the '053 patent, urges the Court to read the claim language in light of the specification, which describes an embodiment of the invention. Following this line of reasoning to an extreme, Nassda's proposed construction involves rewriting full claim limitations to include lengthy, detailed descriptions pulled almost verbatim from the specification. Synopsys, on the other hand, contends that the Court may not read limitations from the specification into the claim language and proposes broader constructions of disputed claim limitations. Both parties can, of course, cite to abundant authority from the Federal Circuit in support of their respective positions.

The Court must here navigate between these conflicting guidelines, one of which requires reference to the specification, and the other of which forbids the wholesale importation of limitations from the specification into claim language. The Federal Circuit has explained that neither of these principles should be applied mechanically:

Although precedent offers assorted quotations in support of differing conclusions concerning the scope of the specification, these cases must be viewed in the factual context in which they arose. Whether an invention is fairly claimed more broadly than the "preferred embodiment" in the specification is a question specific to the content of the specification, the context in which the embodiment is described, the prosecution history, and if appropriate the prior art, for claims should be construed, when feasible, to sustain their validity.

Wang Laboratories, 197 F.3d at 1383. *See also* Renishaw, 158 F.3d at 1250 ("A claim construction is persuasive, not because it follows a certain rule, but because it defines terms in the context of the whole

patent.").

Taken as a whole, the problem with Nassda's lengthy proposed construction is that it draws directly from the specification to limit claim terms despite the fact that there is no indication that the patentee intended to limit the meaning of the disputed limitations to the embodiment described therein. Instead of identifying particular words or phrases that require interpretation, Nassda proposes completely rewriting almost every limitation of each disputed claim. As set forth above, the role of the Court is to interpret disputed claim terms; this Court will not rewrite each claim limitation in full to directly reflect the language of the specification. Doing so eliminates the recognized distinction between the claim language and the specification. The Federal Circuit has addressed the same issue:

If everything in the specification were required to be read into the claims, or if structural claims were to be limited to devices operated precisely as a specification-described embodiment is operated, there would be no need for claims. Nor could an applicant, regardless of the prior art, claim more broadly than that embodiment.

SRI Int'l v. Matsushita Elec. Corp., 775 F.2d 1107, 1121 (Fed.Cir.1985) (en banc) (plurality opinion).

Not only is there no indication of an intent on the part of the patentee to import limitations from the specification, but the specification includes two disclaimers explaining that what is being described is a preferred embodiment and is not intended to limit the scope of the claim language. First, the section of the specification titled "Detailed Description" includes the following disclaimer in the opening paragraph:

In the following description, for purposes of explanation, numerous specific details are set forth in order to provide a thorough understanding of the present invention. It will be obvious, however, to one skilled in the art that the present invention may be practiced without these specific details.

'053 patent, 3 :32-34. The same section ends with the following disclaimer:

The foregoing descriptions of the specific embodiments of the present invention have been presented for purposes of illustration and description. They are not intended to be exhaustive or to limit the invention to the precise forms disclosed, and obviously many modifications and variations are possible in light of the above teaching.... It is intended that the scope of the invention be defined by the claims appended hereto and their equivalents.

Id. at 7:29-41.

Nassda's approach also conflicts with another established principle of claim construction. As will be discussed with respect to the disputed limitations of Claim 1, Nassda proposes reading limitations into that claim that are specifically set forth in later dependent claims. In general, limitations stated in dependent claims "should not be read into the independent claim from which they depend...." Karlin Tech. Inc. v. Surgical Dynamics, Inc., 177 F.3d 968, 972 (Fed.Cir.1999); *Comark,* 156 F.2d at 1187. Because Nassda proposes reading most limitations from the specification into Claim 1, any distinction between that claim and the remaining claims of the patent is eviscerated by Nassda's proposed construction.

Nassda argues that Synopsys' claim construction is so overbroad that it includes chip design methods taught at universities worldwide for over 40 years, rendering the patent invalid. Declaration of Laurence W. Nagel,

Ph.D. ("Nagel Decl."), 10:9-10. However, Nassda fails to explain how any prior art in particular is implicated by Synopsys' proposed construction. Synopsys' experts disagree, explaining that their proposed construction does not read on prior art. FN1 Nassda has not here convinced the Court that this vague concern about invalidity warrants adopting their narrow reading of the claim language. The parties contest the meaning of claims 1-9 and 16.

FN1. Although the Court has held that Nassda is barred by the doctrine of assignor estoppel from asserting invalidity in this case, Synopsys has not presented any caselaw for the proposition that the Court can here disregard the principle of claim construction that the Court must construe the patent so as to avoid invalidity.

A. Claim 1

Claim 1 of the '053 patent reads FN2:

FN2. Disputed terms are emphasized.

A method for analyzing a semiconductor chip design, comprising steps of:
dividing the semiconductor chip design into a *plurality* of *blocks;*

performing a *block level verification based on an assumption that full voltage is being supplied to the blocks;*

modeling the blocks according to a resistor and capacitor network;

simplifying the resistor and capacitor network into an equivalent circuit;

determining voltage drops corresponding to the equivalent circuit;

analyzing the blocks with the voltage being supplied to the blocks reduced according to the determined voltage drops.

1. "dividing the semiconductor chip design into a plurality of blocks"

The parties dispute the meaning of the words "plurality" and "blocks" as they are used in the first limitation of Claim 1.

a. "plurality"

Although the word was not mentioned in the prehearing statement, it now appears that the parties dispute the definition of the word "plurality." Synopsys now contends that the word means "one or more." Pl.'s Brf., 3:24. Nassda argues that the word should be interpreted to mean "more than one." Def.'s Brf., 19 n. 31. It goes without saying that a chip cannot be "divided," as foreseen by the first limitation, into *one piece*. Moreover, a "plurality" refers to at least two parts. Accordingly, the Court construes "plurality" as follows:

"Plurality" means more than one.

b. "block"

One of the central disputes between the parties is the appropriate construction of the word "block," as it is used in the first limitation of Claim 1. Synopsys argues that the term is consistently used within the electronic design automation ("EDA") industry to mean a portion or region of the chip design. Pl.'s Brf., 11:26-12:1. Nassda agrees that, in general, "block" has the generic meaning attributed to it by Synopsys, but adds a number of limiting factors to Synopsys' proposed definition, namely that (1) the portion must be of manageable size such that it can fit into a transistor level simulator; (2) the blocks must be functionally identifiable pieces of the circuit; and (3) the blocks exclude a top level power network. Def.'s Brf., 19:13-22:9. The Court will address each of these proposed limitations in turn.

(1) Of Manageable Size

The specification refers to dividing the chip design into several blocks at the top level. '053 patent, 2:35-38; 3:43-46. Nassda does not, however, point to any language in the intrinsic record reflecting a requirement that the blocks be "of manageable size" or sized to fit into a transistor level simulator. One sentence in the specification, in describing a particular embodiment of the invention, describes each block having four million or less transistors. Id. at 3:43-46. This alone, however, does not amount to a clear disavowal of claim scope. Mere inferences drawn from the description of an embodiment of the invention cannot serve to limit claim terms. *See, e.g.,* Constant v. Advanced Micro-Devices, Inc., 848 F.2d 1560, 1571 (Fed.Cir.1988); Renishaw, 158 F.3d at 1249 ("Nor may we ... add a narrowing modifier before an otherwise general term that stands unmodified in a claim.").

(2) Functionally Identifiable

Likewise, nowhere in the language of the claims or the specification is there any indication that the blocks must be functionally identifiable. If anything, Figure 2 of the patent, which illustrates a chip that has been divided into 16 separate blocks, shows the division of a chip based on location, rather than function of the circuit elements. According to the Federal Circuit, "if an apparatus claim recites a general structure (e.g., a noun) without limiting that structure to a specific subset of structures (e.g., with an adjective), we will generally construe the claim to cover all known types of that structure that are supported by the patent disclosure." *Id. See also* Specialty Composites v. Cabot Corp., 845 F.2d 981, 987 (Fed.Cir.1988) ("Where a specification does not *require* a limitation, that limitation should not be read from the specification into the claims") (italics in original).

Moreover, Synopsys' experts, Martin G. Walker, Ph.D. ("Dr.Walker") and Lawrence Pileggi, Ph.D. ("Dr.Pileggi"), explain that division into functionally identifiable blocks is unnecessary to perform the steps described in the claim language. Reply Declaration of Martin G. Walker, Ph.D. ("Walker Reply Decl."), 11:5-14; Reply Declaration of Lawrence Pileggi, Ph.D. ("Pileggi Reply Decl."), 5:13-23. According to Dr. Walker, if the patentee had intended that the blocks be functionally identifiable, the blocks would have been referred to as "functional blocks," a term he maintains is well known to those of ordinary skill in the art. Walker Reply Decl., 10:5-8.

(3) Top Level Power Network

With respect to Nassda's proposed exclusion of the top level power network from the blocks, Nassda does not direct the Court to any unambiguous language in the claims or specification indicating that the top level

power network must be excluded from the dividing process described in the first limitation of Claim 1. As set forth above, before the Court reads in such a significant limitation from the specification, the written description must describe "with reasonable clarity, deliberateness, and precision" the proposed definition. In re Paulsen, 30 F.3d at 1480.

The claim language itself gives no indication that the top level power network must be excluded from the blocks in Claim 1. Claim 1 instead requires simply that the chip design be divided into blocks. '053 patent, 2 :35-38. A top level power network is one part of a chip design. Further, Dr. Walker explains that the term "block," as it is used in the EDA industry, is commonly understood to encompass the top level power network. Declaration of Martin G. Walker ("Walker Decl."), 8:16-19.FN3 Were it true that such an integral portion of the chip is necessarily excluded from the blocks in Claim 1, one would assume that the patentee would have more clearly articulated the requirement.

FN3. Dr. Pileggi explains that many chips are designed without a top level power network. Declaration of Lawrence Pileggi, Ph. D. ("Pileggi Decl."), 10:10-11.

Moreover, the passages and figures from the specification cited by Nassda do not support its argument that the word "blocks" should be specially interpreted to exclude the top level power network. Nassda's expert, Laurence W. Nagel, Ph.D. ("Dr.Nagel") cites two portions of the specification in support of his conclusion that "the blocks do not include the top level power net." Declaration of Laurence W. Nagel, Ph.D. ("Nagel Decl."), 7:22-23. The first cited section provides:

In the block level verification stage, rather than analyzing the entire chip at once, the new chip design is divided into a number of blocks at the top level. The layout of each block matches that of the schematic. The power connection locations of each block are identified in the chip layout.

'053 patent, 2 :35-40. The second cited portion reads: "In the first stage 101, the semiconductor chip is broken into several top level blocks, with each block having four million or less transistors." Id. at 3:43-46. Neither of these portions of the specification mandates that the blocks exclude a top level power network. If anything, dividing the chip design into "a number of blocks at the top level" would appear to require inclusion of the top level power network within the blocks. Nassda also points to a portion of the summary of the invention section which explains that "[t]he actual voltage drops and current waveforms through the top-level interconnect wires are then determined in the full chip RC network simulation stage based on the functionally equivalent, but reduced RC networks and the recorded current models." Id. at 2:49-54. Again, this portion of the specification does not require that the top level power network be excluded from the blocks in Claim 1. Both the claims and the specification are clear-the chip design is to be divided into a plurality of blocks. Nassda cannot cite to any portion of the intrinsic record mandating that the top level power network be excluded from the blocks in Claim 1.

In describing Figures 8 and 9, the specification does discuss performing RC extraction and reduction for the "top level composite mode," and indicates that the modeled blocks are not involved in this process. '053 patent, 5 :36-6 :21. However, the Court is not convinced that this portion of the specification supports Nassda's argument that the top level power network *must* be excluded from the blocks as they are described in Claim 1. Even assuming that these portions describe a separate analysis of the top level power network, this portion of the specification need not be read into Claim 1 in particular. Nassda's proposed wording regarding the top level power network impermissibly reads in a limitation, assuming any such limitation

exists, from the specification. Moreover, some of the portions of the specification relied upon by Nassda describe "top level simulation," which is taught in dependent Claim 6-not in Claim 1. '053 patent, 6 :5-21.

Therefore, the Court rejects the limiting factors proposed by Nassda and construes "block" as follows:

"Block" means a portion or region of the chip design.

2. "performing a block level verification based on an assumption that full voltage is being supplied to the blocks"

a. "block level verification"

Synopsys argues that this term is clear on its face, but that "verification" means "confirmation that one or more predetermined parameters, requirements, or specifications are met," and that "block level verification" means "verification at the level of the blocks." Pl.'s Brf., 14:12-15:2. Nassda, on the other hand, proposes a much narrower construction. First, Nassda argues that "block level verification" should be construed as "a simulation of voltages and current densities for each block, using extracted resistance and capacitance values for interconnect wires within the block." Def.'s Brf., 22:12-19. Nassda then proposes including a lengthy description of steps for carrying out block level verification which is drawn from the section of the specification which describes "in detail, the steps for performing the block level verification." '053 patent, 3 :5-6.

(1) Simulation

Relying upon the description of a preferred embodiment in the specification, Nassda contends that block level verification requires a simulation of each of the blocks. However, neither the claim language nor the specification limits the process of verification to "simulating voltages and current densities for each block." First, the language of Claim 1 does not refer to a simulation, instead using the word "verification." "Verification" is not synonymous with "simulation"-while the word encompasses simulation, it also covers a number of other operations that may be performed on a chip. As explained by Dr. Walker, various parameters of a chip design can be verified, including voltage, current, power, timing, and layout. Walker Decl., 15:16-17.FN4 Nowhere in the specification is there any clear indication that verification is intended to be limited to other than the ordinary meaning of the term. In fact, the specification, in describing one embodiment, includes a layout versus schematic ("LVS") check in describing this second step of Claim 1. ' 053 patent, 4 :8-11. Nassda acknowledged at oral argument that LVS checking does not involve simulating voltages and current densities for each block. Nassda's proposed construction, limiting the verification step to a simulation, would not allow for this and other types of verification envisioned by the patentee. Moreover, it is particularly difficult to argue that "verification" and "simulation" are synonymous because the two words are not used interchangeably in the claim language or the specification.

FN4. Nassda's own documents interpret the word "verification" to include more than simply "simulating voltages and current densities ." For example, a Nassda presentation describing "HSIM-based verification methodology," includes "leakage checks." Walker Decl, Ex. I. A Nassda white paper describes "physical layout verification." Id. at Ex. F.

The Court also rejects Nassda's argument that block level verification necessarily involves "using extracted resistance and capacitance values for interconnect wires within the block." Dependent Claim 4 describes this

operation. Limitations stated in dependent claims "should not be read into the independent claim from which they depend...." Karlin Tech., 177 F.3d at 972. Again, the specification explicitly refers to at least one operation, LVS checking, which does not require use of extracted resistance and capacitance values.

(2) Nassda's Proposed Steps from Specification

Further, the Court will not add the eleven lengthy steps for performing block level verification drawn from the specification by Nassda. The Supreme Court has explained that: "[t]he difficulty is that if we once begin to include limitations not mentioned in the claim in order to limit such claim ..., we should never know where to stop." McCarty v. Lehigh Val R.R., 160 U.S. 110, 116, 16 S.Ct. 240, 40 L.Ed. 358 (1895).

It would be clear to one of ordinary skill in the art that the embodiment described in the specification is simply an example and is not intended to limit the scope of the claim language to those steps alone. Moreover, the portions of the specification relied upon by Nassda include a number of steps that are explicitly referenced in the later dependent claims. Including this detailed analysis would eliminate any distinction between the claims. *See* Beachcombers, Int'l, Inc. v. WildeWood Creative Products, Inc., 31 F.3d 1154, 1161 (Fed.Cir.1994) (an interpretation of a claim that would render another claim in the patent "superfluous" is "presumptively unreasonable"); United States v. Telectronics, Inc., 857 F.2d 778 (Fed.Cir.1988), *cert. denied,* 490 U.S. 1046, 109 S.Ct. 1954, 104 L.Ed.2d 423 (1989) (claim differentiation counsels against construing claim 1 so that its limitations are the same as dependent claim 2).

Therefore, the Court construes "block level verification" as follows:

"Block level verification" means confirmation at the level of the blocks that one or more predetermined parameters, requirements, or specifications are met.

b. "an assumption that full voltage is being supplied to the blocks"

Synopsys argues that this phrase is clear on its face and need not be interpreted. Pl.'s Brf., 16:4-8. Nassda adds the word "supply" and a requirement that a voltage source be present in its proposed construction. Nassda's proposed construction is as follows: "an assumption that full supply voltage from a voltage source (such as a battery) is supplied to the blocks." Def.'s Brf., 25:7-15. Nassda provides little support from the specification for its position that these limitations must be added to the claim language. In fact, neither of the two portions of the patent relied upon by Nassda includes any reference to "full supply voltage" or a voltage source. '053 patent Abstract; 2:40-43.

Accordingly, the Court finds that the phrase "an assumption that full voltage is being supplied to the blocks" is clear on its face and does not require any interpretation.

3. "modeling the blocks according to a resistor and capacitor network"

Synopsys contends that "modeling" should be construed as "making or constructing a model," that "resistor and capacitor network" should be construed as "a collection of interconnected resistors and capacitors," and that "blocks" should receive the same construction as set forth above. Pl.'s Brf., 17:9-19. Again, Nassda proposes a construction that draws at length from the specification, describing a detailed four-step process for modeling the blocks.

Synopsys maintains that each of the terms used in this limitation would be readily understandable to one of

ordinary skill in the art, and that there is no sign in the specification that the terms were intended to be restricted to the narrow construction proposed by Nassda. The Court agrees. Nassda's proposed construction impermissibly draws limitations from the specification where there is no express intent to do so in the patent language. Again, the Federal Circuit recently explained that:

claim terms take on their ordinary and accustomed meanings unless the patentee demonstrated an intent to deviate from the ordinary and accustomed meaning of a claim term by redefining the term or by characterizing the invention in the intrinsic record using words or expressions of manifest exclusion or restriction, representing a clear disavowal of claim scope.

Teleflex, 299 F.3d 1313, 2002 WL 1358720 (although the specification described only one embodiment of a clip, which had a single pair of legs, no clear statements of scope limited the term to having a single pair of legs). *See also* Kegel Co., Inc. v. AMF Bowling, Inc., 127 F.3d 1420, 1427 (Fed.Cir.1997) ("Without an express intent to impart a novel meaning to a claim term, the term takes on its ordinary meaning."). Interpreting what is meant by a word in a claim "is not to be confused with adding an extraneous limitation appearing in the specification, which is improper." E.I. Dupont De Nemours & Co. v. Phillips Petroleum Co., 849 F.2d 1430, 1433 (Fed.Cir.1988). Further, Nassda's detailed list of steps includes steps that are explicitly described in dependent Claim 4 and independent Claim 9, violating the principle of claim differentiation.

For the foregoing reasons, the Court construes the disputed terms as follows:

"Modeling" means making or constructing a model. "Resistor and capacitor network" means a collection of interconnected resistors and capacitors.

4. "simplifying the resistor and capacitor network into an equivalent circuit"

Synopsys argues that the Court need only provide the commonly accepted definitions of the words "simplifying," "resistor and capacitor network," and "equivalent circuit." Pl.'s Brf., 18:7-16. Here again, instead of identifying specific words it believes require construction, Nassda proposes taking the unusual step of construing the entire phrase to include a multitude of steps drawn almost verbatim from the embodiment of the claimed invention described in the specification. Def.'s Brf., 27:18-25. As seen before, this proposed construction is inappropriate because, among other things, it adds extraneous limitations from the specification. Moreover, the portion of the specification from which Nassda draws its proposed construction refers to a "full chip netlist preparation stage." There is no indication in the language of the specification that this stage is intended to correspond specifically to "simplifying the resistor and capacitor network into an equivalent circuit," as described in Claim 1. Further, RC extraction, which Nassda argues should be included in the construction of this limitation, is specifically described in dependent Claim 4.

The Court adopts the following construction of "simplifying the resistor and capacitor network into an equivalent circuit":

"Simplifying" means reducing in complexity. "Equivalent circuit" means a circuit that has similar properties as another circuit. "Resistor and capacitor network" is defined in the same manner as it was in the previous limitation.

5. "determining voltage drops corresponding to the equivalent circuit"

Synopsys maintains that these terms are easily understandable by those of ordinary skill in the art and do not require significant construction. Pl.'s Brf., 19:3-11. Nassda again argues that this step requires a simulation and proposes an overwhelmingly lengthy construction drawn from the steps described in the specification. Def.'s Brf., 28:18-27. For the reasons set forth above, the Court is unwilling to include the multiple steps proposed by Nassda.

However, the Court agrees with Nassda on one issue with respect to this limitation. Close review of the specification reveals that the "determining" step necessarily includes a simulation. Each time this step is described in the specification, it is identified as involving a simulation. This is true even where the specification describes the invention at its most basic level. For example, Figure 1, a flowchart "describing the basic stages of the present invention," refers to this step as "Full Chip Network Simulation." '053 patent, 3:1-2; Figure 1. The background section explains that after the invention extracts an accurate, yet reduced RC model of the power network and current characteristics, it "simulates the entire power network of the design with those derived models...." Id. at 2:16-21. In the summary of the invention section, the patentee describes this stage again as the "full chip network simulation stage." Id. at 2:49-54. *See also* id. at 3:56-59 ("Thereupon, a full chip RC network simulation can be performed in stage 103. Based on this simulation, the voltage drops corresponding to each of the blocks can now be more easily determined."). These repeated references to simulation evidence an express intent on the part of the patentee to require that a simulation occur in the "determining" step. *See* Intellicall, Inc. v. Phonometrics, Inc., 952 F.2d 1384, 1388 (Fed.Cir.1992) (when the meaning of a term is sufficiently clear in the patent specification, that meaning shall apply).

The Court adopts the following construction:

"determining voltage drops corresponding to the equivalent circuit" means ascertaining, through a simulation, the difference in voltage corresponding to the equivalent circuit. Equivalent circuit is here defined in the same manner as in the fourth limitation.

6. "analyzing the blocks with the voltage being supplied to the blocks reduced according to the determined voltage drops"

Synopsys contends that the language of this limitation is clear to one of ordinary skill in the art and needs no interpretation. Nassda proposes the following language: "Re-simulate the blocks using the calculated voltage drop and current information obtained during the top level simulation, instead of assuming full voltage, to determine whether there are potential voltage, current, thermal, or electromigration problems with the design." Again, Nassda then proposes a lengthy description of the steps required in this "re-simulation," all of which are pulled from the specification. Def.'s Brf., 30:3-26.

According to Synopsys, "analyzing" and "re-simulation" are different concepts. Walker Decl., 28:8-9. The Court agrees that the patent does not treat "analyzing" and "simulating" as synonymous terms. Moreover, in contrast to the "determining" step, there exists no clear disavowal of claim scope such that limiting this step to "re-simulation" would be appropriate.

The Court adopts the following construction of step six:

"Analyzing" means examining methodically. "Block" and "voltage drops" are defined in the same manner as in the previous limitations.

B. Claim 2

Claim 2 is the first of several dependent claims requiring construction. The claim reads:

The method of claim 1, further comprising the steps of:

identifying probe points corresponding to locations where power is supplied to the blocks; obtaining test vectors;

driving the blocks according to the test vectors;

capturing currents flowing through the probe points.

1. "identifying probe points corresponding to locations where power is supplied to the blocks"

Synopsys contends that, if anything, only "probe points" and "power" need to be interpreted here. Nassda, again without identifying particular words that require interpretation, proposes rewording the limitation to read: "during the block level verification, for each block, identify probe points, which correspond to the block's power connection points."

The Court agrees with Nassda that the specification explains that "[a] probe point corresponds to the physical location ... at which the power is supplied to the block." '053 patent, 4 :14-16. This definition, however, is included in the claim language itself and need not be integrated into the Court's construction of that language. Nassda also proposes adding that this step occurs during block level verification. To support this interpretation, Nassda relies upon a section of the specification which explains that "the probe points corresponding to each of the power connection points are generated in step 305." Id. at 4:12-14. Although the specification does, in describing block level verification in an embodiment, appear to be referring to the operation described in the first limitation of Claim 2, there is no indication that "identifying probe points" is confined to the block verification stage. Indeed, Figure 8, which is not associated with block level verification, describes "assigning probe_points for power connection points to the blocks." Id. at 5:39-40.

The Court adopts the following construction of "identifying probe points corresponding to locations where power is supplied to the blocks":

"Probe points" means nodes at which voltage and/or current can be inspected. "Power" means electrical energy supplied to a circuit.

2. "obtaining test vectors"

The parties agree that "test vector" means a stimulus pattern containing electrical test information that is applied to a design. In light of this agreed definition, Synopsys argues that this term is clear on its face. Nassda proposes the following construction: "During the block level verification, obtain test vectors, which contain electrical test information to be used as inputs in simulating the blocks." The Court agrees with Synopsys that no further interpretation of the limitation is necessary. Nassda does not direct the Court to any language in the specification that would mandate the additional language it proposes. Nassda's proposed construction merely anticipates the next limitation of Claim 2.

Accordingly, the Court finds that, beyond the agreed definition of "test vectors," this limitation requires no further interpretation.

3. "driving the blocks according to the test vectors"

Synopsys argues that, because the words "blocks" and "test vectors" have already been defined, the Court should do no more than provide a definition of the word "driving." Nassda proposes the following construction: "During the block level verification, simulate the blocks by using the test vectors as inputs." Although the specification does indicate that "[o]nce the voltages and currents are determined, an approximate simulation of voltage drop and electromigration analysis can be created at step 307," which takes place during the block verification stage, this language does not represent "a clear disavowal of claim scope." '053 patent, 4 :31-33. The cited language only indicates that an "approximate simulation" "can" be created during the block verification stage. There is no clear requirement that this step must take place during block level verification or that a simulation must take place during this stage.

Accordingly, the Court adopts the following construction:

"Driving" means directing the operation of.

4. "capturing currents flowing through the probe points"

The parties agree that "capturing" means recording. Synopsys maintains that no further construction of this limitation is necessary. Again, Nassda simply proposes rewriting the entire claim limitation. Nassda proposes the following construction: "During the block level verification, for each block, capture, or record, the values of the current at the power connection points at various times during the simulation." The Court is not convinced that this operation must occur during block level verification, or that it must occur "for each block," as would be required under Nassda's proposed construction.

The Court finds that, aside from the agreed interpretation of "capturing" to mean recording, there is no need for any further interpretation of this limitation.

C. Claim 3

Claim 3 reads as follows:

The method of claim 1, further comprising the step of *generating current waveforms as a function of time for one of the blocks*.

The parties agree that "current waveforms as a function of time" means a "collection of values of the electrical current recorded over time." Nassda's proposed construction would add a requirement that this step take place during block level verification. Again, the Court is not convinced that the specification manifests an intent to limit this step to the block level verification stage.

In light of the agreed interpretation of "current waveforms as a function of time," the Court finds that there is no need to further interpret the limitation.

D. Claim 4

Claim 4 reads as follows:

The method of claim 1, further comprising the steps of *extracting the resistor and capacitor network;*

performing serial and parallel reductions to the resistor and capacitor network.

'053 patent, 8 :1-4.

1. "extracting the resistor and capacitor network"

Synopsys contends that, at most, the Court should interpret the word "extracting" to mean determining by calculation. Nassda's proposed construction of this entire limitation reads as follows:

During the block level verification, perform an RC extraction within each block to determine the equivalent RC network of the interconnect wires. RC extraction is a method of assigning resistance and capacitance values to the interconnect wires. The resistance and capacitance values extracted from the interconnect wires form an equivalent RC network for that block.

Again, the Court is not convinced that the specification limits the applicability of RC extraction to block level verification only or that the extraction must occur within each block.

The Court adopts the following construction:

Perform an RC extraction. RC extraction is a method of assigning resistance and capacitance values to the interconnect wires. The resistance and capacitance values extracted from the interconnect wires form an equivalent RC network for a block.

2. "performing serial and parallel reductions to the resistor and capacitor network"

The parties agree that "reductions" means mathematical simplification of resistors and capacitors. Synopsys provides proposed definitions of the words "serial" and "parallel." Nassda proposes the following construction: "Reduce, or mathematically simplify, the RC network for each block into an electrically equivalent circuit by combining the resistance values and combining the capacitance values using parallel and/or series reductions of resistors and capacitors." The Court agrees with Synopsys that this limitation is easily understood by one of ordinary skill in the art. Nassda does not argue that any of the words in this limitation are ambiguous, and the portions of the specification cited by Nassda do not provide support for Nassda's proposed construction.

The Court adopts the following construction:

"Serial" means of, relating to, consisting of, or arranged in a series. "Parallel" means to be coupled between the same nodes.

E. Claim 5

Claim 5 reads:

The method of claim 1, further comprising the steps of:

calculating peak voltages at a plurality of nodes and average currents flowing through a plurality o f wires;

storing the peak voltages and average currents.

Synopsys argues that "calculating peak voltages at a plurality of nodes and average currents flowing through a plurality of wires" is clear on its face and requires no construction. Nassda proposes the following construction: "Calculate the peak voltages at more than one node within the blocks and/or the top level power network. A node is an intersection of two or more interconnect wires. Calculate the average currents flowing through more than one interconnect wire within the blocks and/or the top level power network." As set forth above, the Court is not convinced that the blocks necessarily exclude the top level power network. The Court will construe particular terms within the limitation.

"Plurality" means more than one. A "node" is an intersection of two or more interconnect wires.

F. Claim 6

Claim 6 reads as follows:

The method of claim 1 further comprising the step of *performing a top level simulation by: accessing a file corresponding to the semiconductor chip;*

identifying transistors of a top level transistor netlist;

assigning voltage vectors to drive the transistors;

performing voltage drop and current density analysis;

resolving top level issues.

1. "performing a top level simulation"

Synopsys argues that the Court need only interpret the term "top level" to mean a first level of hierarchy. Nassda argues that this step should be construed as follows: "Perform a top level simulation: Determine the actual voltage drops and current waveforms through the top level interconnect wires based on the top level power netlist obtained from the simplifying stage and the recorded current waveforms obtained during the block level verification. This top level simulation includes the following steps:" Nassda then lists a lengthy set of steps drawn from the embodiment described in the specification. The Court sees no reason to adopt the lengthy construction proposed by Nassda. The Court will adopt the definition of "top level" provided by Synopsys.

"Top level" means a first level of hierarchy. The manner in which the "simulation" is performed is described in the following limitations.

2. "accessing a file corresponding to the semiconductor chip"

The parties agree that "accessing a file" means reading a file. Synopsys maintains that no further interpretation of this limitation is necessary. Nassda proposes the following construction: "Access, or read

data, from the top level power netlist." In support of its position that this step applies only to the top level power netlist, Nassda cites to Figure 9, Block 901, which reads: "Access Whole Chip Netlist Files," and an excerpt from the specification reading: "First, the whole chip netlist files (.espf), including calls to reduced .awe block files, is accessed in step 901." '053 patent, 6 :6-8. Neither of these references limits this step to the top level power netlist.

In light of the parties' agreed construction of the phrase "accessing a file," the Court finds that there is no need for any further construction of this limitation.

3. "identifying transistors of a top level transistor netlist"

Synopsys contends that, in addition to the proposed definition of "top level," adopted by the Court above, only the word "netlist" requires any interpretation. Synopsys provides the following definition of "netlist": " 'Netlist' means a point-to-point description of the connections between individual components in a circuit." Nassda proposes the following construction: "Identify more than one transistor in a top level transistor netlist. A top level transistor netlist is a netlist that contains electrical information about transistors located among the top level interconnect wires." The Court agrees with Synopsys that only the word "netlist" needs definition here. Synopsys' definition, drawn from the Authoritative Dictionary of IEEE Standard Terms, will be adopted.

"Netlist" means a point-to-point description of the connections between individual components in a circuit.

4. "assigning voltage vectors to drive the transistors"

Synopsys argues that the only term requiring definition in this limitation is "voltage vectors." According to Synopsys, "voltage vector" means a voltage stimulus pattern containing electrical test information that is applied to a design. Nassda's proposed construction for this limitation is as follows: "Assign test vectors containing voltage values to the transistors in the top level power network for simulation of at least the transistors." Again, the Court is not convinced that adding wording regarding the top level power network, simulation, or "at least the transistors" is appropriate here. The Court therefore adopts Synopsys' definition of "voltage vector" and finds no need to provide any further interpretation of the limitation.

"Voltage vector" means a voltage stimulus pattern containing electrical test information that is applied to a design.

5. "performing voltage drop and current density analysis"

Taking into account the definition of "voltage drop" set forth above, Synopsys argues that, at most, the Court need only define the term "current density" to mean "the concentration of current traveling on a conductive path such as a wire." Nassda proposes the following construction:

Simulate the top level power network, including the transistors, at various instances over time to determine voltages and current densities. Based on this simulation, perform voltage drop and current density, or electromigration, analyses to determine whether voltage drop is too much or current density is too high in the top level power network and transistors.

Again, the Court finds that Nassda's proposed construction, essentially rewording the limitation based on the description of an embodiment in the specification, is inappropriate. The Court adopts Synopsys' definition of

"current density":

"Current density" means the concentration of current traveling on a conductive path such as a wire.

6. "resolving top level issues"

Synopsys contends that this limitation is clear on its face. Nassda proposes the following construction: "Resolve all top level voltage drop and electromigration issues by fixing whatever problems show up with the top level power network as a result of the simulation." Nassda's proposed construction inappropriately limits this step to voltage drop and electromigration issues. This Court has already interpreted "top level" to mean simply "a first level of hierarchy."

The Court finds that this limitation requires no further interpretation.

G. Claim 7

Claim 7 reads as follows:

The method of claim 1 further comprising the step of *determining whether the voltage drops result in any violations*.

Synopsys argues that the Court need only interpret the word "violation." According to Synopsys, "violation" means "a situation not meeting a predetermined specification." Nassda's proposed construction is as follows: "Determine whether there are any voltage drop violations in the top level power network, meaning whether voltage drop is too much to allow the circuit to perform correctly." The Court adopts the following construction:

"Violation" means a situation not meeting a predetermined specification.

H. Claim 8

Claim 8 reads as follows:

The method of claim 1 further comprising the step of *expanding one of the blocks to a transistor level, wherein some of the blocks are analyzed at a top level and some blocks are analyzed at the transistor level*.

1. "expanding one of the blocks to a transistor level"

Synopsys argues that only the word "expanding" needs clarification, and that it should be defined: "increasing in extent, number, volume, or scope." Nassda argues that the entire limitation should be construed as follows: "Instead of using the derived model for one of the blocks, expand one block back to its actual electrical components." The Court adopts Nassda's proposed construction:

Instead of using a derived model for one of the blocks, expand one block back to its actual electrical components.

2. "wherein some of the blocks are analyzed at a top level and some blocks are analyzed at the transistor level."

Synopsys argues that this limitation is clear on its face, taking into account the earlier definitions of the words "block," "analyzed," and "top level." Nassda proposes the following construction: "During the re-simulation of the blocks, simulate some of the blocks at a top level using the modeled block information and some blocks at the transistor level using their actual electrical components." Nassda's proposed construction simply adds a requirement that a simulation take place.

The Court finds that, because "block," "analyzed," and "top level," have already been defined, this limitation requires no interpretation.

I. Claim 9

Claim 9 is the second independent claim in the '053 patent. It reads as follows:

A computer-readable medium having stored thereon instructions for causing a computer to implement computer-controlled reliability analysis of a semiconductor chip design, comprising the steps of:

performing a *block level verification,* wherein the semiconductor chip design is divided into a plurality of *blocks* and a *full voltage supply is assumed to be input to each power connection point corresponding to the blocks;*

modeling the blocks by equivalent RC networks;

performing a simulation on the modeled blocks to determine voltage drops and current values;

analyzing the blocks according to the voltage drops and current values to determine whether there are any performance problems with the chip design.

Synopsys notes that this claim, unlike Claim 1, specifically includes a full voltage supply input to each power connection point, and that it specifically requires a simulation and a determination of current values.

1. Preamble

Synopsys argues that because the premble merely states a purpose or intended use for the invention, it is non-limiting and does not need to be construed. Nassda proposes an altered version of the preamble wording reading as follows: "A storage medium that can be read by a computer containing instructions enabling the computer to implement and control a reliability analysis of a semiconductor chip design. The analysis includes the following steps." The Court agrees with Nassda that the preamble, in describing a computer-readable medium having stored thereon particular instructions, sets forth a structural limitation on the scope of the claim. *See* Corning Glass Works v. Sumitomo Elec. U.S.A., 868 F.2d 1251, 1257 (Fed.Cir.1989). However, the Court sees no need to adopt the construction proposed by Nassda, which simply involves rearranging the disputed language without making it any clearer than it already is.

The Court finds that the language of the preamble does not require interpretation.

2. Remaining Limitations of Claim 9

The remaining disputed limitations of Claim 9 are substantially identical to those in Claim 1 interpreted above. Indeed, the parties simply refer the Court to their arguments for the equivalent limitations from

Claim 1. The disputed limitations contain no further terms that were not already addressed in Claims 1-8 that require construction.

a. "performing a block level verification"

See the construction for "block level verification" in Claim 1.

b. "blocks"

See the construction for "blocks" in Claim 1.

c. "full voltage supply is assumed to be input to each power connection point corresponding to the blocks"

As set forth above, the language of this limitation is different from the corresponding limitation in Claim 1 in that it requires full voltage supply to each power connection point. The Court finds that the limitation contains no terms that need interpretation that have not already been defined.

d. "modeling the blocks by equivalent RC networks"

See the construction for "modeling" and "RC networks" in Claim 1.

e. "performing a simulation on the modeled blocks to determine voltage drops and current values"

Synopsys argues that this limitation is clear on its face and contains no further terms not already addressed in claims 1-8 that need claim construction. Nassda proposes a lengthy construction essentially mirroring the steps for "determining voltage drops corresponding to the equivalent circuit" in Claim 1, although Nassda recognizes that the instant simulation occurs on the blocks, rather than the top level power network.

The Court finds that this limitation contains no terms that require interpretation.

f. "analyzing the blocks according to the voltage drops and current values to determine whether there are any performance problems with the chip design"

Synopsys argues that this limitation is clear on its face. Nassda refers the Court to its discussion of the corresponding, yet somewhat different, limitation in Claim 1. The Court finds that, taking into account the terms in this limitation that have already been defined, there is no need to provide any further interpretation.

J. Claim 16

Claim 16, another independent claim, reads as follows:

A computer system for implementing computer-controlled reliability analysis of a semiconductor chip design, comprising:

a memory for storing *a netlist and a layout corresponding to a schematic* of the semiconductor chip;

a processor coupled to the memory for performing a *block level verification,* wherein the *layout* is divided into a plurality of *blocks* and a *full voltage supply is assumed to be input to each power connection point*

corresponding to the blocks, the processor models the blocks by equivalent RC networks and performs a simulation on the modeled blocks to determine voltage drops and current values, wherein the blocks are analyzed according to the voltage drops and current values to determine whether there are any violations with the chip design;

a display coupled to the processor for displaying the violations.

1. Preamble

The preamble describes a computer system for implementing computer-controlled reliability analysis of a semiconductor chip design. Synopsys argues that because the preamble merely states a purpose or intended use for the invention, it is non-limiting and does not need to be construed. Nassda proposes the following construction of the preamble: "A computer system that can implement and control a reliability analysis of a semiconductor chip design, which includes at least the following elements." As with Claim 9, the Court finds that the preamble sets forth a structural limitation on the scope of the claim, but finds that the language does not require any interpretation. Nassda's proposed construction simply involves altering the order of the language in the preamble.

2. "a memory for storing a netlist and a layout corresponding to a schematic of the semiconductor chip."

Both parties propose alternate definitions of the words "netlist," "layout," and "schematic." "Netlist" has already been defined in Claim 6; the same definition applies here. The Court adopts Synopsys' definition of "layout" and Nassda's definition of "schematic".

"Layout" means an arrangement. "Schematic" means a drawing that shows, in electrical symbols, what components make up a circuit and how they are connected.

3. "block level verification"

See the construction for "block level verification" in Claim 1.

4. "wherein the layout is divided into a plurality of blocks"

See the construction for "layout" from subsection 2, above, and the construction for "block" in Claim 1.

5. "a full voltage supply is assumed to be input to each power connection point corresponding to the blocks"

Synopsys contends that this limitation contains no terms not already addressed in claims 1-8 that need construction. Nassda argues that the limitation should be construed in the same manner as "based on an assumption that full voltage is being supplied to the blocks" from Claim 1. The Court agrees with Synopsys that the limitation contains no terms not already addressed in claims 1-8 that need construction.

6. "the processor models the blocks by equivalent RC networks"

Synopsys argues that this limitation contains no terms not already addressed in claims 1-8 that need construction. Nassda proposes the same construction as it did for "modeling the blocks according to a

resistor and capacitor network" from Claim 1. The Court agrees with Synopsys that, to the extent that any terms need interpretation, the constructions provided for those terms with respect to claims 1-8 can be applied.

7. "performs a simulation on the modeled blocks to determine voltage drops and current values"

Synopsys contends that this limitation is clear on its face and contains no further terms not already addressed in claims 1-8 that need construction. Nassda proposes the same construction as it did for "performing a simulation on the modeled blocks to determine voltage drops and current values" for Claim 9. Because the language here is nearly identical to the corresponding limitation in Claim 9, the Court adopts the same construction for this limitation.

8. "wherein the blocks are analyzed according to the voltage drops and current values to determine whether there are any violations with the chip design"

Synopsys contends that this limitation is clear on its face and contains no further terms not already addressed in claims 1-8 that need construction. Nassda proposes the same construction as it did for "analyzing the blocks with the voltage being supplied to the blocks reduced according to the determined voltage drops" from Claim 1. The Court adopts the same construction it did for the corresponding limitation in Claim 1.

9. "a display coupled to the processor for displaying the violations"

Synopsys argues that only the word "display" needs definition here. According to Synopsys, that word means "a device that gives information in a visual form, as on a screen." Nassda contends that the limitation, taken as a whole, should be construed as follows: "a computer monitor connected to the microprocessor for displaying the voltage drop and current density violations." The section of the specification cited by Nassda does not limit the display to providing voltage drop and current density violations. Accordingly, the Court finds that the only word needing interpretation is "display."

"Display" means a device that gives information in a visual form, as on a screen.

CONCLUSION

For the reasons discussed, the terms are hereby construed as stated above.

IT IS SO ORDERED.

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