United States District Court,
E.D. Texas, Marshall Division.

INTERGRAPH CORPORATION,
Plaintiff(s).
v.
INTEL CORPORATION,
Defendant(s).

No. 2:01-CV-160 (TJW)

June 3, 2002.

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ORDER

T. JOHN WARD**, District Judge.**

On May 10, 2002, the Court held a claim construction hearing in this matter in accordance with its responsibilities under Markman v. Westview Instruments, Inc., 517 U.S. 370, 116 S.Ct. 1384, 134 L.Ed.2d 577 (1996). Having considered the claim construction memoranda, the law, and the intrinsic evidence, together with the arguments of counsel, the Court issues the following order.

I. Introduction.

Plaintiff Intergraph Corp. ("Intergraph") accuses Defendant Intel Corp. ("Intel") of infringing claims contained in United States Patents 5,560,028 ("'028") and 5,794,003 ("'003"). The parties have identified seventy-plus claim terms contained in the two patents that they allege require construction. The parties' positions with regard to many of these "disputed terms," however, do not differ in substance and, had the parties proceeded appropriately, should have resulted in agreed definitions of many of the disputed terms. But, because the parties to this suit have demonstrated a conscious disregard for a reasonable approach to claim construction, the Court draws the task of sorting through the patents, identifying the pertinent areas of dispute, and construing the claim terms appropriately.

II. Legal principals relevant to claim construction.

"A claim in a patent provides the metes and bounds of the right which the patent confers on the patentee to exclude others from making, using or selling the protected invention." *Burke, Inc. v. Bruno Indep. Living Aids, Inc.,* 183 f.3d 1334, 1340 (Fed.Cir.1999). Claim construction is an issue of law for the Court to decide. Markman v. Westview Instruments, Inc., 52 F.3d 967, 970-71 (Fed.Cir.1995) (en banc), *aff'd,* 517 U.S. 370, 116 S.Ct. 1384, 134 L.Ed.2d 577 (1996).

To ascertain the meaning of claims, the Court looks to three primary sources: the claims, the specification, and the prosecution history. Markman, 52 F.3d at 979. Under the patent law, the specification must contain a written description of the invention that enables one of ordinary skill in the art to make and use the invention. A patent's claims must be read in view of the specification, of which they are a part. *Id.* For claim construction purposes, the description may act as a sort of dictionary that explains the invention and may define terms used in the claims. *Id.* "One purpose for examining the specification is to determine if the patentee has limited the scope of the claims." Watts v. XL Sys., Inc., 232 F.3d 877, 882 (Fed.Cir.2000).

Nonetheless, it is the function of the claims, not the specifications, to set forth the limits of the patentee's claims. Otherwise, there would be no need for claims. SRI Int'l, v. Matsushita Elec. Corp., 775 F.2d 1107, 1121 (Fed.Cir.1985) (en banc). As a general rule, words in claims are given their ordinary and customary meaning. Vitronics Corp. v. Conceptronics, Inc., 90 F.3d 1576, 1582 (Fed.Cir.1996). Before the Court redefines the meaning of particular claim terms away from their ordinary meaning, the intrinsic evidence must clearly evidence a different meaning or redefine the claim terms. Bell Atlantic Network Serv. v. Covad Communications Group, Inc., 262 F.3d 1258, 1268 (Fed.Cir.2001). Thus, while the patentee is free to be his own lexicographer, any special definition given to a word must be clearly set forth in the specification. Intellicall, Inc. v. Phonometrics, 952 F.2d 1384, 1388 (Fed.Cir.1992). And, although the specifications may indicate that certain embodiments are *preferred,* particular embodiments appearing in the specification will not be read into the claims when the claim language is broader than the embodiments. Electro Med. Sys., S.A. v. Cooper Life Sciences, Inc., 34 F.3d 1048, 1054 (Fed.Cir.1994).

III. Terms in dispute.

'028 Patent

1. Groups/sets of individual instructions.

Relying on plain and ordinary meaning, Intergraph contends "group of individual instructions" simply means that individual instructions are organized into groups. Intel contends the phrase imports much more than this. However, Intel seems perplexed with determining just how much more the phrase imports, as it has tendered a different definition for "group of individual instructions" in the Joint Claim Construction Statement, in its claim construction brief, and in its presentation at the *Markman* hearing. Putting this moving target tactic aside, Intel's latest claim interpretation argues the phrase should mean a set of instructions that the compiler has determined will be executed in parallel. Intel further delineates its position with the following restrictions: 1) groups of instructions must be within a VLIW and 2) all instructions in each set must be executed in parallel and groups cannot be split across instruction frames.

Based on a review of the claim language and the intrinsic evidence, the Court cannot embrace either of

these positions in whole. The Court construes "groups/sets of individual instructions" as a collection of one or more individual instructions that can be executed simultaneously (i.e. can be dispatched to parallel pipelines simultaneously). '028 patent at 5:10-20.

2. Very long instruction words.

Intergraph invokes fundamental rules of claim construction and asserts that the phrase "very long instruction word" is specifically defined in the claims of the '028 patent as "having a predetermined number N of instructions and including at least one group of M individual instructions to be executed in parallel, where M is less than or equal to N." Intel contends that "VLIW," when employed in the context of a "wide-word" processing architecture, carries with it a definition standard among those skilled in the art at the time the '028 patent was filed. FN1 Accordingly, Intel proposes a construction drawing upon the traditional definition of VLIW discussed in the patent's specification, but augmented by specific limitations it derives from Figs. 7, 10, & 11 of the '028 patent. In sum, Intel proposes the term "very long instruction word" as used in the claims should mean a fixed width frame containing at least 2 tightly packed groups of instructions, each instruction within each frame having a group identifier and a pipeline identifier contained therein.

FN1. Whether the term "very long instruction word" used in the claim was meant to embrace the same concept as the acronym "VLIW" used in the context of "wide-word" processing architecture is a matter for the Court. The patents only use VLIW in describing the prior art and purpose of the proposed invention. In the claims, however, the patentee repeatedly uses the phrase "very long instruction word," not "VLIW." Accordingly, the Court construes the term "very long instruction word."

The Court construes "very long instruction word" as a fixed-width instruction that encodes multiple operations. '028 patent at 1:64-66; 5:23-25. A "very long instruction word" may contain one or more groups of individual instructions. *Id*. at 5:25-28.

3. Very long instruction word storage/register.

Intergraph asserts this term is defined in the summary of the invention of the '028 patent and means "a cache line, a register or other mechanism for holding at least one group of instructions." '028 patent at 3:19-20. Intel seeks to narrow the phrase by including a description of the group of instructions the storage/register is meant to hold, thus finding the term to mean a line in the instruction cache adapted to hold a very long instruction word having at least two groups of instructions, each instruction having pipeline and group identifiers embedded therein. The Court construes the term as a cache line or other mechanism for holding a very long instruction word. ' 028 patent 3 :19-21; 9 :31-38; Fig. 10. The term "very long instruction word" has been defined above.

4. Pipeline identifier.

Intergraph contends this term is defined in the claims as an identifier indicative of a processing pipeline for executing an associated individual instruction. Intel argues, however, that the specification and prosecution history of the '028 patents limit "pipeline identifier" to a "compiler-generated tag embedded within each instruction that identifies the explicit processing pipeline that will execute the instruction." While the prosecution history cited by Intel does support a requirement that instructions be "embedded," the history relates only to specific claims that included the term "embedded." This history in no way imposes an "embedded" requirement on every claim using the term "pipeline identifier." Further, Intel's citations fail to

support its requirement that the identifier necessarily identify the explicit processing pipeline.

The Court construes "pipeline identifier" as a designation indicative of a processing pipeline. '028 patent 3 :9-17; 5 :15-17.

5. Group identifier.

Intergraph contends this term too is defined in the claims as an identifier indicative of a group of individual instructions to which the individual instruction is assigned for execution in parallel. Though again employing its moving target tactic described earlier, Intel's ultimate definition of the term is a tag assigned by the compiler to each instruction that identifies instructions that will execute in parallel (i.e., issued to different and separate processing pipelines on the same clock cycle and processed simultaneously by the pipelines). Intel claims this definition is made clear in the '028 patent's specifications and prosecution history. However, as discussed with respect to pipeline identifiers, these references provide little support for Intel's proposed construction in general. The Court construes "group identifier" as a designation indicative of a group of individual instructions, as that term has been previously defined. '028 patent 3 :24; 5 :10-14.

6. Associated therewith or having.

Relying on the plain meaning of the terms, Intergraph argues "associated therewith" means "related to, but not necessarily embedded within." Intergraph supports this position with language from the '028 patent's specifications which states, "[w]e use the word 'associated' herein to designate the concept that the pipeline and group identifiers are not required to have a fixed relationship to the instruction words. That is, the pipeline and group identifiers need not be imbedded within the instructions themselves as shown in FIG. 7. Instead they may arrive from another means, or on a different cycle." ' 028 patent at 8: 20-26. Intel, however, relying on communications with the patent examiner during prosecution, claims that pipeline and group identifiers must be "embedded" or "encapsulated" within each individual instruction. Thus, Intel contends "associated therewith" or "having" requires that the identifier be embedded within the instruction. However, as discussed above, Intergraph's acceptance of an "embedded" limitation in the prosecution of some claims, claims that issued with the term "embedded" included, does not limit all claims issued.

Thus, the Court construes "associated therewith" or "having" as logically related to or logically connected, but not necessarily embedded. '028 patent at 8: 20-26.

7. Embedded.

Intel defines "embedded" or "embedding" by reference to the word "encapsulating." However, Intel offers no argument or support for its position that "embedded" means "encapsulated," despite being asked directly about this matter at the claim construction hearing. In the Joint Claim Construction Statement, Intel attempts to define "embedded" by reference to what it believes is embedded within an instruction. Contending the term carries no special meaning, Intergraph offers a dictionary definition of "embedded." The Court construes "embedded" as introduced as or made an integral part thereof. '028 patent 7 :9-45; Fig. 6 & 7 (defining by way of description); Webster's II New College Dictionary 366-67 (1995).

8. Adjacent to/ next to.

Intergraph argues "adjacent to" or "next to" carries its plain and ordinary meaning and needs no further construction. Intergraph offers a definition of "relatively near and having nothing of the same kind

intervening." Intel, relying on the '028 specification at 5:61-65, counters that the term means groups are to be placed side-by-side within a frame in accordance with the issue sequence of the groups. Intel's position, however, goes beyond that which is necessary to define these relatively simple, descriptive terms. The Court construes "adjacent to" and "next to" as side-by-side, alongside, beside, or in the next position. '028 patent at 3:31-37; 5:61-6:5.

9. Coupled.

Intergraph again argues this term carries its ordinary meaning "in connection with." Intel argues "coupled" means electrically connected. The Court construes "coupled" as connected, directly or indirectly. '028 patent 10 :5-9; 11 :2-3.

10. Arbitrary number of instructions.

Intergraph contends this phrase carries its ordinary meaning to a person skilled in the art. Intel, incorporating specific claim requirements into the definition of the term, defines the phrase as a number of instructions in a group of instructions that are executed simultaneously that is less than the width of an instruction frame. The Court construes the term as any number of instructions. '028 patent 5 :19-23.

11. Crossbar/ crossbar switch.

Maintaining a consistent position, Intergraph argues "crossbar" or "crossbar switch" carries its ordinary meaning to one skilled in the art. Intel claims the terms "crossbar, associative crossbar, and associative crossbar switch" are all synonymous and mean a switch located within the scalar cache, that has a set of connectors in electrical contact with the storage, is controlled solely by pipeline identifiers embedded by the compiler within each of the software-scheduled instructions being routed through the switch, and has another set of connectors in electrical contact with the processing pipelines. Intel arrives at this definition by, again, placing specific requirements from one or more claims into the definition of the term itself. The Court cannot embrace this method of defining terms, as the claim requirements vary from claim to claim. Accordingly, the Court construes "crossbar" and "crossbar switch" as a switch that selectively couples a group of instructions from the very long instruction word storage to the processing pipelines. '028 patent at 3:11-18; 9:66-10:9.

12. Associative crossbar/ associative crossbar switch.

Borrowing from Intel's practice of incorporating claim elements into the definition of a term, Intergraph defines "associative crossbar" as a first set of connectors coupled to the super scaler storage for receiving each of the software-scheduled instructions therefrom, and a second set of connectors coupled to the plurality of instruction pipelines. Intel's proposed construction is addressed above, as it views the terms "crossbar" and "associative crossbar" to be synonymous. The Court construes "associative crossbar" and "associative crossbar switch" as a crossbar in which the data being routed includes the routing instructions. '028 patent at 3:11-17; 10:10-21.

13. Connectors.

Intergraph argues this term carries its ordinary meaning to a person skilled in the art. Intel contends "connectors" lacks a commonly understood meaning as used in the context of the claims. Relying upon Fig. 10, Intel defines "connectors" as a series of instruction word paths with regard to "first set of connectors"

and a series of pipeline pathways with regard to "a second set of connectors." The Court construes "connectors" as conductors or terminals for making connections. '028 patent at 10:3-9.

The Court is of the opinion that its resolution of the meaning of the above terms resolves the parties' disputes with regard to the '028 patent and that any remaining terms need not be construed.

Means-plus-function elements.

1. Group decoder means responsive to the group identifier for each individual instruction in the very long instruction word storage to be executed for enabling each individual instruction in the very long instruction word storage having similar group identifier to be executed in parallel by the plurality of processing pipelines.

The parties agree that this claim element is drafted in means-plus-function form pursuant to 35 U.S.C. s. 112 para. 6. Under s. 112 para. 6, the Court must first identify the function recited for the "means." The Court then must identify the corresponding structure that the specification links to the function. Medtronic v. Advanced Cardiovascular Sys., 248 F.3d 1303, 1311 (Fed.Cir.2001).

The parties dispute this element's claimed function. Intergraph contends the claimed function is as stated by the claim, "enabling each individual instruction in the very long instruction word storage having similar group identifier to be executed in parallel by the plurality of processing pipelines." Intel argues the "responsive to" language contained in the element is also a part of the recited function or an additional function to be performed by the "means." The Court holds the "responsive to" phrase used in this element, as well as several other means-plus-function elements, is descriptive of the "means," but is not part of the function performed by the "means." Thus, the claimed function is "for enabling each individual instruction in the very long instruction word storage having similar group identifier to be executed in parallel by the plurality of processing pipelines." All disputed terms appearing in the function have been previously defined.

The parties also dispute the corresponding structure. Intergraph identifies the corresponding structures as three alternative embodiments. The first of these includes structures 150-157 of '028 patent Fig. 10. The second and third embodiments cited provide no description of a specific structure. Intel's corresponding structures include those listed in Intergraph's first alternative, along with various other structures of Fig. 9 and 10. The Court finds neither parties' position wholly correct. Rather, the Court concludes the corresponding structures for performing the recited function are structures 150-157 and 144 of '028 patent Fig. 10. '028 patent at 9:50-52, 58-62; Fig. 10. Thus, under s. 112 16, the "group decoder means" is construed to cover the structures 150-157 and 144 and equivalents thereof.

2. Pipeline decoder means responsive to the pipeline identifier of each individual instructions in the very long instruction word storage to be executed for causing each individual instruction in a group of individual instructions having a similar group identifier to be supplied to the different processing pipelines.

The parties agree that this element is drafted in means-plus-function form. The recited function is "for causing each individual instruction in a group of individual instructions having a similar group identifier to be supplied to the different processing pipelines." The parties dispute the corresponding structures.

Intergraph argues the corresponding structures are two alternative embodiments: 1) structures 170-177 of

Figs. 10 and 11, and 2) an alternative which again contains no description of a particular structure. Intel contends the claimed means includes those items identified by Intergraph, plus the instruction word paths 190-197, the pipeline pathways 180-187 and the switches that interconnect the two. The Court concludes the disclosed structures are structures 170-177 of Figs. 10-11. '028 patent at 10:10-33. Thus, the "pipeline decoder means" is construed to cover the structures 170-177 and equivalents thereof.

3. Selection means coupled to the very long instruction word storage for receiving, the group identifier for each individual instruction in the very long instruction word, for determining in response thereto a group of individual instruction to be executed in parallel, and for outputting a control signal.

The parties agree that this element is drafted in means-plus-function form and that the claimed function is "for receiving the group identifier for each individual instruction in the very long instruction word, for determining in response thereto a group of individual instruction to be executed in parallel, and for outputting a control signal."

Intergraph again argues the corresponding structures by presenting three alternative embodiments with only the one having merit. That embodiment identifies structures 150-157 of Fig. 10. Intel argues the corresponding structures for the "selection means" are registers 130, 144 and 145, and MUX 140. The Court concludes the disclosed structures are structures 150-157, 140, and 144 of Fig. 10. '028 patent at 9:30-62. Thus, the "selection means" is construed to cover the structure 150-157, 140, and 144 and equivalents thereof.

4. Decoder means coupled to the selection means and to the very long instruction word storage, for receiving the control signal and the pipeline identifier for each individual instruction and the very long instruction word, for determining in response thereto the appropriate processing pipeline for each individual instruction of the group, an for outputting switch control signals.

The parties agree that this element is drafted in means-plus-function form and that the claimed function is "for receiving the control signal and the pipeline identifier for each individual instruction and the very long instruction word, for determining in response thereto the appropriate processing pipeline for each individual instruction of the group, and for outputting switch control signals."

In its meritorious alternative embodiment, Intergraph claims the corresponding structures are structures 170-177 of Figs. 10 and 11. Intel argues the corresponding structures are those proposed by Intergraph, plus the comparators 150-157. The Court concludes the disclosed structures are structures 170-177. ' 028 patent at 10:10-33; Figs. 10 and 11. Thus, the "decoder means" is construed to cover structures 170-177 and equivalents thereof.

5. Other alleged means or step-plus-function elements.

Intel argues a number of other elements contained in the '028 patent are in step-plus function form and, thus, are also governed by s. 112 para. 6. However, none of these elements contain language indicating a step-plus function form to which s. 112 para. 6 would apply. Accordingly, a presumption exists that these elements are not governed by s. 112 para. 6. Seal-Flex, Inc. v. Athletic Track & Court Const., 172 F.3d 836, 850 (Fed.Cir.1999). Intel has provided no evidence to overcome this presumption. And, because all disputed terms contained in these elements have been previously defined, no further construction is required.

Intel also argues that the phrase "detection means to receive group identifiers of each instruction to be executed in the very long instruction word" contained in claim 9 is a means-plus-function element to be construed under s. 112 para. 6. However, this phrase is not a means-plus-function element. Rather, the phrase presents a detection apparatus in a method claim, which is not governed by s. 1121 para. 6. *See* O.I. Corp. v. Tekmar Co. Inc., 115 F.3d 1576, 1582-83 (Fed.Cir.1997). As all other disputed terms are previously defined, no further construction is needed.

'003 Patent

1. Super scaler cache

Both parties seek to define this phrase by incorporating specific elements of the claims into the definition of the term itself. However, the elements comprising the structure vary among the claims. *Compare* '003 patent at 7:35-55, *with id*. at 8:18-43. Thus, the Court cannot accept this construction approach and looks to the Patent Office examiner's characterization in the prosecution history. The Court construes "super scaler cache" as a cache capable of holding multiple instructions for issuing and executing in parallel. *See* Intel's Claim Construction Brief, Exhibit D, tab. 18, p. 3.

2. Group/ set of software scheduled instructions.

Intergraph argues this term carries its ordinary meaning to one skilled in the art. Intel again inserts elements from other claims to define "group of software scheduled instructions" as a set of 2 or more instructions within the same VLIW which have a common group identifier and which are executed simultaneously. The Court construes "groups of software scheduled instructions" and "sets of software scheduled instructions" as sets of one or more instructions that have been identified by software as being capable of being processed in parallel. '003 patent at 3:61-63.

3. Super scaler storage

Intergraph contends no construction is required for this term, but that it should be given its ordinary meaning to one skilled in the art. Intergraph identifies this ordinary meaning as "storage such as a cache line, a register or other mechanism for holding one group of the groups of software-scheduled instructions, each software-scheduled instruction within the one group having embedded therein an instruction pipeline identifier of a plurality of instruction pipeline identifiers." Incorporating its proposed definition of other terms, Intel similarly defines "super scaler storage" as a memory device adapted to hold one group of instructions where each instruction has a pipeline identifier embedded inside. The Court construes "super scaler storage" as a cache line, register, or other memory device capable of holding multiple instructions for issuing and executing in parallel. '003 patent 5 :32-35.

4. Associated therewith or having.

The parties positions with regard to this term remain consistent from the '028 patent. The Court construes "associated therewith" or "having" as logically related to or logically connected, but not necessarily embedded. '003 patent at 4: 37-45.

5. Communication buses.

The parties' positions with respect to this term do not differ in substance. Intergraph defines

"communication buses" as electrical paths capable of conveying software scheduled instructions, one path for each of the software scheduled instructions. Intel defines the term as electrical connections capable of conveying software-scheduled instructions. The Court construes "communication buses" as electrical paths capable of conveying software scheduled instructions. '003 patent at 5:17-22.

6. Very long instruction word cache.

Intergraph argues that this term is defined by the claims as being similar to a "super scaler cache." Thus, Intergraph's proposed definition seeks to delineate meaning of this term by reference to what it comprises. As discussed in the context of "super scaler cache," this approach is problematic.

Intel, however, adopts an equally problematic approach to defining this term. Intel argues that because the patentee used the term "very long instruction word cache" to distinguish its invention over the prior art during prosecution, it has incorporated the prior art into the present term. Thus, Intel defines "very long instruction word cache" as memory capable of storing VLIW data in a VLIW architecture.

The Court construes the term "very long instruction word cache" as memory or other storage capable of storing very long instruction word data. '003 patent at 2:6-11; 5:31-35.

7. Embedded.

The Court construes "embedded" as introduced as or made an integral part thereof. Webster's II New College Dictionary 366-67 (1995).

8. Associative crossbar/ associative crossbar switch.

The Court construes "associative crossbar" and "associative crossbar switch" as a crossbar in which the data being routed includes the routing instructions. '003 patent at 1:19-25; 7:3-7.

9. Connectors.

The Court construes "connector" as a conductor or terminal for making a connection. '003 patent at 2:11-15; 5:53-58.

10. Coupled.

The Court construes "coupled" as connected, directly or indirectly. '003 patent 5 :53-58; 6 :27-28.

11. Pipeline identifier.

The Court construes "pipeline identifier" as a designation indicative of a processing pipeline. '003 patent 1 :56-60; 2 :9-11; 3 :40-45.

The Court is of the opinion that its resolution of the meaning of the above terms resolves the parties' disputes with regard to the '003 patent and that any remaining terms need not be construed.

Means-plus-function elements.

1. Means for forming groups of software-scheduled instructions.

The parties agree that this claim element should be construed in accordance with 35 U.S.C. s. 112 para. 6. The first step in construing this claim is to identify the function. The Court holds the function is "forming groups of software-scheduled instructions." All disputed terms appearing in the function have been previously defined; thus, the Court turns to identifying the corresponding structure.

Intergraph argues the corresponding structure is that disclosed in several alternative embodiments in the '028 patent at 3:53-63, 6:23-25, and in the '028 patent at 5:9-13 as incorporated by the '003 patent. The first of these embodiments actually discloses a potential corresponding structure. The second does not. The third embodiment referring to the '028 patent only discloses a compiler, the same structure identified in the first embodiment from the '003 patent itself. Intel alleges the corresponding structure is a "VLIW compiler", arguing that this is the only device capable of performing such a function.

However, a "VLIW compiler" is never recited nor identified in the patent. The Court concludes the corresponding structure is the compiler disclosed at 3:53-63 of the '003 patent. Thus, the "means" is construed as covering a compiler and equivalents thereof.

2. Means responsive to the instruction pipeline identifier of each of the software-scheduled instructions, for coupling appropriate connectors of the first set of connectors to appropriate connectors of the second set of connectors, to thereby supply each of the software-scheduled instructions to the appropriate instruction pipeline for parallel execution.

The parties agree that this element is drafted in means-plus-function form. The Court identifies the function as "for coupling appropriate connectors of the first set of connectors, to thereby supply each of the software-scheduled instructions to the appropriate instruction pipeline for parallel execution." All disputed terms appearing in the function have been previously defined.

The parties agree that the corresponding structures include items 213, 234, 265, and like structures of Fig. 3. Intergraph contends the responsive structure also include the multiplexers shown in Fig. 4. Intel disagrees as to the multiplexers but argues decoders 170-177 of Fig. 3 must be included. The Court agrees with both parties positions regarding the additional structures. Thus, the Court concludes the "means" structures are switches 213, 234, 265, and like structures of Fig. 3, together with decoders 170-177 of Fig. 3, and equivalents of this collective structure; and the multiplexers of Fig. 4 and equivalents thereof. '003 patent at 5:59-6:4; 6:26-34.

3. Means for assembling sets of software-scheduled instructions to be executed in parallel.

The parties agree that this element is drafted in means-plus-function form. The Court identifies the function as "for assembling sets of software-scheduled instructions to be executed in parallel." This claim phrase is practically identical to that of claim 1, as are the parties arguments. Thus, the Court reaches a similar conclusion. The Court concludes the "means" structure is the compiler disclosed at 3:53-63 of the '003 patent and equivalents thereof.

4. Selection means connected to receive the instruction pipeline identifiers of the set of instruction pipeline identifiers, the selection means for supplying in response thereto output signals.

The parties agree, as does the Court, that this element is drafted in means-plus-function form and that the claimed function is for supplying output signals in response to the instruction pipeline identifiers. The

parties also agree that the corresponding structures include structures 170-177 of Fig. 3. Yet, Intergraph argues for an alternative embodiment found in the part of Fig. 14 of the '028 patent responsive to the pipeline identifier that generates SEL0-7 for each of the multiplexers. The passage of the '028 patent Intergraph cites, however, does not disclose a structure for performing the recited function; i.e., a block labeled "ENABLE INSTRUCTIONS," with the accompanying description does not disclose a structure for purposes of s. 112 para. 6. The Court concludes the corresponding structures are structures 170-177 of Fig. 3 of the '003 patent and equivalents thereof. '003 patent at 5:59-62.

Furthermore, the "selection means" in claims 4 and 23 is stated in terms of structure and, hence, is not governed by s. 112 para. 6. As all other terms in these claims have been resolved by the Court, no further construction is required.

5. Switching means coupled to receive the output signals for selectively connecting connectors of the first set of connectors to connectors of the second set of connectors to thereby supply each software-scheduled instruction in the set of software-scheduled instructions to be executed in parallel to the appropriate instruction pipeline.

The parties agree, as does the Court, that this element is drafted in means-plus-function form and that the claimed function is "for selectively connecting connectors of the first set of connectors to connectors of the second set of connectors to thereby supply each software-scheduled instruction in the set of software-scheduled instructions to be executed in parallel to the appropriate instruction pipeline." The parties also agree that the responsive structure includes switches 213, 234, 265, and like structures of Fig. 3. Intergraph, however, again argues that part of the multiplexers of Fig. 4 should be included as an alternative embodiment. The Court agrees and concludes the corresponding structures are switches 213, 234, 265, and like structures of Fig. 3, and equivalents thereof, and the multiplexers of Fig. 4 and equivalents thereof. '003 patent at 5:64-6:15; 6:26-34.

Furthermore, the "switching means" in claims 4 and 23 is stated in terms of structure and, hence, is not governed by s. 112 para. 6. As all other terms in these claims have been resolved by the Court, no further construction is required.

6. Means for forming groups of software-scheduled instruction words, software-scheduled instruction words in each group executable in parallel.

The parties agree that this element is drafted in means-plus-function form. The Court identifies the function as "for forming groups of software-scheduled instruction words, software-scheduled instruction words in each group executable in parallel." This claim phrase is almost identical to that of claim 1 and Intel fails to set forth a corresponding structure, as are the parties arguments. Intergraph argues the corresponding structure should be the same as it proposed for claim 1. The Court incorporates its discussion of Intergraph's arguments from claim 1 and concludes the corresponding structure is the compiler disclosed at 3:53-63 of the '003 patent and equivalents thereof.

7. Means for assembling a group of software-scheduled instruction words, software-scheduled instruction words in the group executable in parallel.

The parties agree that this element is drafted in means-plus-function form. The Court identifies the function as "for assembling groups of software-scheduled instruction words in each group executable in parallel." This claim phrase also is practically identical to that of claim 1, as are the parties arguments. Thus, for the

reasons addressed, Court concludes the corresponding structure is the compiler disclosed at 3:53-63 of the '003 patent and equivalents thereof.

8. Means responsive to the instruction pipeline identifier of each of the software-scheduled instructions, for coupling appropriate connectors of the first set of connectors to appropriate connectors of the second set of connectors, to thereby supply each of the software-scheduled instructions to the appropriate instruction pipeline for parallel execution.

This same claim element appears in claim 1 and is construed above in reference to that claim. The same construction applies with respect to claim 20.

IV. Conclusion.

Having canvassed the parties' respective arguments, the Court is of the opinion that this order resolves all material areas of dispute.

ORDERED.

E.D.Tex.,2002.
Intergraph Corp. v. Intel Corp.