United States District Court,
N.D. California.

XILINX, INC,
Plaintiff.
v.
ALTERA CORPORATION,
Defendant.
ALTERA CORPORATION,
Plaintiff.
v.
XILINX, INC,
Defendant.

No. 93-20409 SW, 96-20922 SW

July 30, 1998.

CLAIM CONSTRUCTION ORDER

WILLIAMS, J.

I. BACKGROUND

On June 7, 1993, Xilinx, Inc. ("Xilinx") initiated Civil Action No. 93-20409 against Altera Corporation ("Altera") alleging infringement of U.S. Reissue Patent No. 34,363 ("the '363 patent") and U.S. Patent No. 4,642,487 ("the '487 patent"). On August 8, 1996, this action was reassigned to this Court.

On June 7, 1993, Altera initiated a separate action against Xilinx alleging infringement of U.S. Reexamination Patent No. B1 4,617,479 ("the B1'479 patent"), and U.S. Patent Nos. 4,774,421 ("the '421 patent") and 4,609,986 ("the '986 patent"). FN1 The specification of the '986 patent incorporates by reference the specification of the B1'479 patent. Altera's action against Xilinx was ultimately given case number Civil No. 96-20922, and on November 7, 1996, was reassigned to this Court.

FN1. Altera also initially alleged infringement of U.S. Patent No. 4,020,469 but has since withdrawn that allegation.

This Court deemed the two actions related and on December 11, 1996, ordered that a joint claim construction hearing be held for both actions. On October 20-23, 1997, the Court conducted the claim construction hearing for the five patents at issue. During the hearing, the parties presented tutorials, offered evidence and made arguments for the purpose of aiding the Court in construing the disputed terms used in the claims. Following the hearing, the parties submitted additional briefs in support of their proposed

constructions.

II. LEGAL STANDARD FOR CLAIM CONSTRUCTION

Determining patent infringement requires a two-step analysis: "First, the claim must be properly construed to determine its scope and meaning. Second, the claim as properly construed must be compared to the accused device or process." Nike Inc. v. Wolverine World Wide, Inc., 43 F.3d 644, 646 (Fed.Cir.1994) (quoting Carroll Touch, Inc. v. Electro Mechanical Systems, 15 F.3d 1573, 1576 (Fed.Cir.1993)). Claim construction is a matter of law to be determined by a court. Markman v. Westview Instruments, Inc., 52 F.3d 967, 979 (Fed.Cir.1995), *aff'd,* 517 U.S. 370, 116 S.Ct. 1384, 134 L.Ed.2d 577 (1996). The comparison between the properly construed claims and the device accused of infringing is a question of fact. General Mills, Inc. v. Hunt-Wesson, Inc., 103 F.3d 978, 981 (Fed.Cir.1997).

A. Evidence

In construing the meaning of claims, courts first consider a patent's intrinsic evidence, which includes the claims, the specification, and the prosecution history. Markman, 52 F.3d at 979. The patent title may be considered as an interpretive aid. *See* Exxon Chemical Patents, Inc. v. Lubrizol Corp., 64 F.3d 1553, 1557 (Fed.Cir.1995). In addition to intrinsic evidence, the parties may offer extrinsic evidence which includes expert testimony, inventor testimony, dictionaries and learned treatises. Markman, 52 F.3d at 980. Although a court may consider extrinsic evidence, it should look first to the intrinsic evidence of record. Vitronics Corp. v. Conceptronic, Inc., 90 F.3d 1576, 1582 (Fed.Cir.1996).

When considering the intrinsic evidence courts are to look first to the claims themselves to define the scope of the invention. Id. at 1582. Generally, the words in a claim are given their ordinary and customary meaning. *Id*. However, "a patentee may choose to be his own lexicographer and use terms in a manner other than their ordinary meaning, as long as the specific definition of the term is clearly stated in the patent specification or file history." *Id*. Thus, the specification may act as a dictionary when it expressly or impliedly defines terms used in the claims. *Id*. Furthermore, the file history is often critical in determining the meaning of the claims. Any interpretation that was disclaimed during the prosecution must be excluded from the definition of claim terms. Southwall Tech., Inc. v. Cardinal IG Co. ., 54 F.3d 1570, 1576 (Fed.Cir.1995), *cert. denied,* 516 U.S. 987, 116 S.Ct. 515, 133 L.Ed.2d 424 (1995).

"In most situations, an analysis of the intrinsic evidence alone will resolve any ambiguity in a disputed claim term. In such circumstances, it is improper to rely on extrinsic evidence." Id. at 1583. Only when intrinsic evidence alone is insufficient may the court use extrinsic evidence, and then only to aid the court in "coming to the proper understanding of the claims" and the technology involved. Id. at 1584. Extrinsic evidence may not be used to vary or contradict the claim language. Markman, 52 F.3d at 981. Expert testimony is to be eschewed and used only as a last resort. Vitronics, 90 F.3d at 1584-85. The Federal Circuit in *Vitronics* showed a clear preference for other types of extrinsic evidence, such as dictionaries and prior art documents. *Id*. at 1585.

B. Means-plus-function Claim Elements

As a general principle of claim construction, limitations found in the specification of a patent should not be read into a claim. In re Donaldson Co., 16 F.3d 1189, 1195 (Fed.Cir.1994). However, claim elements expressed as a means or step for performing a specified function are construed to cover the corresponding "structure, material or acts described in the patent specification" and their "equivalents." 35 U.S.C. s. 112,

para. 6. Under a means-plus-function analysis, if the specification mentions specific alternative structures, those structures are included in the scope of the patent. *See* Serrano v. Telular Corp., 111 F.3d 1578, 1583 (Fed.Cir.1997). A specification that merely mentions the possibility of alternative structures without specifically identifying them is not sufficient to expand the scope of the claim beyond the example used. *See* Fonar Corp. v. General Electric Co., 107 F.3d 1543, 1551 (Fed.Cir.), *cert. denied,* 522 U.S. 908, 118 S.Ct. 266, 139 L.Ed.2d 192 (1997).

"In determining whether to apply the statutory procedure of section 112, para. 6, the use of the word 'means' triggers a presumption that the inventor used this term advisedly to invoke the statutory mandates for means-plus-function clauses." York Prods., Inc. v. Central Tractor, 99 F.3d 1568, 1574 (Fed.Cir.1996). However, "[t]o invoke this statute, the alleged means-plus-function claim element must not recite a definite structure which performs the described function." Cole v. Kimberly-Clark Corp., 102 F.3d 524, 41 U.S.P . Q.2d 1001, 1006 (Fed.Cir.1996). "An element with ... a detailed recitation of structure, as opposed to its function, cannot meet the requirements of the statute." *Id*. Whether the procedure of s. 112 para. 6 applies should be decided "on an element-by-element basis, based upon the patent and its prosecution history." *Id*.

C. "Jepson" Claims

A "Jepson" claim is one that contains (1) a preamble that recites an old device, process, or combination, (2) a transition phrase such as "wherein the improvement comprises," and (3) a body which states the new elements or improvements upon the old device, process, or combination. *See* 37 C.F.R. s. 1.75(e); *see also Ex parte Jepson,* 1917 C.D. 62 (Ass't Comm'r Pat.1917). The preamble in a Jepson claim constitutes "a limitation for purposes of determining patentability and infringement." 3 Donald S. Chisum, *Chisum on Patents* s. 8.06[1][c], at 8-104 (1998); *see also Manual of Patent Examining Procedure,* s. 608.01(m) (6th ed.2d rev.1996) ("The preamble of [a Jepson claim] is considered to positively and clearly include all the elements or steps recited therein as a part of the claimed invention."; Pentec, Inc. v. Graphic Controls Corp., 776 F.2d 309, 315 (Fed.Cir.1985) ("Although a preamble is impliedly admitted to be prior art when a Jepson claim is used, ... the claimed invention consists of the preamble in combination with the improvement.") (citations omitted).

III. DISCUSSION

The Court has very carefully examined the claims and the proposed constructions offered at the claims construction hearing. In addition, the Court has employed the assistance of the independent technical advisor in fully understanding the technology pertinent to the patents in suit. *See* Order re: Duties of the Technical Advisor, dated July 17, 1997. The Court reiterates that the technical advisor has not contributed evidence or rendered conclusions of law. Furthermore, the technical advisor has offered no opinion regarding any legal issues in this action, including opinions on the validity of the patents in suit or whether any of the contested patent claims are infringed by the accused products.

Although the Court permitted extrinsic evidence at the claim construction hearing, the Court construes the claims without consideration of extrinsic evidence except as explicitly noted below. Furthermore, the Court notes that although Xilinx urged the Court to construe portions of the claims of the original '479 patent, the Court construes only the disputed claims of the reexamined B1'479 patent, taking into consideration the claim language and file history of the original patent. What follows is the claim language and the Court's construction thereof for each disputed claim.

The '363 Patent

Patent '363 Claim 11	Construction
A configurable system comprising:	A configurable system is one or more devices connected together that can be configured to perform different functions.
One master configurable logic array;	A configurable logic array ("CLA") is a circuit containing configurable logic elements which can be connected to each other and to inputs and outputs, if any, through a configurable interconnect structure. *See in passim* 1:64-2:46.[2] A configurable logic element ("CLE") is "a combination of devices which are capable of being electrically interconnected by switches operated in response to control bits to perform any one of a plurality of logical functions." 1:59-63. A master CLA is one which "initiates the transfer of the

	information for controlling or configuring the CLA from the non-volatile memory to the master CLA and to the slave CLAs" as described below.
	11:50-53. *See* Fig. 8B.
a plurality of slave configurable logic arrays;	A slave CLA is one which receives configuration data from the master. The system must have more than one slave CLA.
at least one memory;	A memory is a device external to the configurable logic arrays which is capable of storing some or all of the configuration data necessary to configure the CLAs of the system.
said master configurable logic array having means for retrieving data from said at least one memory,	The master CLA must have a structure which is the same as or the equivalent of the structure in the specification which performs the function of retrieving data from the

	memory. The structure disclosed in the specification is: standard circuitry that generates address signals and a control signal; ports to communicate those signals outside of the array; and a port to receive configuration data from a source external to the array. *See* Fig. 8B.
means for first using said data for configuring itself, and	The master CLA must have a structure which is the same as or the equivalent of the structure in the specification which performs the function of using the retrieved data for configuring itself first. A CLA is configured when the combination of configured CLEs and the interconnect structure yields a desired logical output. 6:17-20. A CLE is configured when it is capable of performing a desired logic

	function. 6:41-42. The structure disclosed in the specification which uses the retrieved data for configuring itself first is the RAM of Figure 3A, the RAM of Figure 3B, or the dynamic shift register-static latch of Figure 5 operating in its static latch mode. 5:64-6:2; 7:66-8:4; *see* Figs. 3A, 3B, and 5.
means for passing some of said data to said plurality of slave configurable logic arrays.	The master CLA has a structure which is the same as or the equivalent of the structure in the specification which performs the function of passing some of the retrieved data to the slave CLAs. The structure disclosed in the specification is: standard circuitry that generates a data clock signal; a port to communicate clock signals from the master to the

	the master to the slaves; and a port to communicate data signals from the master to the first slave. Fig. 8B.

FN2. Citations to the patent specification are of the form column: line. For example, 1:64-2:46 refers to column 1 line 64 through column 2 line 46. Unless otherwise noted, all citations to the specification refer to the patent from which the disputed language originates.

Patent '363 Claim 21	Construction
A programmable circuit comprising:	A programmable circuit is a circuit which is capable of being programmed to perform different functions.
a plurality of configurable logic elements,	See discussion of CLE in claim 11 above. The circuit must have more than one CLE.
each configurable logic element having a plurality of input leads and at least one output lead and having	An input lead is a structure that can be used to input a signal to a CLE. Each CLE must have more than one input lead. An output lead is a structure that can be used to output a signal from a CLE. Each CLE must have at least one output lead. *See e.g.* Figs. 2, 3A, 3B, 4A & 7A.
a programming means to cause said configurable	A structure which is the same as or the equivalent of

logic element to perform a selected logic function;	the structure in the specification which performs the function of causing a CLE to perform a selected logic function. The structure disclosed in the specification is the RAM of Figure 3A, the RAM of Figure 3B, or the dynamic shift register-static latch operating in its static latch mode. 5:64-6:2 ("To program the circuitry of a logic element such as shown in Figure 2 selected signals are applied to input leads of the configurable logic element identified as configuration control input leads from a source such as the RAM of FIG. 3A or 3B described above thereby to generate a desired logical function in each of the logic elements"); 7:66-8:4; *see* Figs. 3A, 3B, and 5.

a plurality of input/output ports;	An input/output port is a structure that can be used to input a signal, output a signal, or both, to or from the programmable circuit.
	12:65-68 and Fig. 4A.
a group of interconnect lines;	Interconnect lines are structures, regardless of their length, which conduct data signals from place to place within the integrated circuit device. *See, e.g.*
	Fig. 7A (LL1, LL2, L1, L2).
means for programmably connecting each of said input leads of each of said configurable logic elements to at least one of said interconnect lines;	A structure which is the same as or the equivalent of the structure in the specification which performs the function of programmably connecting CLE input leads to interconnect lines. The structure disclosed in the specification is the RAM of Figure 3A, the RAM of Figure 3B, or the dynamic shift register-static latch of Figure 5

	operating in its static latch mode, and the pass transistors it controls. 5:64-6:2; 6:38-48; 7:40-43; 7:66-8:4; *see* Figs. 3A, 3B, 5, 7B, and 9A-G.
means for programmably connecting said at least one output lead of each of said configurable logic elements to at least one of said interconnect lines;	A structure which is the same as or the equivalent of the structure in the specification which performs the function of programmably connecting CLE output leads to interconnect lines. The structure disclosed in the specification is the RAM of Figure 3A, the RAM of Figure 3B, or the dynamic shift register-static latch of Figure 5 operating in its static latch mode, and the pass transistors it controls. 5:64-6:2; 6:38-48; 7:40-43; 7:66-8:4; *see* Figs. 3A, 3B, 5, 7B, and 9A-G.
means for programmably	A structure which is the same

connecting each of said input/output ports to at least one of said interconnect lines; and	as or the equivalent of the structure in the specification which performs the function of programmably connecting input/output ports to interconnect lines. The structure disclosed in the specification is the RAM of Figure 3A, the RAM of Figure 3B, or the dynamic shift register-static latch of Figure 5 operating in its static latch mode, and the pass transistors it controls. 5:64-6:2; 6:38-48; 7:40-43; 7:66-8:4; *see* Figs. 3A, 3B, 5, 7B, and 9A-G.
means for programmably connecting each one of said interconnect lines to at least one other of said interconnect lines;	A structure which is the same as or the equivalent of the structure in the specification which performs the function of programmably connecting interconnect lines to one another. The structure disclosed in the specification is the RAM of Figure 3A, the RAM of Figure 3B, or

	RAM of Figure 3B, of the dynamic shift register-static latch of Figure 5 operating in its static latch mode, and the pass transistors it controls. 5:64-6:2; 6:38-48; 7:40-43; 7:66-8:4; *see* Figs. 3A, 3B, 5, 7B, and 9A-G.
whereby each of said input leads and each of said at least one output lead of each of said configurable logic elements can be connected directly or indirectly to each of said input/output ports and to each other, and whereby each of said configurable logic elements can be programmed to perform a selected one of a plurality of logic functions, and said configurable logic elements can be connected to each other and to said	Connected directly means that a connection can be made solely via interconnect lines, without passing through a CLE. Connected indirectly means that a connection must pass through a CLE. Patent File History, Amendment in Response to 2nd Office Action, Jan. 13, 1993 at 17-18; Patent File History, Notice of Allowability, Feb. 2, 1993 at 2.

and to said input/output ports in a selectable manner.	

Patent '363 Claim 22	Construction
A programmable circuit as in claim 21	See claim 21.
wherein said programming means of each of said configurable logic elements comprises logic element pass transistors.	See discussion of "programming means" in claim 21 above. The "programming means" element of each CLE must include logic element pass transistors.

Patent '363 Claim 23	Construction
A programmable circuit as in claim 22	See claim 22.
wherein said programming means includes a plurality of memory cells	See discussion of "programming means" in claims 21 and 22 above. The "programming means" element of each CLE must include more than one cell of the RAM of Figure 3A, the RAM of Figure 3B, or the dynamic shift register-static latch of Figure 5 operating in its static latch mode.
and wherein each of said logic element pass transistors is controlled by a corresponding	Each logic element pass transistor must be controlled by one of the cells described

one of said plurality of memory cells.	above.
Patent '363 Claim 24	Construction
A programmable circuit as in claim 23	See claim 23.
in which said plurality of memory cells forms at least part of a shift register,	The memory cells must be arranged so as to form at least part of a shift register. *See* Fig. 5.
control signals being loaded into said memory cells by being transferred through said shift register until each of said signals is properly located in said corresponding one of said memory cells.	Control signals are to be loaded into the shift register by transferring (shifting) those signals from one cell to the next within the shift register until the signals are in their proper locations.
Patent '363 Claim 25	Construction
A programmable circuit as in claim 23	See claim 23.
in which said memory cells can be re-programmed.	The memory cells must be capable of being programmed more than once.
Patent '363 Claim 27	Construction
A programmable circuit as in claim 21	See claim 21.
wherein said means for programmably connecting each of said input leads of	See discussion of "means for programmably connecting" in claim 21 above. Each

each of said configurable logic elements to at least one of said interconnect lines, said means for programmably connecting said at least one output lead of each of said configurable logic elements to at least one of said interconnect lines, said means for programmably connecting each of said input/output ports to at least one of said interconnect lines, and said means for programmably connecting each of said interconnect lines to at least one other of said interconnect lines comprise pass transistors.	of the "means for programmably connecting" elements must include pass transistors.

Patent '363 Claim 28	Construction
A programmable circuit as in claim 27	See claim 27.

wherein said means for programmably connecting	See discussion of "means for programmably connecting" in

further comprises memory means, said memory cells forming at least part of a shift register,	claims 21 and 27 above. The "memory means" element of this claim has the same meaning as the "memory cells" element of claim 23. Each of the "means for programmably connecting" elements must include cells which are arranged to form at least part of a shift register.
wherein each of said pass transistors is controlled by one of said memory cells, and	Each pass transistor must be controlled by one of the cells which form part of the shift register.
wherein said means for programmably connecting further comprises means for transferring said series of signals through said shift register until each of said signals is properly located in an associated one of said memory cells uniquely coupled to one of said pass	See discussion of "means for programmably connecting" in claims 21 and 27 above. Each of the "means for programmably connecting" elements must include a structure which is the same as or the equivalent of the structure in the specification which performs the function of transferring a

transistors.	series of signals through the shift register until each signal is properly located in a cell which is only connected to one pass transistor. The structure disclosed in the specification is the clock signals (theta)1 and (theta)2 and pass transistors 53-1, 53-2, and 53-3 of Figure 5. 6:52-8:9.

Patent '363 Claim 29	Construction
A programmable circuit as in claim 28	See claim 28.
in which said means for programmably connecting includes means for changing the contents of said memory cells, thereby to reconfigure said programmable circuit.	See discussion of "means for programmably connecting" in claims 21, 27, and 28 above. Each of the "means for programmably connecting" elements must include a structure which is the same as or the equivalent of the structure disclosed in the specification which performs the function of changing the

	contents of the cells, thereby reconfiguring the programmable circuit. The structure disclosed in the specification is the dynamic shift register-static latch of Figure 5.

Patent '363 Claim 30	Construction
A programmable circuit comprising:	A programmable circuit is a circuit which is capable of being programmed to perform different functions.
a plurality of logic elements, each logic element having a plurality of input leads and at least one output lead, and having a programming means to cause said logic element to perform a selected logic function;	The circuit must have more than one logic element. A "logic element" is the same as a "configurable logic element", defined in claim 11 above. 1:53-54. The input leads, output leads, and "programming means" elements of this claim have the same meaning as the corresponding elements of claim 21.
a plurality of input/output ports;	The input/output ports, interconnect lines, and "means for programmably connecting"

a group of interconnect lines; means for programmably connecting each of said input leads of each of said logic elements to at least one of said interconnect lines; means for programmably connecting said at least one output lead of each of said logic elements to at least one of said interconnect lines; means for programmably connecting each of said input/output ports to at least one of said interconnect lines; and means for programmably connecting each of said interconnect lines to at least one other of said interconnect lines;	elements of this claim have the same meaning as the corresponding elements of claim 21.

whereby each of said logic elements can be programmed to perform a selected one of a plurality of logic functions, and said logic elements can be connected to each other and to said input/output ports in a selectable manner.	No construction necessary.

Patent '363 Claim 31	Construction
A programmable circuit as in claim 30	See claim 30.
wherein programming means of each of said logic elements comprises transistors.	See discussion of "programming means" in claims 21 and 30 above. The "programming means" element of each logic element must include transistors.

Patent '363 Claim 32	Construction
A programmable circuit as in claim 31	See claim 31.
wherein said programming means includes a plurality of memory cells	See discussion of "programming means" in claims 21, 30, and 31 above. See discussion of "memory cell" in claim 23 above. The "programming means" element must include

	more than one such cell.
and wherein said transistors are controlled by said plurality of memory cells.	The transistors of claim 31 must be controlled by the cells described above.

Patent '363 Claim 33	Construction
A programmable circuit as in claim 32	See claim 32.
in which said plurality of memory cells forms at least part of a shift register,	The memory cells must be arranged so as to form at least part of a shift register. *See* Fig. 5.
control signals being loaded into said memory cells by being transferred through said shift register until each of said signals is properly located in said corresponding one of said memory cells.	Control signals are to be loaded into a shift register by transferring (shifting) those signals from one cell to the next within the shift register until the signals are in their proper locations.

Patent '363 Claim 34	Construction
A programmable circuit as in claim 32	See claim 32.
in which said memory cells can be re-programmed.	The memory cells must be capable of being programmed more than once.

Patent '363 Claim 36	Construction
A programmable circuit as in claim 30	See claim 30.

wherein said means for programmably connecting comprise transistors.	See discussion of "means for programmably connecting" in claims 21 and 30 above. Each "means for programmably connecting" element must include transistors.

Patent '363 Claim 37	Construction
A programmable circuit as in claim 36	See claim 36.
wherein said means for programmably connecting further comprise memory cells, said memory cells forming at least part of a shift register,	See discussion of "means for programmably connecting" in claims 21, 30 and 36 above. The memory cells element of this claim has the same meaning as the corresponding element of claim 23. Each of the "means for programmably connecting" elements must include cells which are arranged so as to form at least part of a shift register.
wherein said transistors are controlled by said memory cells, and	The transistors must be controlled by the cells described above.
wherein said means	See discussion of

for programmably connecting further comprises means for transferring said series of signals through said shift register until each of said signals is properly located in an associated one of said memory cells.	"means for programmably connecting" in claims 21, 30 and 36 above. Each "means for programmably connecting" element must include a structure which is the same as or the equivalent of the structure in the specification which performs the function of transferring a series of signals through the shift register until each signal is properly located in a cell. The structure disclosed in the specification is the clock signals (theta)1 and (theta)2 and pass transistors 53-1, 53-2, and 53-3 of Figure 5. 6:52-8:9.
Patent '363 Claim 38	Construction
A programmable circuit as in claim 37	See claim 37.
in which said means for programmably connecting includes means for changing the contents of said	See discussion of "means for programmably connecting" in claims 21, 30, 36, and 37 above. Each of the

memory cells, thereby to reconfigure said programmable circuit.	"means for programmably connecting" elements must include a structure which is the same as or the equivalent of the structure disclosed in the specification which performs the function of changing the contents of the cells, thereby reconfiguring the programmable circuit. The structure disclosed in the specification is the dynamic shift register-static latch of Figure 5.

Patent '363 Claim 57	Construction
A configurable logic array chip comprising:	A CLA chip is a CLA as defined in claim 11 above, implemented in a single integrated circuit.
a plurality of storage cells for holding configuration information, said configuration information configuring said configurable logic array chip; and	A storage cell is a structure that is capable of retaining a single bit of binary data. 6:31. The CLA chip must have more than one storage cell which is able to retain configuration information for the CLA chip

	the CLA chip. Although the specification identifies a shift register-static latch as a particular type of storage cell that may be used, the structural language of this claim does not limit the type of storage cell that is claimed.
means for selecting configuration information from a device external to said configurable logic array chip and initiating the transfer of said configuration information into said storage cells.	A structure which is the same as or the equivalent of the structure in the specification which performs the function of selecting configuration information from a device external to the CLA chip and initiating the transfer of that information to the storage cells described above. The structure disclosed in the specification is: standard circuitry that generates address signals and a control signal; ports to communicate those signals outside of the

	chip; and a port to receive configuration data from an external source. Fig. 8B.

Patent '363 Claim 58	Construction
A configurable logic array chip as in claim 57 in which said means for causing said configuration information to be loaded causes said configuration information to be loaded in response to said system being powered up.	See claim 57. See discussion of "means for selecting configuration information and initiating transfer" in claim 57 above. The "means for selecting configuration information and initiating transfer" element must include a structure which is the same as or the equivalent of the structure in the specification which performs the function of causing the configuration information to be loaded in response to the system being powered up. The structure disclosed in the specification is: standard circuitry that

	generates address signals and a control signal; ports to communicate those signals outside of the chip; and a port to receive configuration data from an external source.
	11:43-12:22; Fig. 8B.

Patent '363 Claim 59	Construction
A configurable logic array	See claim 57.
chip as in claim 57	
in which said means for causing said configuration information to be loaded causes said configuration information to be loaded in response to said system being reset.	See discussion of "means for selecting configuration information and initiating transfer" in claim 57 above. The "means for selecting configuration information and initiating transfer" element must include a structure which is the same as or the equivalent of the structure in the specification which performs the function of causing the configuration information to be loaded in response to the

	response to the system being reset. The structure disclosed in the specification is: standard circuitry that generates address signals and a control signal; ports to communicate those signals outside of the chip; and a port to receive configuration data from an external source.
	11:43-12:22; Fig. 8B.

Patent '363 Claim 81	Construction
A configurable system comprising:	A configurable system is one or more devices connected together that can be configured to perform different functions.
one master configurable logic array;	The master CLA element of this claim has the same meaning as the corresponding element of claim 11.
at least one slave configurable logic array;	The slave CLA element of this claim has the same meaning as the corresponding element of claim 11. The system must include at least one slave

	CLA.
at least one memory; said master configurable logic array having means for retrieving data from said at least one memory, means for first using said data for configuring itself, and means for passing some of said data to said at least one slave configurable logic array.	The memory, "means for retrieving," "means for using," and "means for passing" elements of this claim have the same meaning as the corresponding elements of claim 11.

The '487 Patent	
Patent '487 Claim 1	Construction
A configurable logic array comprising:	A configurable logic array ("CLA") is a circuit containing configurable logic elements which can be connected to each other and to inputs and outputs, if any, through a configurable interconnect structure. *See* *in passim* 1:54-58.
a plurality of configurable logic elements (CLEs),	A configurable logic element ("CLE") is "a combination of devices which are capable of

	being electrically interconnected by switches operated in response to control bits to [per]form any one of a plurality of logical functions." 1:14-18. The CLA must have more than one CLE.
each CLE having at least one input lead and at least one output lead;	An input lead is a structure that can be used to input a signal to a CLE. Each CLE must have at least one input lead. An output lead is a structure that can be used to output a signal from a CLE. Each CLE must have at least one output lead. *See e.g.* Figs. 2, 3A, 3B, 4A & 7A.
a general interconnect structure comprising a plurality of general interconnect leads and a plurality of programmable general interconnect junctions for interconnecting selected	A general interconnect structure is defined using the following definitions: Interconnect leads are structures, regardless of their length, which conduct

ones of said general interconnect leads;	data signals from place to place within the integrated circuit device. *See* Fig. 4A. "The leads in Fig. 4A which are neither input leads nor output leads are all called general interconnect leads.. . ." 6:12-14. Interconnect junctions are structures which connect one interconnect lead to another interconnect lead. *See* 1:64-66 and Fig. 4A. "An access junction is a programmable junction for connecting a general interconnect lead to an input lead of a CLE or for connecting an output lead of a CLE to a general interconnect lead." 1:66-2:2. "[T]he junctions in Fig. 4A which are not access

	junctions for input and output leads are called general interconnect junctions." 6:14-16. The general interconnect structure must have more than one general interconnect lead and more than one general interconnect junction.
one or more input access junctions for each input lead, each of said input access junctions being programmable for connecting a corresponding general interconnect lead to said input lead;	See discussion of "access junction" above. The CLA must have at least one input access junction for each input lead of each CLE.
one or more output access junctions for each output lead, each of said output access junctions being programmable for connecting said output lead to a corresponding general interconnect lead;	See discussion of "access junction" above. The CLA must have at least one output access junction for each output lead of each CLE.
means for programming said general interconnect	A structure which is the same as or the equivalent of

junctions	the
and said access	structure in the
junctions to	specification
provide an electrical path	which performs the function of
connecting one of said at	programming general
least one output lead of one	interconnect junctions and
of said plurality of CLEs to	access junctions so as to
one of said at least one input	provide an electrical path
lead of one of said plurality	from an output lead of one CLE
of CLEs, said electrical path	to the input lead of another
containing two access	CLE which contains two access
junctions and at least a	junctions and at least a
portion of one of said general	portion of a general
interconnect leads; and	interconnect lead. The
	structure disclosed in the
	specification is a memory, or
	a programming register. 6:48-54,
	58-63. *See also* Figs. 3a
	and 3b (RAM) and Fig. 5 (shift
	register (static latch)).
at least one special	A special interconnection is
interconnection circuit which	one that connects an output
permits a selected output lead	lead of one CLE to the input
of one of said CLEs to be	lead of another CLE, but that
connected to a selected input	does not contain any general

lead of another CLE, said special interconnection circuit not containing any portion of the general interconnect leads or any junction in the general interconnect structure.	interconnect leads or any junction in the general interconnect structure.
	As defined above, general interconnect leads are all leads except input leads and output leads. *See above*.
	The junctions that are in the general interconnect structure (referred to above as "general interconnect junctions") are those that are not access junctions for input leads or output leads. *See above*. Therefore, access junctions that connect general interconnect leads to input leads or output leads are not in the general interconnect structure.

Patent '487 Claim 3	Construction
A configurable logic array as in claim 1	See claim 1.
wherein said special interconnection	See discussion of special interconnection

circuit comprises a lead connected to said selected output lead and a pass transistor for each input lead of said selected CLE connected between said lead connected to said selected output lead and said corresponding input lead.	circuit in claim 1 above. The special interconnection circuit must include: (1) a lead connected to a selected output lead of a CLE ("the special lead"); and (2) one pass transistor corresponding to each input lead of another CLE. Each pass transistor is able to connect between its corresponding input lead and the special lead.

The B1'479 Patent [3]	
Patent B1'479 Claim 1	Construction
A reprogrammable logic array device comprising:	A reprogrammable logic array device is a device that can be programmed to perform various functions and that can be programmed more than once.
means forming a first programmable AND array	This is not a means-plus-function claim element. The detailed recitation of structure included in this claim language (see below) is sufficient to rebut the presumption triggered by

	presumption triggered by the use of the word "means." The claim language does not link the term "means" to any function, as "forming a first programmable AND array" fails to define a function. Rather, "forming a first programmable AND array" describes a structure. Therefore, this element is not construed according to s. 112 para. 6. The memory cells (described below) are arranged so as to form a programmable AND array. An AND array is more than one AND gate.
having a plurality of first static, reprogrammable logic memory cells	As this is a structural claim, the logic memory cells may be of any type as long as they are static and reprogrammable.
arranged in addressable rows and columns	The memory cells are physically arranged on the device in rows and columns. Each row must be addressable

	and each column must be
	addressable.
and which can be individually	The ability must exist to
programmed to contain logic	change the contents of one
data;	memory cell without changing
	the contents of any other
	cell. This phrase does not
	require the ability to program
	one memory cell at a time.
	11:24-27.
second static, reprogrammable	The second static,
architecture control memory	reprogrammable memory cells
cells, said second static	must be of the same type as
memory cells being of the same	the first static,
type as said first static	reprogrammable memory cells,
memory cells;	and there must be more than
	one of such cells.
first input circuit means for	A structure which is the same
receiving a first input signal	as or the equivalent of the
and for developing a first	structure in the specification
buffered signal corresponding	which performs the function of
thereto;	receiving a first input signal
	and developing a corresponding
	first buffered signal. The
	structure disclosed in the

	specification is the entire input circuit shown in Figure 9. 7:12-48.
first row driver means responsive to said first buffered signal and operative to interrogate a particular row of said memory cells and to cause said first AND array to output signals corresponding to the data contained therein;	A structure which is the same as or the equivalent of the structure in the specification which is responsive to the first buffered signal and which performs the function of interrogating a particular row of memory cells and causing the first AND array to output signals corresponding to the data contained therein. To interrogate means "to give or send out a signal to (as a transponder or computer) for triggering an appropriate response." *Webster's New Collegiate Dictionary,* 599 (1981). The structure disclosed in the specification is the logic gates G11 and G12 and the inverter formed by T13, T14 and T15 in

	Figure 10. 7:49-8:2. The term "interrogate" does not require that the row driver apply a signal directly to the memory cells. Fig. 6A.
first sensing means for sensing the signals output by said first AND array and for developing a corresponding first data signal which is the logical OR of the signals output by said first AND array;	A structure which is the same as or the equivalent of the structure in the specification which performs the function of sensing the signals output by the first AND array and developing a corresponding first data signal which is the logical OR of the signals output by the first AND array. The structure disclosed in the specification is the OR/NOR Gate, Sense Amplifier of Figure 12. 8:31-55.
first signal storage means for receiving and temporarily storing said first data signal;	A structure which is the same as or the equivalent of the structure in the specification which performs the function of receiving and temporarily storing the first data

	storing the first data signal. The structure disclosed in the specification is the D Flip-Flop of Figure 13. 8:56-9:8.
first output terminal means; and	A structure which is the same as or the equivalent of the structure in the specification which performs the function of providing an output on a terminal. The structure disclosed in the specification is the inverter formed by transistors P3 and N3, the inverter formed by P4 and N5, and the I/O pad, all of Figure 16. 9:57-10:11.
first switching means responsive to a control signal coupled to and responsive to contents of said second memory cells, said first switching means operative to couple either said first data signal or a data signal temporarily stored in said first signal	A structure which is the same as or the equivalent of the structure in the specification which performs the function of coupling either the first data signal or a data signal temporarily stored in the first signal storage means to the first output terminal

storage means to said first output terminal means.	means in response to a control signal. The structure disclosed in the specification is the output multiplexer (OMUX) of Figure 14. 9:9-44.

FN3. The Reexamination Certificate for this patent only includes those paragraphs of the specification affected by amendment. Therefore, citations to the specification for this patent refer to the specification of the original '479 patent unless otherwise noted.

Patent B1'479 Claim 2	Construction
A programmable logic array	See claim 1.
device as recited in claim 1	
and further comprising second row driver means responsive to a signal input thereto and operative to interrogate another particular row of said memory cells and to cause said first AND array to output other data signals corresponding to the data contained therein to said first sensing means for developing another data signal.	The device must include a "second row driver means" element. The "second row driver means" element of this claim is an additional structure which has the same meaning as the "first row driver means" element of claim 1. The "second row driver means" element must interrogate a different row of memory cells than the "first row driver means" element so as to output another data signal to the "first

	signal to the "first sensing means" element.
Patent B1'479 Claim 5	Construction
A programmable logic array device as recited in claim 2	See claim 2.
wherein said first switching means is also operative to couple either the data signal output by said first sensing means or a data signal temporarily stored in said first signal storage means into said second row driver means.	See discussion of "first switching means" in claim 1 above. A structure which is the same as or the equivalent of the structure in the specification which performs the function of the "first switching means" above, and, in addition, the function of coupling either the data signal output by the first sensing means or a data signal temporarily stored in the first signal storage means into the second row driver means. The structure disclosed in the specification is the OMUX of Figure 14 and the feedback multiplexer ("FMUX") of Figure

	15. 9:9-19, 45-56.
Patent B1'479 Claim 6	Construction
A programmable logic array device as recited in claim 5 wherein said first switching means includes an output multiplexing device for connecting either the output of said first sensing means or the temporarily stored first data signal contained in said first storage means to said first output terminal means.	See claim 5.
Patent B1'479 Claim 7	Construction
A programmable logic array device as recited in claim 6 wherein said first switching means further includes a feedback multiplexing circuit operative to couple either the output of said first sensing means, the temporarily stored first data signal, or the data appearing at said first	See claim 6.

appearing at said first output terminal means to said second row driver means.	

Patent B1'479 Claim 19	Construction
A programmable logic array device as recited in claim 1	See claim 1.
and further comprising:	
means forming a second programmable AND array having a plurality of memory cells arranged in addressable rows and columns and which can be individually programmed to contain logic data; second input circuit means for receiving a second input signal and for developing a second buffered signal corresponding thereto; second row driver means responsive to said second buffered signal and operative to interrogate a first particular row of said second AND array memory cells and to	The "second programmable AND array", "second input circuit means", "second row driver means", "second sensing means", "second signal storage means", "second output terminal means", and "second switching means" elements of this claim all have the same meaning as the corresponding elements of claim 1. The device must include a second one of each of these elements.

cause said second AND array to output signals corresponding to the data contained therein; second sensing means for sensing the signals output by said second AND array and for developing a corresponding second data signal which is the logical OR of the signals output by said second AND array; second signal storage means for receiving and temporarily storing said second data signal; second output terminal means; and second switching means responsive to a control signal and operative to couple either said second data signal or a data signal temporarily stored in said second signal storage means to said second output terminal means.

Patent B1'479 Claim 20	Construction
A programmable logic array	See claim 19.
device as recited in claim 19	
and further comprising third row driver means responsive to a signal input thereto and operative to interrogate another particular row of said memory cells in said second AND array and to cause said second AND array to output other data signals corresponding to the data contained therein to said second sensing means for developing another data signal.	The device must include a "third row driver means" element. The "third row driver means" element of this claim is an additional structure which has the same meaning as the "first row driver means" element of claim 1. The "third row driver means" element must interrogate a different row of memory cells in the second AND array than the "second row driver means" element so as to output another data signal to the "second sensing means" element.

Patent B1'479 Claim 21	Construction
A programmable logic array	See claim 20.
device as recited in claim 20	
wherein said first switching	See discussion of "first

means is also operative to couple either the data signal output by said first sensing means or a data signal temporarily stored in said first signal storage means into said third row driver means.	switching means" in claim 1 above. A structure which is the same as or the equivalent of the structure in the specification which performs the function of the "first switching means" element above, and, in addition, the function of coupling either the output of the first sensing means or a data signal temporarily stored in the first signal storage means to the third row driver means. The structure disclosed in the specification is the OMUX of Figure 14 and the FMUX of Figure 15.

Patent B1'479 Claim 36	Construction
A reprogrammable logic array device comprising:	A reprogrammable logic array device is a device that can be programmed to perform various functions and that can be programmed more than once.
	The "first programmable

	The "first programmable AND
means forming a first	array" element of this claim
programmable AND array having	has the same meaning as the
a plurality of static,	corresponding element of claim
reprogrammable logic memory	1.
cells arranged in addressable	
rows and columns and which can	
be individually programmed to	
contain logic data;	
a static programmable	The device must include a
architecture control memory	static programmable
cell;	architecture control memory
	cell.
first input circuit means for	The "first input circuit
receiving a first input signal	means", "first row driver
and for developing a first	means", and "first sensing
buffered signal corresponding	means" elements of this claim
thereto;	all have the same meaning as
first row driver means	the corresponding elements of
responsive to said first	claim 1.
buffered signal and operative	
to interrogate a particular	
row of said memory cells and	
to cause said first AND array	

to output signals corresponding to the data contained therein; first sensing means for sensing the signals output by said first AND array and for developing a corresponding first data signal which is the logical OR of the signals output by said first AND array;	
first signal storage means for receiving and temporarily storing said first data signal, operation of said signal storage means controlled by at least a first control signal, said first control signal derived from at least one of said input signals based on contents of at least one signal storage memory cell, said signal storage memory cell being a static, reprogrammable memory	A structure which is the same as or the equivalent of the structure in the specification which performs the function of receiving and temporarily storing a first data signal and which is controlled by a first control signal. The control signal must be derived from at least one input signal based on the contents of at least one static reprogrammable memory cell. The structure disclosed in the

cell;	specification is the D Flip-Flop of Figure 13. Control signals are portrayed in Figure 13 as SET-bar, RESET-bar, CLK, and CLK-bar.
first output terminal means; and first switching means responsive to a second control signal coupled to and responsive to contents of said architecture control memory cell, said first switching means operative to couple either said first data signal or a data signal temporarily stored in said first signal storage means to said first output terminal means.	The "first output terminal means" and "first switching means" elements of this claim have the same meaning as the corresponding elements of claim 1.

Patent B1'479 Claim 37	Construction
A programmable logic array device as recited in claim 36 wherein said signal storage means is a D flip flop having a reset signal line coupled to said first control	See claim 36. See discussion of "signal storage means" in claim 36 above. The "signal storage means" element

signal.	must be a D Flip-Flop which has a reset signal line coupled to the first control signal.
Patent B1'479 Claim 38	Construction
A programmable logic array device as recited in claim 37	See claim 37.
wherein said first control signal is a logical function of at least one of said inputs, said logical function selected from the group consisting of invereting [sic], or non-inverting buffered.	The first control signal must be either an inverted, buffered input signal or a non-inverted, buffered input signal.
Patent B1'479 Claim 39	Construction
A programmable logic array device as recited in claim 37	See claim 37.
wherein a clock input to said signal storage means is coupled to one of said input signals.	The "signal storage means" element must include a clock input that is connected to one of the input signals.
Patent B1'479 Claim 40	Construction
A programmable logic array device as recited in claim 37	See claim 37.
wherein a clock	The D Flip-Flop must

input to said flip flop is coupled to one of said input signals.	include a clock input that is connected to one of the input signals.

Patent B1'479 Claim 41	Construction
A programmable logic array device as recited in claim 36	See claim 36.
wherein said output terminal means comprises an output circuit that selectively couples logic output to an output pin, said output circuit coupled to and controlled by a product term from said AND array.	See discussion of "output terminal means" in claim 36 above. The "output terminal means" element must include an output circuit that either connects or does not connect the logic output to an output pin. A product term from the AND array must be connected to the output circuit and determine whether the circuit connects or does not connect the logic output to an output pin.

Patent B1'479 Claim 42	Construction
A programmable logic array device as recited in claim 36	See claim 36.
wherein said output terminal means is adapted to	See discussion of "output terminal means" in

	claim 36
alternately receive input from an input/output pin.	above. A structure which is the same as or the equivalent of the structure in the specification which performs the function of the "output terminal means" above, and, in addition, alternately receives input from an input/output pin. The structure disclosed in the specification is all of Figure 16, except the "Input
	Circuit (Fig.9)".

Patent B1'479 Claim 43	Construction
A programmable logic array	See claim 36.
device as recited in claim 36	
further comprising a feedback circuit adapted to selectively feed back to an AND input either said first data signal or said data signal temporarily stored.	The device must include a feedback circuit that is capable of connecting either the first data signal or the temporarily stored data signal to an AND input.

Patent B1'479 Claim 48	Construction
A programmable logic array device comprising:	A programmable logic array device is a device that can be programmed to

	programmed to perform various functions.
means forming a first programmable AND array having a plurality of logic memory cells arranged in addressable rows and columns and which can be individually programmed to contain logic data;	The "first programmable AND array" element of this claim has the same meaning as the corresponding element of claim 1 with the following exception: the AND array has memory cells that are described as "logic memory cells" rather than "first static reprogrammable logic memory cells." The memory cells in this claim do not need to be reprogrammable or static.
first input circuit means for receiving a first input signal and for developing a first buffered signal corresponding thereto; first row driver means responsive to said first buffered signal and operative to interrogate a	The "first input circuit means", "first row driver means", "first sensing means", "first signal storage means", and "first output terminal means" elements of this claim all have the same meanings as the corresponding elements of claim 1.

particular row of said memory cells and to cause said first AND array to output signals corresponding to the data contained therein;	
first sensing means for sensing the signals output by said first AND array and for developing a corresponding first data signal which is the logical OR of the signals output by said first AND array;	
first signal storage means for receiving and temporarily storing said first data signal;	
first output terminal means;	
second row driver means responsive to a signal input thereto and operative to interrogate another particular row of said memory cells and to cause said first AND array to output other data signals corresponding to the	The structure corresponding to the "second row driver means" element of this claim has the same meaning as the corresponding element of claim 2.

corresponding to the data contained therein to said first sensing means for developing another data signal; and	
first switching means responsive to a control signal and operative to couple either said first data signal or a data signal temporarily stored in said first signal storage means to said first output terminal means and also operative to couple either the data signal output by said first sensing means or a data signal temporarily stored in said first signal storage means into said second row driver means, said first switching means further comprising:	A structure which is the same as or the equivalent of the structure in the specification which performs the function of connecting either the first data signal or a data signal temporarily stored in the signal storage means to the output terminal means, and also connecting either that same first data signal or that same data signal temporarily stored in the signal storage means to the second row driver means. The structure disclosed in the specification is the OMUX of Figure 14 and the FMUX of Figure 15.
i) an output multiplexing device for connecting either	The first switching means must include a multiplexing device

the output of said first sensing means or the temporarily stored first data signal contained in said first signal storage means to said first output terminal means;	that connects either a data signal from the sensing means or a data signal temporarily stored in the signal storage means to the output terminal means.
and	
ii) a feedback multiplexing circuit operative to couple either the output of said first sensing means, the temporarily stored first data signal, or the data appearing at said first output terminal means to said second row driver means.	The first switching means must include a feedback multiplexing circuit that connects either a data signal from the sensing means, a data signal temporarily stored in the signal storage means, or the data signal that appears at the output terminal means to the second row driver means.

Patent B1'479 Claim 49	Construction
A programmable logic device as recited in claim 48	See claim 48.
wherein said feedback multiplexing circuit is adapted to feed back a selected signal to logic	See discussion of feedback multiplexing circuit in claim 48 above. The feedback multiplexing circuit

inputs without applying said selected signal to an output pin of said programmable logic device.	must be able to connect a selected signal to the second row driver means without connecting that signal to an output pin.

Patent B1'479 Claim 55	Construction
A reprogrammable logic array device comprising:	A reprogrammable logic array device is a device that can be programmed to perform various functions and that can be programmed more than once.
means forming a first programmable AND array having a plurality of logic memory cells arranged in addressable rows and columns and which can be individually programmed to contain logic data,	The "first programmable AND array" element of this claim has the same meaning as the corresponding element of claim 48.
wherein each of said plurality of memory cells comprise first and second MOS transistors coupled in series between first and second nodes, one of said first or second	The first programmable AND array must have memory cells made up of two MOS transistors connected in series. One of the transistors must include a gate that holds an

	electrical
transistors comprising a gate	charge for a substantial
having a substantial time-invariant	length of time. The
charge thereon based	electrical charge must be
on a programming input,	based on a programming input.
whereby said first and second	The two transistors must
transistors cooperate to	cooperate to produce a logic
produce said logic cell data	signal at an output node.
at an output node;	
first input circuit means for	The "first input circuit
receiving a first input signal	means", "first row driver
and for developing a first	means", "first sensing means",
buffered signal corresponding	"first signal storage means",
thereto;	and "first output terminal
first row driver means	means" elements of this claim
responsive to said first	have the same meanings as the
buffered signal and operative	corresponding elements of
to interrogate a particular	claim 1.
row of said memory cells and	
to cause said first AND array	
to output signals	
corresponding to the data	
continued therein based on	
said logic cell data;	

first sensing means for sensing the signals output by said first AND array and for developing a corresponding first data signal which is the logical OR of the signals output by said first AND array;	
first signal storage means for receiving and temporarily storing said first data signal;	
first output terminal means;	
and	
first switching means responsive to a control signal and operative to couple either said first data signal or a data signal temporarily stored in said first signal storage means to said first output terminal means.	A structure which is the same as or the equivalent of the structure in the specification which performs the function of connecting either a data signal from the sensing means or a data signal temporarily stored in the signal storage means to the output terminal means in response to a control signal. The structure disclosed in the

	disclosed in the specification
	is the OMUX of Figure 14.

Patent B1'479 Claim 57	Construction
A reprogrammable logic array device for operation in a logic system comprising:	A reprogrammable logic array device is a device that can be programmed to perform various functions and that can be programmed more than once.
means forming a first programmable AND array having a plurality of logic memory cells arranged in addressable rows and columns and which can be individually programmed to contain logic data;	The "first programmable AND array" element of this claim has the same meaning as the corresponding element of claim 48.
first input circuit means for receiving a first input signal and for developing a first buffered signal corresponding thereto;	The "first input circuit means", "first row driver means", "first sensing means", "first signal storage means", and "first output terminal means" elements of this claim have the same meanings as the corresponding elements of claim 1.
first row driver means responsive to said first buffered signal and operative to interrogate to a	

particular row of said memory cells and to cause said first AND array to output signals corresponding to the data contained therein;

first sensing means for sensing the signals output by said first AND array and for developing a corresponding first data signal which is the logical OR of the signals output by said first AND array;

first signal storage means for receiving and temporarily storing said first data signal;

first output terminal means;	
first switching means responsive to a control signal and operative to couple either said first data signal or a data signal temporarily stored in said first signal storage means to said first output terminal means;	The "first switching means" element of this claim has the same meaning as the corresponding element of claim 55.

and means in said system for modifying a programmed state of selected memory cells in real time based on selected conditions, whereby said programmable logic array is adaptive to said system.	A structure which is the same as or the equivalent of the structure in the specification which performs the function of modifying a programmed state of selected memory cells in real time based on selected conditions. The structure disclosed in the specification is the programming circuitry portrayed in Figures 17, 18, 19, 20, 21, 22A and 22B.
	10:20-15:7.
Patent B1'479 Claim 58	Construction
A reprogrammable logic array device comprising:	A reprogrammable logic array device is a device that can be programmed to perform various functions and that can be programmed more than once.
means forming a first programmable AND array having a plurality of logic first reprogrammable memory cells arranged in addressable	The "first programmable AND array" element of this claim has the same meaning as the corresponding element of claim 1 with the following

rows and columns and which can be individually programmed to contain logic data;	exception: the AND array has memory cells that are described as "logic first reprogrammable memory cells" rather than "first static reprogrammable logic memory cells." The memory cells in this claim do not need to be static.
second reprogrammable architecture control memory cells;	The second reprogrammable memory cells must control the routing of signals through the device. 9:22-25, 51-54.
first input circuit means for receiving at least first and second input signals from respective first and second input pins, and for developing buffered signals corresponding thereto;	A structure which is the same as or the equivalent of the structure in the specification which performs the function of receiving at least first and second input signals from first and second input pins and developing corresponding buffered signals. The structure disclosed in the specification is the

	entire input circuit shown in Figure 9. 7:12-48.
first row driver means responsive to said buffered signals and operative to interrogate a particular row of said memory cells and to cause said first AND array to output signals corresponding to the data contained therein;	A structure which is the same as or the equivalent of the structure in the specification which is responsive to the first and second buffered signals and which performs the function of interrogating a particular row of the memory cells and causing the first AND array to output signals corresponding to the data contained therein. To interrogate means "to give or send out a signal to (as a transponder or computer) for triggering an appropriate response." *Webster's New Collegiate Dictionary*, 599 (1981). The structure disclosed in the specification is the logic gates G11 and G12 and the inverter

	and the inverter formed by T13, T14 and T15 in Figure 10. 7:49-8:2. The term "interrogate" does not require that the row driver apply a signal directly to the memory cells. Fig. 6A.
first sensing means for sensing the signals output by said first AND array and for developing a corresponding first data signal which is the logical OR of the signals output by said first AND array;	This element has the same meaning as the corresponding element of claim 1 above.
first signal storage means for receiving and temporarily storing said first signal, said first signal storage means comprising a clock input, said clock input coupled to said first input pin;	A structure which is the same as or the equivalent of the structure in the specification which performs the function of receiving and temporarily storing the first data signal. The structure disclosed in the specification is the D Flip-Flop of Figure 13. 8:56-9:8. The "first signal storage

	means" element must include a clock input which is connected to the first input pin of the input circuit means.
first output terminal means; and first switching means responsive to a control signal coupled to and responsive to contents of said second memory cells, said first switching means operative to couple either said first data signal or a data signal temporarily stored in said first signal storage means to said first output terminal means.	The "first output terminal means" and "first switching means" elements of this claim have the same meanings as the corresponding elements of claim 1.

Patent B1'479 Claim 59	Construction
A programmable logic array device comprising:	A programmable logic array device is a device that can be programmed to perform various functions.
means forming a first programmable AND array having a plurality of first logic	The "first programmable AND array" element of this claim has the same meaning as the

reprogrammable memory cells arranged in addressable rows and columns and which can be individually programmed to contain logic data;	corresponding element of claim 58.
second reprogrammable architecture control memory cells, said second memory cells comprising at least a storage selection memory cell, a feedback control memory cell, and an output control memory cell;	The second reprogrammable architecture control memory cells must control the routing of signals through the device. 9:22-25, 51-54. The second set of memory cells must include at least a storage selection memory cell, a feedback control memory cell, and an output control memory cell. A storage selection memory cell contains data that determines whether to supply a data signal from the sensing means or a temporarily stored data signal to the output terminal means. *See* discussion of "first

	switching means" below. A feedback control memory cell contains data that determines whether or not to supply a data signal from the sensing means to the AND array. *See* discussion of "feedback switching means" below. An output control memory cell contains data that determines whether or not to supply an output signal to an output pin. *See* discussion of "first output terminal means" below.
first input circuit means for receiving a first input signal and for developing a first buffered signal corresponding thereto; first row driver means responsive to said first	The "first input circuit means", "first row driver means", "first sensing means", and "first signal storage means" elements of this claim have the same meanings as the corresponding elements of

buffered signal and operative to interrogate a particular row of said memory cells and to cause said first AND array to output signals corresponding to the data contained therein;	claim 1.
first sensing means for sensing the signals output by said first AND array and for developing a corresponding first data signal which is the logical OR of the signals output by said first AND array;	
first signal storage means for receiving and temporarily storing said first data signal;	
first output terminal means, said output terminal means comprising means selecting whether an output signal is to be supplied to an output pin based on contents of said output control memory	A structure which is the same as or the equivalent of the structure in the specification which performs the function of providing an output on a terminal, and selecting whether or not to

cell;	supply the output signal to an output pin based on the contents of an output control memory cell. The structure disclosed in the specification is the entire circuit of Figure 16 except the "Input Circuit (Figure 9)". 9:57-10:11.
first switching means responsive to a control signal coupled to and responsive to contents of said storage selection memory cell, said first switching means operative to couple either said first data signal or a data signal temporarily stored in said first signal storage means to said first output terminal means;	A structure which is the same as or the equivalent of the structure in the specification which performs the function of connecting either a first data signal from the sensing means or a data signal temporarily stored in the signal storage means to the output terminal means, and performing that function based on the contents of a storage selection memory cell. The structure disclosed in the specification is the OMUX of Figure 14.

	9:9-44.
and feedback switching means responsive to contents of said feedback control memory cell and operative to couple or not couple said first data signal to said AND array.	A structure which is the same as or the equivalent of the structure in the specification which performs the function of connecting the data signal from the sensing means to the AND array, and selecting whether or not to connect the data signal based on the contents of a feedback control memory cell. The structure disclosed in the specification is the FMUX of Figure 15.

The '421 Patent	
Patent '421 Claim 1	Construction
In a programmable logic device including a plurality of electronic logic circuit means each having data input, output, and input/output terminals, and having feedback paths to said data input terminals, and being responsive to input data signal	This is a "Jepson" claim in that it begins with a preamble that recites an old device, continues with a transition that states "an improved programmable means comprising" and concludes with the body of the claim as the statement of the new improvements upon the

signals received at said data input and input/output terminals and operative to perform particular logic functions and to generate commensurate circuit means output signals, and

old device.

The limitations imposed by the preamble include "electronic logic circuit means" elements which perform the function of responding to input data signals and operating to perform logic functions and to generate output signals. This claim covers a structure which is the same as or the equivalent of the structure in the specification which performs the function described above. The structure disclosed in the specification is Figure 8A (except elements 80, 82 and 88), or Figure 8B (except the D-F.F. (FIG.13) elements, the OMUX (FIG.14) elements, and the two columns of elements to the far left of the Figure, one labeled "Input Circuit (Fig.9)" and the other labeled "Row Driver (Fig. 10)"), which by reference incorporate Figures 9-12,

	and 16. 3:33-38.

The structures of Figure 8A and 8B include a programmable AND array, an OR/NOR array, a feedback row driver, an I/O driver and input circuit, and a feedback multiplexer. 7:3-7.

The device must include more than one "electronic logic circuit means" element, and each such element must have data input terminals, data output terminals, data input/output terminals, and signal feedback paths to the data input terminals.

Data input terminals are structures that can be used to input a signal to the "electronic logic circuit means" elements.

Data output terminals are structures that can be used to output a signal from the "electronic logic circuit means" elements.

	Data input/output terminals are structures that can be used to input a signal, output a signal, or both, to or from the "electronic logic circuit means" elements. Signal feedback paths are circuitry that a signal goes through as it passes back to a data input terminal.
programmable means for configuring the architecture of said logic device so that each said logic circuit means is operative to perform a particular logic function, an improved programmable means comprising:	The "programmable means" of the preamble is a means-plus-function element. Written in Jepson-style, this claim is for an improved programmable means, which performs the function of configuring the architecture of the device so that each "electronic logic circuit means" element performs a particular logic function. The body of the claim defines the improved programmable means that performs this function.
a plurality of architecture	The programmable means

control circuits each including:	includes more than one architecture control circuit as further described in the claim elements that follow.
a reprogrammable memory device having an output terminal and having a programming potential input terminal by which said memory device may be programmed to either a first state to generate a logic signal of a first level or programmed to a second state to generate a logic signal of a second level at said memory device output terminal;	Each architecture control circuit must have a reprogrammable memory device having an output terminal and a programming potential input terminal. An output terminal is a structure that can be used to output a signal from the reprogrammable memory device. "Programming potential" is a high voltage (for instance 21 volts in a circuit that normally operates at between 0 and 5 volts) that is required to program the memory device. 4:35-45; 10:36-62. A "programming potential input terminal" is a terminal connecting the programming potential to the memory

	device. The requirement that the reprogrammable memory device have a programming potential input terminal limits the range of covered devices to those that require a programming potential. SRAM memory cells do not require a programming potential as that term is defined in the specification.
programming means responsive to input program data signals and to an address signal corresponding to said reprogrammable memory device and operative to program said memory device by applying a programming potential to said memory device programming potential input terminal;	A structure which is the same as or the equivalent of the structure in the specification which performs the function of programming the memory device by applying a programming potential to the programming potential input terminal. The structure disclosed in the specification is: transistor N1 whose gate is connected to line 100 of Figure 24; circuitry to raise ARDTCNTL of Figure 24 to a

	programming potential; an "Architectural Program Decoder (Fig.20) and a [programming potential] level shifting circuit similar to the Pass Gate Driver (Figure 22A)" connected to PADFEED of Figure 24; and "a column driver circuit similar to that shown in Fig. 21" connected to line 14H10 of Figure 24. 14:26-37.
sense means coupled to said memory device output terminal for sensing the level of a logic signal generated by said programmed memory device and for developing a commensurate control signal; and	A structure which is the same as or the equivalent of the structure in the specification which performs the function of sensing the level of a logic signal generated by the programmed memory device and developing a commensurate control signal. The structure disclosed in the specification is the Schmidt trigger circuit 202 of Figure 24. 14:16-18.
multiplexer means responsive to said control signal and operative to couple said logic	A structure which is the same as or the equivalent of the structure in the specification

circuit means output terminal	which performs the function of
either to an input/output	coupling the logic circuit
terminal or to a signal	means output terminal either
feedback path thereby causing	to an input/output terminal or
said logic circuit means to	to a signal feedback path
have one of a predetermined	thereby causing the logic
set of logic circuit	circuit means to have one of a
configurations.	predetermined set of logic configurations. The structure disclosed in the specification is the FMUX of Figure 15.
	9:63-10:5.

Patent '421 Claim 7	Construction
In a programmable logic device	See claim 1.
as recited in claim 1	
wherein said logic circuit	See discussion of "electronic
means includes	logic circuit means" in claim
register means for temporarily	1 above. The "electronic
storing said circuit means	logic circuit means" elements
output signal and for	must include a structure which
developing a stored output	is the same as or the
signal, and	equivalent of the structure disclosed in the specification which performs the function of temporarily storing the "electronic logic

	circuit means" element output signal and developing a stored output signal. The structure disclosed in the specification is the D Flip-Flop of Figure 13. 9:7-16.
wherein said multiplexer means includes a plurality of transistor switching means connected between a plurality of data signal receiving terminals and a multiplexer output terminal, said data signal receiving terminals being coupled to receive said circuit means output signal, said stored output signal and an input signal from said input/output terminal, each said switching means being coupled to receive a control signal from one of said architecture control circuits	See discussion of "multiplexer means" in claim 1 above. The multiplexer means of claim 1 must include more than one of the structures which are the same as or the equivalent of the structures in the specification which perform the function of conducting or not conducting a data signal so as to allow the multiplexer means to selectively connect a data signal to the multiplexer output terminal. The particular data signal to be connected is (1) the circuit means output signal; (2) the

whereby one of said switching means may be rendered conductive and the others of said switching means may be rendered nonconductive by appropriately programming the corresponding reprogrammable memory device.	stored output signal; or (3) an input signal from an input/output terminal. The selection of which data signal to connect is determined by control signals from the architecture control circuits, which in turn are derived from the contents of the corresponding reprogrammable memory device. The structure disclosed in the specification is the multiplexer of Figure 15. The structures disclosed in the specification as the transistor switching means are switching transistors such as those labeled "N" in Figure 15.

Patent '421 Claim 13	Construction
In an integrated circuit device including electronic logic circuit means having data input, output, and input/output terminals,	This is a "Jepson" claim in that it begins with a preamble that recites an old device, continues with a transition that states "an improved

and
signal feedback paths to said
data input terminals, and
being responsive to at least
one architecture control
signal and operative to
perform a particular
electronic function on at
least one input data signal
received at a data input
terminal to generate at least
one commensurate circuit means
output signal at said circuit
means output terminal, and

programmable means comprising"
and concludes with the body of
the claim as the statement of
the new improvements upon the
old device.

The limitations imposed by the
preamble include an
"electronic logic circuit
means" element which responds
to at least one architecture
control signal and which
performs the function of

operating to perform a
particular electronic function
on at least one input data
signal to generate at least
one commensurate circuit means
output signal. This claim
covers a structure which is
the same as or the equivalent
of the structure in the
specification which performs
the function described above.
The structure disclosed in the
specification is Figure 8A

(except elements 80, 82 and 88), or Figure 8B (except the D-F.F. (FIG.13) elements, the OMUX (FIG.14) elements, and the two columns of elements to the far left of the Figure, one labeled "Input Circuit (Fig.9)" and the other labeled "Row Driver (Fig. 10)"), which by reference incorporate Figures 9-12, 15 and 16. 3:33-38.

The structures of Figure 8A and 8B include a programmable AND array, an OR/NOR array, a feedback row driver, an I/O driver and input circuit, and a feedback multiplexer. 7:3-7.

The "electronic logic circuit means" element must have data input terminals, data output terminals, data input/output terminals, and signal feedback paths to the data input terminals.

Data input terminals are

	structures that can be used to input a signal to the "electronic logic circuit means" element. Data output terminals are structures that can be used to output a signal from the "electronic logic circuit means" element. Data input/output terminals are structures that can be used to input a signal, output a signal, or both, to or from the "electronic logic circuit means" element. Signal feedback paths are circuitry that a signal goes through as it passes back to a data input terminal.
having programmable means for providing said architecture control signal to configure the architecture of said logic device so that said circuit means will perform a particular electronic function, an improved programmable means	The "programmable means" of the preamble is a means-plus-function element. Written in Jepson-style, this claim is for an improved programmable means, which performs the function of providing an architecture

comprising:	
	control signal to configure the architecture of the device so that the "electronic logic circuit means" element performs a particular electronic function. The body of the claim defines the improved programmable means that performs that function.
at least one architecture control circuit including: a reprogrammable memory device having an output terminal and a programming potential input terminal and which may be programmed either to a first state to generate a logic signal of a first level or programmed to a second state to general a logic signal of a second level at said memory device output terminal; programming means responsive to input program data signals and to a corresponding address signal and operative to program said memory	The "reprogrammable memory device," "programming means," and "sense means" elements of this claim have the same meaning as the corresponding elements of claim 1.

program said memory device to one of said states by applying a programming potential to said memory device programming potential input terminal; and sense means for sensing the level of a logic signal generated at said programmed memory device output terminal and for developing therefrom said architecture control signal for configuring the architecture of said logic device so that said circuit means will perform a particular electronic function.	

Patent '421 Claim 16	Construction
In an integrated circuit device as recited in claim 13	See claim 13.
wherein said electronic logic circuit means includes multiplexer means responsive to said architecture control signals and operative to couple said circuit	See discussion of "electronic logic circuit means" in claim 13 above. The "electronic logic circuit means" element must include a structure which is the same as or the

means output terminal either to an input/output terminal or to a signal feedback path.	equivalent of the structure in the specification which is responsive to the architecture control signals and which performs the function of connecting the "electronic logic circuit means" element output terminal either to an input/output terminal or to a signal feedback path. The structure disclosed in the specification is the OMUX of Figure 14 and the FMUX of Figure 15.

Patent '421 Claim 19	Construction
In an integrated circuit device as recited in claim 16	See claim 16.
wherein said programmable means includes a plurality of architecture control circuits	See discussion of "programmable means" and "architecture control circuits" in claims 1 and 13 above. The "programmable means" element must include more than one

	more than one architecture control circuit.
and wherein said electronic logic circuit means further includes register means for temporarily storing said circuit means output terminal signal and for developing a stored output signal,	The "register means" element of this claim has the same meaning as the corresponding element of claim 7.
and wherein said multiplexer means includes a plurality of transistor switching means connected between a plurality of data receiving terminals and a multiplexer output terminal, said data receiving terminals being coupled to receive said circuit means output terminal signal, said stored output signal and an input signal from said input/output terminal, each said transistor switching means being coupled to received a control signal from one of said architecture	The "multiplexer means" element of this claim has the same meaning as the corresponding element of claim 7.

control circuits whereby one of said switching means may be rendered conductive and the others of said switching means may be rendered nonconductive by appropriately programming the corresponding reprogrammable memory devices.	

Patent '421 Claim 25	Construction
In an integrated circuit device as recited in claim 16	See claim 16.
wherein said programmable means includes a plurality of architecture control circuits,	See discussion of "programmable means" in claims 1 and 13 above. The "programmable means" element must include more than one architecture control circuit.
and wherein said electronic logic circuit means further includes register means for temporarily storing said circuit means output signal and for developing a stored output signal,	The "register means" element of this claim has the same meaning as the corresponding element of claim 7.
and wherein said multiplexer	The "multiplexer means"

means includes output multiplexer having a plurality of transistor switching means connected between a plurality of data receiving terminals and a multiplexer output terminal, said data receiving terminals being coupled to receive said circuit means output signal, said stored output signal and an input signal from said input/output terminal, each said switching means being coupled to receive a control signal from one of said architecture control circuits whereby one of said switching means may be rendered conductive and the others of said switching means may be rendered non-conductive by appropriately programming the corresponding reprogrammable memory devices.	element of this claim has the same meaning as the corresponding element of claim 7.

The '986 Patent	
Patent '986 Claim 1	Construction
A programmable integrated circuit logic array device, comprising:	A programmable integrated circuit logic array device is an integrated circuit device that can be programmed to perform various logic functions.
a plurality of input terminals for receiving input signals;	An input terminal is a structure that can be used to input a signal. The device must have more than one input terminal.
a plurality of I/O terminals for receiving input signals and/or transmitting output signals;	An I/O terminal is a structure that can be used to input a signal, output a signal, or both, to or from the device. The device must have more than one I/O terminal.
first plurality of macrocells each including	A macrocell is a repeating block of circuit elements (as described below) which includes the wiring necessary to connect the elements.
at least a first programmable AND array having a	The "first programmable AND array" element of this

first plurality of memory cells arranged in addressable rows and columns, each said cell being individually programmable to contain logic data corresponding to the memory state of the cell,	claim has the same meaning as the corresponding element of patent B1'479 claim 1. The term "each said memory cell being individually programmable to contain logic data" has the same meaning as the term "which can be individually programmed to contain logic data" in patent B1'479 claim 1.
first sensing means connected to said first AND array, said first sensing means being responsive to certain ones of said input signals and operative to detect the memory state of one or more of said cells and to develop a corresponding first data signal,	A structure which is the same as or the equivalent of the structure in the specification which is responsive to certain ones of the input signals and which performs the function of detecting the memory state of one or more of the memory cells, and developing a corresponding first data signal. The structure disclosed in the specification

	is standard circuitry to implement an OR gate and a sense amplifier. 5:13-15;
	Fig. 2 element 66, and Fig. 3.
first signal storage means,	A structure which is the same as or the equivalent of the structure in the specification which performs the function of storing a signal. The structure disclosed in the specification is the D Flip-Flop shown as element 76 of
	Figure 3. 5:18.
first feedback means,	A structure which is the same as or the equivalent of the structure in the specification which performs the function of feeding back signals. The structure disclosed in the specification is a connection between the feedback multiplexer and a row driver.
	See Figs. 2-5.
and first multiplexing means for selectively	This means-plus-function claim language requires a

coupling said first data signal to one of said I/O terminals, to said first storage means, or to said first feedback means; and	structure which is the same as or the equivalent of a structure in the specification which performs the function of selectively coupling the first data signal developed by the sensing means to an I/O terminal, to the storage means, or to the feedback means. There is no structure in the specification which performs this function. The Court notes that the specification discloses a structure that performs a similar, although somewhat different, function. The text and drawings of the specification portray a structure that continuously connects the first data signal to the storage means. The selectivity provided by the

	disclosed multiplexing means allows coupling of: (1) either the first data signal or the output of the storage means to the I/O terminal; and (2) either the output of the storage means or the I/O terminal to the feedback means. The structure disclosed in the specification which performs these functions is the feedback multiplexer labeled 93 and the output multiplexer labeled 91 of Figure 3. 4:59-62; 5:25-28, 34-36.
a plurality of data buses including	A data bus is "one or more conductors that are used for transmission of ... data.. . ." *The IEEE Standard Dictionary of Electrical and Electronics Terms,* 117 (6th ed.1996).
a global input signal bus for coupling input signals	A global input signal bus is a data bus that couples

from said input terminals to a first group of cells in the AND arrays of each said	input terminals to all AND arrays on the device. 6:42-44; Fig. 5.
macrocell,	
a local feedback bus for coupling signals applied to the feedback means of at least some of said macrocells to a second group of cells of at	A local feedback bus is a data bus that couples feedback signals to a subset of the AND arrays on the device. 6:49-54. *See also* 4:25-28; 5:37-42;
least some of said macrocells,	Figs. 1 and 5.
and a global feedback bus for coupling data signals applied to some of said feedback means to a third group of cells of all of said AND arrays of said macrocells.	A global feedback bus is a data bus that couples feedback signals from a subset of macrocells to all AND arrays on the device. 6:45-48. *See also* 4:28-34; 6:33-35; Figs. 1 and 5.

Patent '986 Claim 2	Construction
A programmable integrated circuit logic array device as recited in claim 1 and further	See claim 1.
comprising:	
a second plurality of macrocells each including a	The "programmable AND array", "second sensing means",

programmable AND array having a plurality of memory cells arranged in addressable rows and columns, each said cell being individually programmable to contain logic data corresponding to the memory state of the cell, second sensing means responsive to certain ones of said input signals and operative to detect the memory state of one or more of said cells and to develop a corresponding data signal, second signal storage means, seconds feedback terminal means, and second multiplexing means for coupling said second data signal to said second storage means or to said second feedback means.	"second signal storage means", "second feedback terminal means", and "second multiplexing means" all have the same meaning as the corresponding elements of claim 1.

Patent '986 Claim 12	Construction
A programmable integrated circuit logic array	See claim 1.

device as recited in claim 1 and further comprising:	
a plurality of input latching circuits each coupling one of said input terminals to said input signal bus whereby input signals applied to said input terminals are maintained stable during certain intervals of time.	An input latching circuit is standard circuitry that captures and holds input signals. 7:22-45; Fig. 6.

Patent '986 Claim 13	Construction
A programmable integrated circuit logic array device as recited in claim 12	See claim 12.
wherein said input latching circuits include one input level shifting inverter stage, an output driver element, and a switchable pass gate and latch coupling the inverter stage to the driver element.	The input latching circuits must contain one input level shifting inverter stage, an output driver element, and a switchable pass gate and latch which couples the inverter stage to the driver element.
	See, e.g., Fig. 6; 7:22-45.

Patent '986 Claim 14	Construction
A programmable integrated circuit logic array device as	See claim 1.

recited in claim 1	
wherein said first multiplexing means includes a first switching means for connecting either the output of said first sensing means or the output of said first signal storage means to one of said I/O terminals.	See discussion of "multiplexing means" in claim 1 above. The "multiplexing means" element must include a structure which is the same as or the equivalent of the structure in the specification which performs the function of connecting either the output of the "first sensing means" element or the output of the "first signal storage means" element to one of the I/O terminals. The structure disclosed in the specification is the output multiplexer 91 of Figure 3.

Patent '986 Claim 15	Construction
A programmable integrated circuit logic array device as	See claim 14.

recited in claim 14	
wherein said first multiplexing means further includes a second switching means operative to	See discussion of "multiplexing means" in claims 1 and 14 above. This means-plus-function claim language

couple either the output of said first sensing means or one of said I/O terminals to said first feedback means.	requires a structure which is the same as or the equivalent of a structure in the specification which performs the function of coupling the output of the sensing means or the output of one of the I/O terminals to the feedback means. There is no structure in the specification which performs this function. The Court notes that the specification discloses a structure that performs a similar, although somewhat different, function. The text and drawings of the specification portray a structure that allows coupling of either the output of the storage means or the output of one of the I/O terminals to the feedback means. The structure disclosed in the specification which performs this function is the feedback multiplexer labeled 93 in Figure 3. 4:59-62; 5:25-28, 34-36.

IT IS SO ORDERED.