United States District Court,
E.D. Texas, Lufkin Division.

SEOUL SEMICONDUCTOR CO. LTD,
Plaintiff.
v.
NICHIA CORP.; Nichia America Corp.; and Daktronics, Inc,
Defendants.

Civil Action No. 9:07-CV-273

Feb. 6, 2009.

Background: Owner of patent directed toward semiconductor structure that utilized three-dimensional inclusions to confine charge carriers, and reduce effect of dislocations, brought infringement action against competitor. Parties sought claim construction.

Holdings: The District Court, Ron Clark, J., held that:
(1) terms "inclusion" and "three-dimensional inclusion" meant island of semiconductor material grown by three-dimensional nucleation buried in layer of different semiconductor material that has larger bandgap;
(2) term "active layer" meant layer in which both types of carriers, electrons and holes, are simultaneously present in significant numbers compared to an intrinsic semiconductor at room temperature;
(3) term "layer" meant a thickness of material, which may be made up of sub-layers, but does not refer to a substrate in a device unless the substrate is an electronically active portion of the device;
(4) term "sub-layer" meant a distinguishable thickness of material in a layer; and
(5) term "structure having plural layers in semiconductor material" meant two or more layers of semiconductor material used in a device.

Claims construed.

5,075,742. Construed.

David C. Radulescu, Danielle Rosenthal, Weil Gotshal & Manges, New York, NY, Benjamin Charles Elacqua, Fish & Richardson PC, Houston, TX, Claude Edward Welch, Law Office of Claude E. Welch, Lufkin, TX, Hojin Chang, Yulchon, Seoul, Korea, KO, Jennifer L. Jonak, Lukens Law Group, San Francisco, CA, Rip Finst, Weil, Gotshal & Manges, LLP, Redwood Shores, CA, for Plaintiff.

Otis W. Carroll, Jr., Collin Michael Maloney, Ireland Carroll & Kelley, Tyler, TX, Alison M. Tucher, Deok Keun Matthew Ahn, Morrison & Foerster LLP, San Francisco, CA, Clayton Edward Dark, Jr., Attorney at Law, Lufkin, TX, James Pooley, Marc David Peters, Morrison & Foerster, Palo Alto, CA, for Defendants.

RON CLARK**, District Judge.**

Plaintiff Seoul Semiconductor Co, Ltd. ("Seoul") filed suit against Defendants Nichia Corp., Nichia America Corp., and Daktronics, Inc. (collectively "Nichia") claiming infringement of United States Patent No. 5,075,742 ("the '742 patent"). The court conducted a Markman hearing to assist it in interpreting the meaning of the claim terms in dispute. FN1 Having considered the patents, and the parties' contentions as presented in their briefs and the arguments of counsel, the court now makes the following findings and construes the disputed claim terms. FN2

FN1. To become familiar with the technology underlying the '742 patent from the perspective of one skilled in the art and to better understand the technical aspects of both parties' arguments, the court appointed Dr. Howard Schmidt as technical advisor. [Doc. # 42]. Dr. Schmidt received his Ph.D. in Physical Chemistry from Rice in 1986. He is a Senior Research Fellow in the Department of Chemical and Biomolecular Engineering and the Smalley Institute of Rice University, and Senior Nanotechnology Advisor to the Advanced Energy Consortium. He joined Rice in 2003 as Executive Director of the Carbon Nanotechnology Laboratory and served in that capacity until February 2008. He is the recipient of the R & D 100 Award (1989) and the NSF Tibbett's Award (1994). His early research involved growth processes of electronic materials, including GaAs and diamond. His current research focuses on nanostructured materials for energy conversion and harvesting. He has 26 peer-reviewed papers and 28 conference presentations.

FN2. The transcript of the hearing contains a number of representations and agreements of the parties and the answers of their experts to technical questions from the court, all of which will not be repeated here, but which may assist in understanding the issues presented. This Order governs in the event of any conflict between the Order and the court's preliminary analysis at the hearing. The transcript will be cited as Tr. at p. ----, l. ----.

I. CLAIM CONSTRUCTION STANDARD OF REVIEW

[3] [4] " '[T]he claims of the patent define the invention to which the patentee is entitled the right to exclude.' " Phillips v. AWH Corp., 415 F.3d 1303, 1312 (Fed.Cir.2005)(*en banc*) (citation omitted), *cert. denied,* 546 U.S. 1170, 126 S.Ct. 1332, 164 L.Ed.2d 49 (2006). "Because the patentee is required to 'define precisely what his invention is,' it is 'unjust to the public, as well as an evasion of the law, to construe it in a manner different from the plain import of its terms.' " Id. at 1312 (quoting White v. Dunbar, 119 U.S. 47, 52, 7 S.Ct. 72, 30 L.Ed. 303 (1886)).

[5] The words of a claim are generally given their ordinary and customary meaning. Phillips, 415 F.3d 1303, 1312. The "ordinary and customary meaning of a claim term is the meaning that the term would have to a person of ordinary skill in the art in question at the time of the invention." Id. at 1313. Analyzing "how a person of ordinary skill in the art understands a claim term" is the starting point of a proper claim construction. Id.

[6] [7] A "person of ordinary skill in the art is deemed to read the claim term not only in context of the

particular claim in which the disputed term appears, but in the context of the entire patent, including the specification." Id. Where a claim term has a particular meaning in the field of art, the court must examine those sources available to the public to show what a person skilled in the art would have understood the disputed claim language to mean. Id. at 1314. Those sources "include 'words of the claims themselves, the remainder of the specification, the prosecution history, and extrinsic evidence concerning relevant scientific principles, the meaning of technical terms, and the state of the art.' " Id. (citation omitted).

[8] "[T]he ordinary meaning of claim language as understood by a person of skill in the art may be readily apparent even to lay judges, and claim construction in such cases involves little more than the application of the widely accepted meaning of commonly understood words." Id. In these instances, a general purpose dictionary may be helpful. Id.

[9] However, the Court emphasized the importance of the specification. "[T]he specification 'is always highly relevant to the claim construction analysis. Usually it is dispositive; it is the single best guide to the meaning of a disputed term.' " Id. at 1315 (quoting Vitronics Corp. v. Conceptronic, Inc., 90 F.3d 1576, 1582 (Fed.Cir.1996)). A court is authorized to review extrinsic evidence, such as dictionaries, inventor testimony, and learned treaties. Phillips, 415 F.3d 1303, 1317. However, their use should be limited to edification purposes. Id. at 1319.

[10] [11] The intrinsic evidence, that is, the patent specification, and, if in evidence, the prosecution history, may clarify whether the patentee clearly intended a meaning different from the ordinary meaning, or clearly disavowed the ordinary meaning in favor of some special meaning. *See* Markman v. Westview Instruments, Inc., 52 F.3d 967, 979-80 (Fed.Cir.1995); *aff'd,* 517 U.S. 370, 116 S.Ct. 1384, 134 L.Ed.2d 577 (1996). Claim terms take on their ordinary and accustomed meanings unless the patentee demonstrated "clear intent" to deviate from the ordinary and accustomed meaning of a claim term by redefining the term in the patent specification. Johnson Worldwide Assoc., Inc. v. Zebco Corp., 175 F.3d 985, 990 (Fed.Cir.1999).

[12] [13] The " 'ordinary meaning' of a claim term is its meaning to the ordinary artisan after reading the entire patent." Phillips, 415 F.3d 1303, 1321. However, the patentee may deviate from the plain and ordinary meaning by characterizing the invention in the prosecution history using words or expressions of manifest exclusion or restriction, representing a "clear disavowal" of claim scope. Teleflex, Inc. v. Ficosa N. Am. Corp., 299 F.3d 1313, 1327 (Fed.Cir.2002). If the patentee clearly intended to provide his own definitions,the "inventor's lexicography governs." Phillips, 415 F.3d 1303, 1316.

II. PATENT BACKGROUND AND TECHNOLOGY

Seoul asserts Claims 1-5 of U.S. Patent No. 5,075,742. The '742 patent was filed on January 10, 1991 and issued on December 24, 1991. It is directed to semiconductor structures and claims priority back to a French patent dated January 10, 1990.

Semiconductors have properties useful in controlling the flow of electrons in devices such as computers, televisions, and lasers. Semiconductors are grown (manufactured) using a variety of techniques and can be made of a single chemical element, such as silicon or from compounds of chemical elements such as gallium arsenide ("GaAs"). One of the problems that must be dealt with is the occurrence of dislocations-a type of defect that occurs during the growth process that can affect the performance of the semiconductor.

Some semiconductors, known as "n-type semiconductors" have an excess of free electrons in a certain

energy band known as the conduction band. Others, known as "p-type semiconductors" have a deficit of free electrons or "holes." These are in a lower energy grouping called a valence band. Layering a p-type semiconductor with an n-type results in a "p-n junction" in the region where the layers meet.

A semiconductor possesses a bandgap which is the range of disallowed energy levels between the conduction and valence bands as illustrated in Figure 1. An electron in the conduction band may recombine with a hole in the valence band and release light. The reverse process may also occur in which light is absorbed, creating an electron and a hole. These processes are frustrated if an electron or hole combines encounters a dislocation.

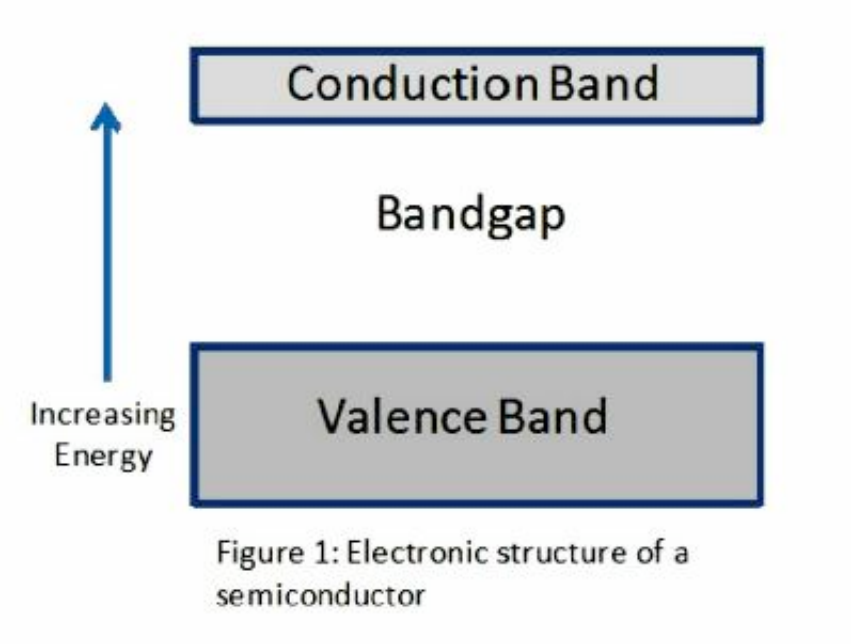

Figure 1: Electronic structure of a semiconductor

The '742 patent is directed toward a semiconductor structure that utilizes three-dimensional inclusions to confine charge carriers (the electrons and holes) and reduce the effect of dislocations. The patent discloses a structure with multiple layers made of semiconductor material. One layer contains three-dimensional inclusionsthat have a smaller bandgap than the bandgap of the layer itself.

III. PERSON OF ORDINARY SKILL IN THE ART

[14] The importance of identifying the education and experience of one of skill in the art has long been established. *See* Nazomi Communications, Inc. v. Arm Holdings, PLC, 403 F.3d 1364, 1370-71 (Fed.Cir.2005). Nevertheless Seoul did not set out its position on this issue in its opening brief. Seoul stated in its Reply Brief, submitted almost ten months after suit was filed, that it was waiting for information "before it commits to a particular 'level of ordinary skill in the art' in this case." Seoul's Reply Brief, Doc. # 56, p. 1, fn. 1. Tr. at p. 9, l. 17-p. 10, l. 14. The court understands the tactical advantage at trial, and the opportunities to claim error if an appeal is needed, that result from avoiding disclosure of contentions until the trial court rules on an important issue. However, the complexity and expense of modern commercial litigation make the cost of dilatory tactics and "trial by ambush" prohibitive. Accordingly, the Federal Rules

of Civil Procedure have evolved, and local rules have been adopted by district courts, to reduce cost and delay. *See* Fed.R.Civ.P. 1 & 26 and the Advisory Committee Notes for the 1993 Amendments to those Rules. *See also* Finisar Corp. v. DirecTV Group, Inc., 424 F.Supp.2d 896, 898-99 (E.D.Tex.2006)

At the Markman hearing Seoul's counsel finally stated its position that one of ordinary skill would have a Ph.D, but then observed "I don't really think it matters too much." Tr. p. 11, l. 20. Based on this remark and its failure to brief the subject, the court finds that Seoul has waived argument on this point.

[15] The court has reviewed the patent and extrinsic references in the field. Semiconductor technology and the potential use of layers of different materials from Groups III and V of the Mendeleevian classification were well known in 1991. FN3 A number of significant scientific articles within the field were lead-authored by graduate students prior to receiving their doctoral degree. Tr. at p. 14, l. 24-p. 15, l. 12. These individuals possessed a bachelor's degree and experience making multi-layer III-V semiconductor structures. The court concludes that a person of ordinary skill in the art has the equivalent of a four year degree (denoted in the United States as a bachelor's degree) in physics, electrical engineering, materials science, or a related area, coupled with three or more years of industrial or research experience making multi-layer III-V semiconductor structures. Extensive experience and technical training might substitute for some educational requirements, while advanced education might substitute for some experience. Nichia did not object to the definition. Tr. at p. 9, l. 16.

FN3. The Mendeleevian classification is commonly referred to as the Periodic Table of the Elements. This patent refers to elements found in Groups III and IV of that table, as well as silicon, a Group IV element.

IV. CLAIM CONSTRUCTION

1. "semiconductor/ semiconductor material" Claims 1 and 5.

Claim 1 of the '742 patent, states in part, with the disputed claim term in bold: "A structure having plural layers in **semiconductor material,....**"

Claim 5 states in part, with the disputed claim term in bold: "The structure claimed in claim **1,** wherein said layer comprising said inclusion comprises one of the following **semiconductor materials**...."

Nichia suggested defining this term as: "a compound made up of two or more of the following elements: gallium (Ga), arsenic (As), aluminum (Al), indium (In), and phosphorus (P)." Seoul proposed that the court construe semiconductor material to mean "a material whose conductivity properties can be controlled by either adding dopants or by applying an electric field."

The background of the invention and the summary of the invention provide references to semiconductors in general. Col. 1, l. 15-16; col. 4, l. 33-36. Nitride semiconductors were known at the time of the patented invention. *See e.g.* H.U. Baierand W. Monch, *Formation of Aluminum Nitride Films on GaAs(110) at Room-Temperature by Reactive Molecular-Beam Epitaxy: X-Ray and Soft-X-Ray Photoemission Spectroscopy,* 68 Journal of Applied Physics 586 (1990); R.F. Davis et al., *Critical Evaluation of the Status of the Areas for Future Research Regarding the Wide Band Gap Semiconductors Diamond, Gallium Nitride and Silicon Carbide,* 104 Mat. Sci. and Eng. 77 (1988). The specification discusses III-V semiconductors, a list that includes more elements than the five identified by Nichia. It is true that the specification names the semiconductors formed from materials on Nichia's list, but these are descriptions of specific embodiments.

Col. 1, l. 20-23; col. 3, l. 11-14; col. 6, l. 20-24. Additionally, while Claim 1 uses the general term "semiconductor material," Claim 5 describes semiconductors made of only the five specific elements included in Nichia's list. Since neither the specification nor prosecution history indicates otherwise, this lends support to the argument that "semiconductor material" includes more than those five elements.

As with many scientific terms there are a number of definitions of "semiconductor" that are partly correct, or that convey one or more properties or concepts associated with the term. A simple example would be to define a semiconductor as a material, the conductivity or resistivity of which, is between an insulator and a conductor. In this case that does not help one of skill in the art, or a juror. In the context of this patent the properties of carriers and forbidden bandgaps in semiconductors are important because the object of the invention is to reduce the influence of dislocations on the functioning of multilayer structures made from semiconductor material. *See* ' 742 Patent, Abstract; col. 1, l. 8-10; col. 2, l. 46-53; col. 2, l. 65-col. 3, l. 2.

Based on these specification references, the following definition focuses on these properties of a semiconductor:

"**semiconductor**" and "**semiconductor material**" mean "**a solid material that conducts limited electric current by means of a small number of carriers (free electrons or holes) and additional carriers that can be freed from their local bonds by the addition of other elements (doping) or by application of an electrical or magnetic field.**"

The parties agreed to this definition, Tr. at p. 36, l. 21-p. 38, l. 18. *See McGraw-Hill Encyclopedia of Electronics and Computers* 798-99 (Sybil P. Parker ed., 2d ed. 1988); *see also The IEEE Standard Dictionary of Electrical and Electronic Terms* 963 (6th ed. 1996).

2. "Inclusion" and "three-dimensional inclusion" Claims 1-5.

[16] This term is used in each of the five claims of the '742 patent. An exemplar use in Claim 1, stating in part, with the disputed term in bold: "each of said sub-layers having **three-dimensional inclusions** in a semiconductor material...."

Nichia argues that the proper term to construe is actually "three-dimensional inclusion" and offers the definition "islands of indium arsenide grown using three-dimensional nucleation and then buried by a different material." The specification discloses inclusions made from semiconductor materials other than indium arsenide ("InAs"). In addition, Claim 4 specifically states that the inclusions are made of InAs, while Claim 1 merely discloses the need for inclusions. Reading Claim 1 to require the inclusions to be made of InAs would render Claim 4 unnecessary. At the hearing Nichia agreed that the inclusions need not be made from InAs. Tr. at p. 50, l. 14-p. 51, l. 25.

Seoul suggested that "inclusion" should be construed to mean "a crystal or a fragment of a crystal found within another crystal." This is somewhat broad, implying that an inclusion could be of any material.

The "Summary Of The Invention" starts off with "one of the layers comprises three-dimensional inclusions in a semiconductor material...." '742 Patent, col. 2, l. 66-67. The patentees distinguished prior art, including U.S. Pat. No. 4,802,181 to Iwata which used etching and subsequent deposition to create quantum boxes and U.S. Pat. No. 4,751,194 to Cibert et al. which disclosed ion-implantation and lithographic masking techniques to form quantum boxes, by stating that the inclusions were grown in the material and not inserted

later. Pl. Br., Ex. 5 (Prosecution File History), Examiner's First Office Action at 3-4; Response to First Office Action at 4-5. The patentee distinguished the references on the basis that the inclusions are formed "during the semiconductor crystal growth" Id. at 5.

The only growth process discussed in the specification is three-dimensional nucleation. Col. 6, l. 37-39. Seoul contends that the specification discloses the two-dimensional growth mode as a route to the formation of inclusions. Tr. at p. 41, l. 2-9; *See* col. 5, l. 18-20. However, that part of the specification describes only the growth of the first monolayer of atoms. The specification then goes on to discuss a transition to a three-dimensional growth mode beginning with the second monolayer of atoms. Col. 5, l. 21-25; l. 38-40. The three-dimensional growth mode can be accomplished via different synthetic routes, such as molecular beam epitaxy, chemical vapor deposition and vapor phase epitaxy. *See* col. 6, l. 38-40. The fact that different techniques may be used to deposit the material that makes up the layers does not change the fact that the physical formation of the inclusions is by three-dimensional growth process.

While the parties argued about the use of "island" in any definition, the word is used a number of times within the specification. Col. 4, l. 62; col. 5, l. 25; col. 5, l. 26; col. 5, l. 28; col. 5, l. 29. It does not necessarily convey a "flat region" as argued by Seoul. Tr. at p. 63, l. 22-23 (testimony of Seoul's expert Dr. Streetman). The "Description of the Preferred Embodiments" disclosed a hemispherical shape. Col. 4, l.62-63 ("the inclusions **8** of InAs form islands substantially of a semi-spherical cap shape"). Further, use of the term "island" to convey three-dimensional features is consistent with the extrinsic evidence. Def. Resp., Doc. # 53, Ex. 10, J-Y Marzin, *II-V Semiconductor Strained-Layer Superlattices,* in *Physics, Fabrication, and Application of Multilayered Structures* 215, 220 (Dhez & Weisbuch eds., 1988) ("the growth process can switch from bidimensional to three-dimensional: this process results in the formation of 3D islands"); *see also* Def. Resp., Doc. # 53, Ex. 2, Dieter Bimberg, Marius Grundmann, and Nikolai Ledentsov, *Quantum Dot Heterostructures* 43 (1999) (illustrating a pyramid and prism shapes). The court will therefore construe, the term "inclusion" as follows:

"**inclusion**" and "**three-dimensional inclusion**" mean "**island of semiconductor material grown by three-dimensional nucleation buried in a layer of a different semiconductor material that has a larger bandgap.**"

"Three-dimensional nucleation" is a process where structures form and grow in three-dimensions, but does not include two-dimensional flat layer-by-layer growth.

3. "active layer" Claim 3.

[17] The term "active layer" appears in Claim 3: "The structure claimed in claim 1, wherein said layer comprising said inclusions is an **active layer** of an optoelectronic component."

Nichia suggests that the court adopt wording contained in the specification which states that "the active layer [ ] is the only region of the structure in which the two types of carriers are simultaneously present...." Col. 2, l. 47-53. Nichia's construction does not go far enough, as it is possible for electrons and holes to be simultaneously present in other layers, although not in appreciable numbers relative to the active layer. One of skill in the art would know that outside the active layer, some hole and electrons exist in practice. Even in a pure, undoped semiconductor (called an intrinsic semiconductor) at room temperature, some holes and electrons simultaneously exist. *See* Tr. at p. 80, l. 24 to p. 81, l. 5. Therefore, the issue is really one of degree. Holes and electrons are simultaneously present in the active layer to a significantly greater degree

than in any other layer.

Seoul criticizes Nichia's proposed construction, citing a book by Nichia's technical advisor, for the proposition that "[c]arriers tend to escape from the active layer of an LED into the confinement layers." Seoul's Claim Const. Br. at 13, Ex. 9, E. Fred Schubert, *Light-Emitting Diodes,* 81 (2nd ed. 2006). However, earlier in the chapter, the text explains that "[i]n an ideal LED, the injected carriers are confined to the active region by the barrier layers adjoining the active regions." Id. at 75. Again, this illustrates that the issue is one of degree. While electrons and holes may simultaneously exist and they may recombine to emit light, this occurs to a greater degree in the active layer. The active layer may simultaneously contain a thousand times more electrons and holes than an intrinsic semiconductor. For example, the carrier density in intrinsic (undoped) GaAs in a quantum well device is 10^{15} cm^{-3} or less (*see* Sajal Paul et al., *Empirical expressions for the alloy composition and temperature dependence of the band gap and intrinsic carrier density in Ga x In 1-x As,* 69 J. Appl. Phys. 827 (1991); Wallace C.H. Choy et al., *AlGaAs-GaAs Quantum-Well Electrooptic Phase Modulator with Disorder Delineated Optical Confinement,* 34 IEEE J. Quant. Elec. 84 (1998)), whereas the carrier density in the active region of a quantum well laser under operating conditions is over 10^{18} cm^{-3} (*see* A. Champage et al., *The Performance of Double Active Region InGaAsP Lasers,* 27 IEEE J. Quant. Elec. 2238 (1991)).

Further, Seoul's proposal that "active layer" means "a layer in the device that is capable of emitting light (i.e., emitting photons as electrons and holes recombine) when current is applied" suffers the same practical problem. If electrons and holes exist in the same region, they may recombine and release a photon of light. Moreover, the specification discloses more than light emitting devices, specifically optical modulators and optical switches. Col. 4, l. 33-36. The parties even agreed that the term "optoelectronic component" includes more than simply light emitting devices. It would be inappropriate to require the active layer to emit light as not every optoelectronic component that contains inclusions with a smaller bandgap than the surrounding material emits light. Tr. at p. 92, l. 3-13; Tr. at p. 136, l. 7-18; Pl. Resp., Doc. # 53, Ex. 8, U.S. Patent No. 5,187,715. The court will therefore construe the term as follows:

"**active layer**" means "**the layer in which both types of carriers (electrons and holes) are simultaneously present in significant numbers compared to an intrinsic semiconductor at room temperature**."

4. "layer" Claim 1, 3, and 5.

[18] An exemplar use of the term layer is in Claim 1, stating in part, with the disputed term in bold: "A structure having plural **layers** in semiconductor material...." Seoul argues that "layer" be construed to mean "a layer of material but does not refer to a substrate in a device." Nichia does not think that the term needs to be construed, but if it is, Nichia proposes "a thickness of material" and does not exclude the substrate.

Specifically, the parties dispute whether a layer includes the substrate. Seoul argues that the specification contrasts a layer with the substrate and that a person of ordinary skill in the art would understand the two terms to mean different things and would not think that a substrate is a layer.

Nichia points to dictionaries for the proposition that a layer can include a substrate and criticizes Seoul's proposed claim construction because it indicates what a layer is not, rather than what it is. The latter argument is unavailing as it may be necessary to construe a claim term to exclude sub-portions of the claim term, as here where the court has been asked to interpret both "layer" and "sub-layer." AFG Industries, Inc.

v. Cardinal IG Co., Inc., 239 F.3d 1239, 1250 (Fed.Cir.2001) (defining layer to exclude inter-layers which are too thin to be optically significant).

Generally, the specification distinguishes between the substrate and a layer. *See e.g.* col. 3, l. 61-64 ("semiconductor substrate **1** and a stacking of three or four layers in semiconductor material **2, 3, 4** and **5** placed on a major side of the substrate **1.**"); Col 4, l. 11-13 ("According to a preferred embodiment, the stacking of layers **2** to **5** constitutes a double heterostructure GaAs/GaAlAs formed on a substrate in silicon Si."). Nichia's technical expert, Dr. Schubert, and Seoul's expert, Dr. Streetman both admit that a substrate must be present to deposit semiconductors. Tr. at p. 106, l. 19 to p. 107, l. 19; Tr. p. 109 at 9-10.

However, in certain instances, the substrate should be included as a layer. At times the specification includes the substrate as a layer. In discussing the state of the prior art and dislocation formation in deposited semiconductors, the specification references a silicon substrate and the 4% lattice mismatch between GaAs and Si which results in a large number of dislocations. Col. 1, l. 39-42. The specification continues to explain that "when the crystalline lattice parameter of a layer is lower than that of a second layer, the first layer is subjected to tension and dislocations occur in the layer interface." Col. 1, l. 29-51. The Si substrate is the first layer and the GaAs is the second. Dislocations result from the lattice mismatch. The '742 patent specifically relies upon lattice mismatch and the three-dimensional growth mode to produce the inclusions. If the properties of the substrate are vitally important to the design and operation of the structure, the substrate is a layer.

Further, the substrate could be an electronically active portion of the structure. If it is, it would be logical to include it in the definition of layer. Both GaAs and InP have been used as substrates. Col. 1, l. 64-66. When the substrate functions as an electronically active portion of the structure, such as the n-type or p-type layer, it would be incorrect to exclude it from the definition of a "layer." If the substrate only acts as a mechanical support, it is not a layer.

The court will therefore construe "layer" as follows:

"**layer**" means "**a thickness of material, which may be made up of sub-layers, but does not refer to a substrate in a device unless the substrate is an electronically active portion of the device**."

5. "sub-layer" Claim 1.

[19] This term is used in Claim 1 of the '742 patent: "one of said layers comprising plural substantially parallel **sub-layers** ... each of said **sub-layers** having three-dimensional inclusions...." Seoul argues that "sub-layer" should be construed as "a portion of a layer," while Nichia suggests "a distinguishable portion of a layer constituted of the same material as the layer." Figures 9 and 10 of the specification illustrate sub-layers. Each is distinguishable as a thin layer of InAs that separates the GaAs sub-layers containing InAs inclusions. The sub-layers are made of the same material as the other sub-layers and thus the overall layer, except that the inclusions are also part of the sub-layer. Thus, to require the entire sub-layer to be made of exactly the same material as the layer is inaccurate. Moreover, graded junction materials also exist in the scientific literature. *See e.g.* C.K. Peng, S. Sinha, and H. Morkoc, *Characterization of graded interface In x Ga 1-x""" / In 0.52 $Al_{0.48}$As (0.53<<x<<0.70) structures grown by molecular beam epitaxy,* 62 J. Appl. Phys. 2880 (1987); H.X. Jiang, *Band Structure of Superlattice with Graded Interfaces,* 61 J. Appl. Phys 624 (1987). The composition of graded materials varies, such that no two horizontal cross sections contain the same composition or bandgap.

In support of its position that the sub-layer be made of the same material as the layer, Defendant cites Col 4, l. 36-39 of the specification which states: "In particular, the confining layers 3 and 5 may each be constituted by several layers of the same material but with different doping concentrations" for the proposition that each sub-layer must be made from the same material. Tr. at p. 120, l. 20-p. 121, l. 13. The specification used the word "may," which does not create a firm requirement.

The prosecution history further refutes the requirement that all sub-layers must be made of the same material. During prosecution, the patentee combined Claims 1 and 2 to create current Claim 1. The applicants amended the claims by incorporating the concept of "several substantially parallel planes [of inclusions]" in claim 1 as "plural substantially parallel sub-layers having ... inclusions." *See* Pl. Br., Doc. # 53, Ex. 5 (Prosecution File History), Response to First Office Action at 2-3. The patentee and the examiner understood that different materials, namely a plane of inclusions, would be within each sub-layer. Nothing in the specification or prosecution suggests that the patentee acted as his own lexicographer to require the sub-layer to be made of exactly the same material as the rest of the layer.

Therefore, the court will construe the term as follows:

"**sub-layer**" means "**a distinguishable thickness of material in a layer**"

6. "[inclusions] in a semiconductor material." Claim 1.

The term appears in Claim 1, stating in part, with the disputed term in bold: "each of said sub-layers having three-dimensional inclusions **in a semiconductor material**...." Seoul argues that this should be construed to mean that the inclusions are "made of a semiconductor material." Nichia claims that the phrase is indefinite because "in" could mean "made of" or "inside," and either definition is consistent with the specification. The court has construed "inclusion" and "three-dimensional inclusion" to mean "island of semiconductor material grown by three-dimensional nucleation buried in a layer of a different semiconductor material that has a larger bandgap." Therefore both limitations suggested by Nichia are present in the phrase. The inclusions must be "made of" semiconductor material and the inclusions must be buried or "inside" other semiconductor material. Nichia agreed that given the court's construction of "inclusion," the term is not indefinite. Tr. at p. 140, l. 8-12. Likewise, since the earlier definition of inclusion controls, there is no need to construe this phrase separately.

7. "structure having plural layers in semiconductor material" Claim 1.

[20] This term is seen in Claim 1 of the '742 patent, stating in part, with the disputed term in bold: "A **structure having plural layers in semiconductor material,**...." The parties agreed that in this phrase "in a semiconductor material" means "made of a semiconductor material." They also agreed that "plural" means "two or more." Here, the dispute is whether the "structures" disclosed by the '742 patent must be directed toward a device.

Seoul suggests that the term be construed to mean "two or more layers of semiconductor material used in a semiconductor device." Nichia argues that this term need not be construed because the parties agreed to the definition of the term "plural" and the term "[plural layers] in semiconductor material."

Figure 1 of the '742 patent discloses a prior art structure that is used as a device. It contains semiconductor layers sandwiched between two thin metal layers (6 and 7) that act as electrodes. Col. 4, l. 43-45. These

metal layers are connected to leads. Once the metal electrodes in Figure 1 are connected to a suitable power source, such as a battery, light will be emitted. Similarly, Figure 4 discloses the present invention, including metal electrodes 6a and 7a. *See* col. 4, l. 48-49. Light emission would also result when this device is connected to a power supply.

Moreover, the patent examiner considered this invention to be directed toward a device. In the first Office Action, the examiner described claims 1 through 6 in the original application as "drawn to a semiconductor device." *See* Rosenthal Decl. Exh. 5 [Office Action, March 11, 1991 at 2]. The examiner placed the invention in Class 357, entitled "Active Solid State Devices, e.g. Transistors, Solid State Diodes," and Class 372, entitled "Coherent Light Generators." *See* Cover Page at [52].

A simple device might be incorporated as part of another device. Sophisticated devices can be made up of many simpler components, each of which could be a device. For example, an LED is a device, which can also be used as part of a laser, a more complex device.

Nichia argues that claim differentiation should apply to limit Claim 3 to specific optoelectronic components while limiting Claim 1 only to the broader definition of "structure." Claim 3 requires the layer containing the inclusions to be the "active layer" and the entire structure to be used as an optoelectronic component. The specification discloses that the "active layer" contains inclusions and that the invention is directed toward optoelectronic components.

[21] The doctrine of claim differentiation is a rebuttable presumption. Regents of University of Cal. v. Dakocytomation Cal., Inc., 517 F.3d 1364, 1375 (Fed.Cir.2008). "The doctrine of claim differentiation is not a hard and fast rule and will be overcome by a contrary construction dictated by the written description or prosecution history." Id. (internal citations omitted). Here, the specification defines the active layer and the use of the invention. It also discloses that the invention is directed toward a device, a simple device that may also be used in more complex devices. Therefore, the court will construe the term as follows:

"**structure having plural layers in semiconductor material**" means "**two or more layers of semiconductor material used in a device.**"

8. "sub-layers deposited successively during growth of said one layer, each of said sub-layer having ... inclusions" Claim 1.

[22] This term is seen in Claim 1 of the '742 patent, stating in part, with the disputed term in bold: "A structure having plural layers in semiconductor material, one of said layers comprising plural substantially parallel **sub-layers deposited successively during growth of said one-layer, each of said sub-layers having three-dimensional inclusions** in a semiconductor material...."

The specification describes the formation of an active layer by deposition of GaAs and InAs with no post-growth steps. *See* col. 5, l. 9-17 (describing the deposition of InAs after a deposition of GaAs); col. 5, l. 33-35 ("After each deposition of inclusions in a plane, the epitaxial growth of GaAs is again performed so as to form another active sub-layer"). Further, the preferred embodiment discloses sub-layers deposited one on top of another, right after each other. The specification mentions other heterostructures besides the one discussed in the preferred embodiment. Col. 6, l. 19-21. However, the specification does not describe a deviation from the method employed to create the sub-layers with the inclusions. Col. 6, l. 25-26 ("InAs inclusions can be fabricated here according to the method embodying the invention.").

In addition, to overcome prior art references, the patentee indicated that the deposition of inclusions "is realized during semiconductor crystal growth." Pl. Br., Doc. # 53, Ex. 5 (Prosecution File History), Response to First Office Action at 4-5. The prior art references used post-growth steps, such as masking, annealing, and injecting ions, to create quantum boxes which serve the same function as the inclusions. Id. at 4-5.

Therefore, the court will construe the term as follows:

"**sub-layers deposited successively during growth of said one layer, each of said sub-layer having ... inclusions**" means "**the layer is formed by growing sub-layers, each of which has inclusions, one at a time, with each sub-layer forming on the preceding sub-layer.**"

The parties agreed with this definition, subject to their dispute over the definition of "sub-layer," which is discussed above. Tr. at p. 158, l. 20-25; Tr. at p. 161, l. 9-p. 162, l. 2.

9. "each of said sub-layers having three-dimensional inclusions in a semiconductor material *and* a narrower forbidden band gap than a forbidden band gap of said one layer." Claim 1.

[23] This term is found in claim 1 of the '742 patent, stating in part, with the disputed term in bold: "A structure having plural layers in semiconductor material, one of said layers comprising plural substantially parallel sub-layers deposited successively during growth of said one layer, **each of said sub-layers having** three-dimensional inclusions in a semiconductor material ***and*** **a narrower forbidden band gap than a forbidden band gap of said one layer.**" (the "and" at issue, which was changed from "having" during prosecution, is emphasized). The parties agree that the real dispute revolves around the "and" and whether it is the sub-layers or the three-dimensional inclusions that must possess the narrower forbidden bandgap than the layer. Tr. at p. 166, l. 6-p. 167, l. 22.

Construing the word "and," according to its normal meaning, requires that the sub-layers have two characteristics: (1) they contain three-dimensional inclusions; and (2) they possess a narrower forbidden bandgap than a bandgap found in the layer. The issue is whether the second requirement is possible, that is, whether a sub-layer can contain a narrower bandgap than a bandgap of a layer. Inclusions, as the specification discloses, possess a smaller bandgap than the surrounding material of the sub-layer and layer. *See e.g.* Figure 6; col. 4, l. 55-60; col. 5, l. 41-43. One of skill in the art would understand that the second requirement of a sub-layer is met precisely because the sub-layer contains two different types of materials, the material of the inclusions (InAs in the preferred embodiment) and the material surrounding the inclusions (GaAs in the preferred embodiment). When one of skill in the art measures the bandgap of the sub-layer, through techniques such as optical absorption, electroreelection or photoluminescence, the measurement yields both the bandgap of the InAs inclusions and the surrounding GaAs material as well as information about the size and electrical characteristics of the quantum wells or inclusions. *See* Tr. at p. 180, l. 14-17; *see also* Claude Weisbuch & Borge Vinter, *Quantum Semiconductor Structures: Fundamentals and Applications* 58, 71, 73, 75, 76 (1991). Because the sub-layer contains inclusions which have a narrower bandgap, the sub-layer necessarily must also possess a bandgap (the bandgap of the InAs inclusions) which is narrower than another bandgap found in the layer (the bandgap of the GaAs).

Moreover, this is the required result even if the court had adopted Seoul's definition that "[inclusions] in a semiconductor material" means "made of a semiconductor material." Under this construction, Seoul argues that the claim requires that the *inclusions* contain a narrower bandgap, not the sub-layer. Tr. at p. 173, l. 4-9.

The claim would then require that the inclusions (1) be made of a semiconductor material; and (2) be made of a narrower forbidden bandgap. In the context of the whole claim, this makes little grammatical or technical sense because it would describe an object that is "made" of a property; in this case, the property of a narrower forbidden bandgap. The patentee never hinted that "and" would have a special definition in this patent.

Further, the prosecution history does not require any additional limitations be placed on the phrase at issue. The replacement of "having" with "and" was only a grammatical change and not done to overcome a prior art rejection. The patentee distinguished prior art, namely the Cibert et al. and Iwata references, based on structural differences and required post-processing steps in the prior art. *See* Pl. Br., Ex. 5 (Response to First Office Action) at 4-5. The patentee also made a number of other grammatical changes as the examiner requested. *See* Pl. Br., Ex. 5 (Response to First Office Action) at 1-2 (illustrating a number of grammatical changes); (Examiner's Action) at 2 ("The disclosure is objected to because of the following informalities: The specification contains nonidiomatic English.").

The court will therefore construe the entire phrase as follows:

"each of said sub-layers having three-dimensional inclusions in a semiconductor material **and a narrower forbidden band gap than a forbidden band gap of said one layer**" means "that in addition to having three dimensional inclusions, **each sub-layer must contain a forbidden band gap that is less than the band gap of the layer.**"

V. CONCLUSION

The jury will be instructed in accordance with the court's interpretation of the disputed claim terms in the '742 patent.

E.D.Tex.,2009.
Seoul Semiconductor Co. Ltd. v. Nichia Corp.