United States District Court, S.D. California.

HEWLETT-PACKARD DEVELOPMENT COMPANY, L.P.,

Plaintiff. v. GATEWAY, INC, Defendant. Gateway, Inc, Counterclaim-Plaintiff. v. Hewlett-Packard Development Company, L.P., Hewlett-Packard Company and Compaq Information Technologies Group, L.P, Counterclaim-Defendants. Intel Corp, Intervenor. Civil No. 04CV0613-B(LSP)

Jan. 12, 2006.

John Allcock, DLA Piper US, San Diego, CA, for Plaintiff/Counterclaim-Defendants.

Darryl J. Adams, Dean M. Munyon, James D. Smith, Wayne Harding, Dewey Ballantine, Austin, TX, Jonathan D. Baker, Dechert LLP, Mountain View, CA, W. Bryan Farney, Dechert LLP, Austin, TX, for Defendant.

CLAIM CONSTRUCTION ORDER FOR UNITED STATES PATENT NUMBER 5,381,530

RUDI M. BREWSTER, Senior District Judge.

Pursuant to Markman v. Westview Instruments, Inc., 517 U.S. 370, 116 S.Ct. 1384, 134 L.Ed.2d 577 (1996), on November 3 and 10, 2005, the Court conducted a Markman hearing in the above-titled patent infringement action regarding construction of the disputed claim terms for U.S. Patent Number 5,381,530 ("the '530 patent"). Plaintiff Hewlett-Packard Development Company, L.P. ("HP") was represented by the law firm of DLA Piper Rudnick Gray Cary U.S. LLP, Defendant Gateway, Inc. ("Gateway") was represented by the law firm of Dewey Ballantine LLP, and Intervenor Intel Corporation ("Intel") was represented by the law firm of Weil, Gotshal & Manges LLP.

At the Markman hearing, the Court, with the assistance of the parties, analyzed the claim terms in order to prepare jury instructions interpreting the pertinent claims at issue in the '530 patent. Additionally, the Court prepared a case glossary for terms found in the claims and the specification for the '530 patent considered to be technical in nature which a jury of laypersons might not understand clearly without specific definition.

After careful consideration of the parties' arguments and the applicable statutes and case law, the Court **HEREBY CONSTRUES** the claims in dispute in the '530 patent and **ISSUES** the relevant jury instructions as written in Exhibit A, attached hereto. Further, the Court **HEREBY DEFINES** all pertinent technical terms as written in Exhibit B, attached hereto.

IT IS SO ORDERED.

EXHIBIT A FN1

UNITED STATES PATENT NUMBER 5,381.530-CLAIM CHART VERBATIM CLAIM LANGUAGE COURT'S CONSTRUCTION

Claim 1	
1. A method for filtering input	1. A method for filtering input commands directed to a controller
commands directed to a controller	operating using a series of software commands responsive to input
operating using a series of software	commands [the input commands cause the controller to execute a
commands responsive to input	series of software instructions when the controller receives the input
commands, said controller accessed	commands], said controller accessed by a microprocessor, said input
by a microprocessor, said input	commands intended to direct said controller to produce system
commands intended to direct said	control signals [the input commands intended by a program
controller to produce system control	executed by the microprocessor to cause the controller to produce
signals in response to said input	system control signals] (system control signals [signals used to
commands from said microprocessor,	direct the operation of, and capable of being understood by, any
comprising the steps of:	device that has to handle them in the system]) in response to said
	input commands from said microprocessor, comprising the steps of:
monitoring signal lines coupled to	monitoring signal lines coupled to output terminals of said
output terminals of said	microprocessor, said signal lines communicating input commands
microprocessor, said signal lines	from the microprocessor;
communicating input commands from	
the microprocessor;	
processing a selected input command	processing a selected input command using a <i>logic device</i> [a
using a logic device; and	programmable device for performing specific logic functions]; and
producing an output signal from said	producing an output signal from said logic device corresponding to
logic device corresponding to said	said selected input command, as said system control signal, and in
selected input command, as said	replacement of said system control signal directed to be produced
system control signal, and in	by said controller, [the logic device generating the system control
replacement of said system control	signal the controller would have generated if the controller had
	initially received the selected input command] after a shorter delay
controller, after a shorter delay from	from the time said monitoring step detects said selected input
the. time said monitoring step detects	command than the delay if said controller <i>operated using a series of</i>
said selected input command than the	software commands responsive to said selected input command [the
	selected input command causes the controller to execute a series of
a series of software commands	software instructions when the controller receives the selected input
responsive to said selected input	command].
command.	
Claim 2	

2. The method of claim 1, further

comprising:	
blocking a write command signal	blocking a write command signal from being applied to said
from being applied to said controller	controller for said selected input command,
for said selected input command.	
Claim 3	
3. The method of claim 2, wherein	3. The method of claim 2, wherein said <i>logic device</i> has an input
said logic device has an input coupled	coupled to receive said write command signal, and has an output for
to receive said write command signal,	presenting said write command signal to said controller; and
and has an output for presenting said	
write command signal to said	
controller; and	
wherein said blocking step is	wherein said blocking step is performed by said <i>logic device</i> not
performed by said logic device not	presenting said write command signal to said controller responsive to
presenting said write command signal	receiving said selected input command.
to said controller responsive to	
receiving said selected input	
command.	
Claim 4	
4. The method of claim 1, wherein	4. The method of claim 1, wherein said <i>logic device</i> is a separate
said logic device is a separate	<i>integrated circuit</i> [a small piece of semiconductive material that
integrated circuit from said controller.	contains interconnected miniaturized electronic circuits, often
	<i>referred to as a "chip"</i>] from said controller.
Claim 5	
5. The method of claim 1, wherein	5. The method of claim 1, wherein said system control signal
said system control signal corresponds	corresponds to an address bit masking signal.
to an address bit masking signal.	
Claim 6	
6. The method of claim 1, wherein	6. The method of claim 1, wherein said system control signal
said system control signal corresponds	corresponds to a <i>microprocessor reset signal</i> [a signal that causes
to a microprocessor reset signal.	the microprocessor to return to the state it would be in if the power
	were turned off and then on again].
Claim 7	
7. The method of claim 1, wherein	7. The method of claim 1, wherein said controller is of the 8042 type
said controller is of the 8042 type.	[an INTEL 8042 keyboard controller].
Claim 8	
8. A method of controlling a computer	8. A method of controlling a computer system, said computer system
system, said computer system	comprising a microprocessor having real and protected mode
comprising a microprocessor having	operation capabilities and a controller <i>for operating in a</i>
real and protected mode operation	programmed manner according to input commands [the input
	commands cause the controller to execute a series of programmable
capabilities and a controller for	communus cause the controller to execute a series of programmable
capabilities and a controller for operating in a programmed manner	instructions when the controller receives the input commands]
operating in a programmed manner	
-	instructions when the controller receives the input commands]
operating in a programmed manner according to input commands	<i>instructions when the controller receives the input commands</i>] produced by the microprocessor, said microprocessor coupled to signal lines for communicating the input commands to the controller
operating in a programmed manner according to input commands produced by the microprocessor, said	<i>instructions when the controller receives the input commands</i>] produced by the microprocessor, said microprocessor coupled to signal lines for communicating the input commands to the controller

detecting a FORCE-A20 input	detecting a FORCE-A20 input command [a command initiating the
e 1	FORCE-A20 function of causing the A20 line of the microprocessor
e	to stay low] on the signal lines, said FORCE-A20 input command
	intended to direct the controller to produce a FORCE-A20 system
	control signal [the FORCE-A20 input command intended by a
	program executed by the microprocessor to cause the controller to
6	produce a FORCE-A20 system control signal] for use in masking
	address bit A20; and
	responsive to said detecting step, producing the FORCE-A20 system
	<i>control signal</i> with <i>circuitry</i> [<i>a programmable device for performing</i>
	<i>specific logic functions</i>] coupled to the signal lines;
to the signal lines;	
	wherein the propagation delay of the <i>circuitry</i> in producing the
	FORCE-A20 system control signal responsive to said detecting step
	is shorter than the delay of the controller operating in the
	programmed manner to the FORCE-A20 input command.
the delay of the controller operating in	
the programmed manner to the	
FORCE-A20 input command.	
Claim 9	
	9. The method of claim 8, further comprising:
comprising:	
	blocking a write command signal from being applied to the controller
	responsive to said detecting step, so that said controller is rendered
	inoperable to produce the FORCE-A20 system control signal
	responsive to said FORCE-A20 input command.
inoperable to produce the FORCE-	
A20 system control signal responsive	
to said FORCE-A20 input command.	
Claim 10	
10. The method of claim 9, wherein	10. The method of claim 9, wherein said <i>circuitry</i> has an input for
	receiving the write command signal, and has an output coupled to
· 1	said controller for communicating the write command signal thereto;
	and
controller for communicating the	
write command signal thereto; and	
	wherein said blocking step is performed by said <i>circuitry</i> .
performed by said circuitry.	
Claim 11	
	11. The method of claim 8, wherein said <i>circuitry</i> is in a separate
	integrated circuit from that of said controller.
integrated circuit from that of said	0
controller.	
Claim 12	
	12. The method of claim 8, further comprising:

comprising:	
detecting a CPU-RESET input	detecting a CPU-RESET input command [a command initiating the
command on the signal lines, said	reset function of causing the microprocessor to return to the state it
CPU-RESET input command	would be in if the power were turned off and then on again] on the
intended to direct the controller to	signal lines, said CPU-RESET input command intended to direct
produce a CPU-RESET system	the controller to produce a CPU-RESET system control signal [the
control signal for application to the	CPU-RESET input command intended by a program executed by the
microprocessor; and	microprocessor to cause the controller to produce a CPU-RESET
interoprocessor, and	system control signal] for application to the microprocessor; and
responsive to said step of detecting	responsive to said step of detecting the <i>CPU-RESET input</i>
the CPU-RESET input command,	command, producing the CPU-RESET system control signal with
producing the CPU-RESET system	the <i>circuitry</i> .
control signal with the circuitry.	
Claim 13	
13. The method of claim 8, wherein	13. The method of claim 8, wherein the controller comprises a
the controller comprises a keyboard	keyboard controller of the 8042 type.
controller of the 8042 type.	
Claim 14	
14. A data processing system,	14. A data processing system, comprising:
comprising:	
a microprocessor of a type having the	
capability of operating in real mode	mode and in protected mode, said microprocessor coupled to an
and in protected mode, said	address bus including an A20 address line, said microprocessor
microprocessor coupled to an address	having the functional capability of forcing the A20 address line to a
bus including an A20 address line,	logic level responsive to a FORCE-A20 signal;
said microprocessor having the	
functional capability of forcing the	
A20 address line to a logic level	
responsive to a FORCE-A20 signal;	
a controller having inputs for	a controller having inputs for receiving a set of input commands
receiving a set of input commands	produced by said microprocessor <i>intended to cause said controller to</i>
produced by said microprocessor	direct system operation in a programmed manner in response to
intended to cause said controller to	said input commands, said set of input commands comprising a
direct system operation in a	FORCE-A20 input command that is intended to generate the
programmed manner in response to	FORCE-A20 signal [intended by a program executed by the
r	microprocessor to cause the controller to direct system operation in a
-	programmed manner, the input commands including a command
input command that is intended to	intended by the program executed by the microprocessor to produce
*	
circuitry, having inputs coupled to	<i>circuitry</i> , having inputs coupled to said microprocessor to receive
said microprocessor to receive input	input commands therefrom, <i>for generating the FORCE-A20 signal</i>
commands therefrom, for generating	responsive to receiving a FORCE-A20 input command from said
the FORCE-A20 signal responsive to	microprocessor and in replacement of said controller generating the
receiving a FORCE-A20 input	FORCE-A20 signal; [in response to receiving a FORCE-A20 input
command from said microprocessor	command, generating the FORCE-A20 signal that the controller
and in replacement of said controller	would have generated if the controller had initially received the
and in replacement of said condoner	would have generaled if the controller had initially received the

generating the FORCE-A20 signal;	FORCE-A20 input command]
wherein said generating circuitry	wherein said generating <i>circuitry</i> generates the FORCE-A20 signal
generates the FORCE-A20 signal	responsive to the FORCE-A20 input command in a shorter time than
responsive to the FORCE-A20 input	the delay of said controller operating in the programmed manner
command in a shorter time than the	responsive to the FORCE-A20 input command [the controller
delay of said controller operating in	executing a series of programmable instructions to produce the
	FORCE-A20 signal if the controller received the FORCE-A20 input
the FORCE-A20 input command.	command].
Claim 15	
15. The system of claim 14,	15. The system of claim 14, wherein said generating <i>circuitry</i> is
wherein said generating circuitry is	located in a separate <i>integrated circuit</i> from that of said controller.
located in a separate integrated	
circuit from that of said controller.	
Claim 16	
16. The system of claim 14, wherein	16. The system of claim 14, wherein said generating <i>circuitry</i> is also
said generating circuitry is also for	for blocking a write command signal from being applied to said
blocking a write command signal	controller for said FORCE-A20 input command.
from being applied to said controller	
for said FORCE-A20 input command.	
Claim 17	17 The sector of the interval of the sector of the se
17. The system of claim 16, wherein	17. The system of claim 16, wherein said generating <i>circuitry</i> has an input for receiving a write commond signal and has an autnut
said generating circuitry has an input for receiving a write command signal,	input for receiving a write command signal, and has an output coupled to said controller for presenting the write command signal
and has an output coupled to said	thereto.
controller for presenting the write	
command signal thereto.	
Claim 18	
18. The system of claim 14, wherein	18. The system of claim 14, wherein said microprocessor also has an
said microprocessor also has an input	input for receiving a CPU-RESET signal;
for receiving a CPU-RESET signal;	
wherein said set of input commands	wherein said set of input commands further comprises a <i>CPU</i> -
further comprises a CPU-RESET	RESET input command that is intended to generate the CPU-RESET
input command that is intended to	signal; and
generate the CPU-RESET signal; and	
wherein said generating circuitry is	wherein said generating <i>circuitry</i> is also for <i>generating the CPU</i> -
also for generating the CPU-RESET	RESET signal responsive to receiving the CPU-RESET input
signal responsive to receiving the	command from said microprocessor and in replacement of said
CPU-RESET input command from	controller generating the CPU-RESET signal [in response to
said microprocessor and in	receiving the CPU-RESET input command, generating the CPU-
replacement of said controller	RESET signal the controller would have generated if the controller
generating the CPU-RESET signal.	had initially received the CPU-RESET input command].
Claim 19	
19. The system of claim 18, wherein	19. The system of claim 18, wherein said generating <i>circuitry</i>
said generating circuitry comprises a	comprises a programmable logic array.
programmable logic array.	
Claim 20	

20. The system of claim 18, wherein	20. The system of claim 18, wherein said generating <i>circuitry</i>
said generating circuitry comprises:	comprises:
a first programmable logic array for	a first programmable logic array for generating the FORCE-A20
generating the FORCE-A20 signal	signal responsive to receiving a FORCE-A20 input command from
responsive to receiving a FORCE-	said microprocessor; and
A20 input command from said	
microprocessor; and	
a second programmable logic array	a second programmable logic array for generating the CPU-RESET
	signal responsive to receiving a CPU-RESET input command from
responsive to receiving a CPU-	said microprocessor.
RESET input command from said	
microprocessor.	
Claim 21	
21. A method of controlling a	21. A method of controlling a computer system, said computer
computer system, said computer	system comprising a microprocessor and a controller <i>for operating in</i>
system comprising a microprocessor	a programmed manner according to input commands produced by
and a controller for operating in a	the microprocessor, said microprocessor coupled to signal lines for
programmed manner according to	communicating the input commands to the controller, said method
input commands produced by the	comprising the steps of:
microprocessor, said microprocessor	
coupled to signal lines for	
communicating the input commands	
to the controller, said method	
comprising the steps of:	
	detecting a microprocessor reset input command [a command
command on the signal lines, said	initiating the reset function of causing the microprocessor to return to
microprocessor reset input command	the state it would be in if the power were turned off and then on again
intended to direct the controller to] on the signal lines, said microprocessor reset input command
produce a microprocessor reset	intended to direct the controller to produce a microprocessor reset
system control signal for application	system control signal [the microprocessor reset input command
to the microprocessor; and	intended by a program executed by the microprocessor to cause the
1 /	controller to produce a microprocessor reset system control signal]
	for application to the microprocessor; and
responsive to said detecting step,	responsive to said detecting step, producing the <i>microprocessor reset</i>
producing the microprocessor reset	system control signal [a system control signal that causes the
system control signal with circuitry	microprocessor to return to the state it would be in if the power were
coupled to the signal lines and to the	turned off and then on again] with circuitry coupled to the signal
microprocessor;	lines and to the microprocessor;
wherein the propagation delay of the	wherein the propagation delay of the <i>circuitry</i> in producing the
circuitry in producing the	microprocessor reset system control signal responsive to said
microprocessor reset system control	detecting step is shorter than the delay of the controller operating in
signal responsive to said detecting	the programmed manner to the <i>microprocessor reset input command</i> .
step is shorter than the delay of the	
controller operating in the	
programmed manner to the	
microprocessor reset input command.	
Claim 22	

22. The method of claim 21, further	22. The method of claim 21, further <i>comprising:</i>
comprising:	
blocking a write command signal from being applied to the controller responsive to said detecting step, so that said controller is rendered inoperable to produce the microprocessor reset system control signal responsive to said	blocking a write command signal from being applied to the controller responsive to said detecting step, so that said controller is rendered inoperable to produce the <i>microprocessor reset system control signal</i> responsive to said <i>microprocessor reset input command</i> .
č 1	
microprocessor reset-input command.	
Claim 23	
23. The method of claim 22, wherein said circuitry has an input for receiving the write command signal, and has an output coupled to said controller for communicating the write command signal thereto; and	23. The method of claim 22, wherein said <i>circuitry</i> has an input for receiving the write command signal, and has an output coupled to said controller for communicating the write command signal thereto; and
wherein said blocking step is	wherein said blocking step is performed by said <i>circuitry</i> .
performed by said circuitry.	
Claim 24	
24. The method of claim 21, wherein said circuitry is in a separate integrated circuit from that of said controller.	24. The method of claim 21, wherein said <i>circuitry</i> is in a separate <i>integrated circuit</i> from that of said controller.
Claim 25	
25. The method of claim 21, wherein the controller comprises a keyboard controller of the 8042 type.	25. The method of claim 21, wherein the controller comprises a keyboard controller <i>of the 8042 type</i> .
Claim 26	
26. A data processing system, comprising:	26. A data processing system, <i>comprising:</i>
a microprocessor having an input for receiving a microprocessor reset signal;	a microprocessor having an input for receiving a <i>microprocessor reset signal:</i>
a controller having inputs for receiving a set of controller input commands produced by said	a controller having inputs for receiving a set of controller input commands produced by said microprocessor <i>intended to cause said</i> <i>controller to direct system operation in a programmed manner in</i>
	response to said controller input commands, said set of input commands comprising a microprocessor reset input command that
in a programmed manner in response to said controller input commands, said set of input commands	<i>is intended to generate the microprocessor reset signal;</i> [<i>intended by a program executed by the microprocessor to cause the controller to direct system operation in a programmed manner, the input</i>
comprising a microprocessor reset input command that is intended to generate the microprocessor reset signal;	commands including a microprocessor reset input command intended by the program executed by the microprocessor to produce commands to generate the microprocessor reset signal]

circuitry, having inputs coupled to said microprocessor to receive input commands therefrom, for generating the microprocessor reset signal responsive to receiving a microprocessor reset input command from said microprocessor and in replacement of said controller generating the microprocessor reset signal;	<i>circuitry</i> , having inputs coupled to said microprocessor to receive input commands therefrom, for <i>generating the microprocessor reset</i> <i>signal responsive to receiving a microprocessor reset input</i> <i>command from said microprocessor and in replacement of said</i> <i>controller generating the microprocessor reset signal;</i> [<i>in response</i> <i>to receiving a microprocessor reset input command, generating the</i> <i>microprocessor reset signal that the controller would have generated</i> <i>if the controller had initially received the microprocessor reset input</i> <i>command</i>]
controller operating in the	wherein said generating <i>circuitry</i> generates the <i>microprocessor reset</i> <i>signal</i> responsive to the <i>microprocessor reset input command</i> in a shorter time than the delay of <i>said controller operating in the</i> <i>programmed manner responsive to the microprocessor reset input</i> d <i>command</i> . [the controller executing a series of programmable instructions to produce the microprocessor reset signal if the e controller received the microprocessor reset input command]
Claim 27	
27. The system of claim 26, wherein said generating circuitry is located in a separate integrated circuit from that of said controller.	27. The system of claim 26, wherein said generating <i>circuitry</i> is located in a separate <i>integrated circuit</i> from that of said controller.
Claim 28	
28. The system of claim 26, wherein said generating circuitry is also for blocking a write command signal from being applied to said controller for said microprocessor reset input command.	28. The system of claim 26, wherein said generating <i>circuitry</i> is also for blocking a write command signal from being applied to said controller for said <i>microprocessor reset input command</i> .
Claim 29	
29. The system of claim 28, wherein said generating circuitry has an input for receiving a write command signal, and has an output coupled to said controller for presenting the write command signal thereto.	29. The system of claim 28, wherein said generating <i>circuitry</i> has an input for receiving a write command signal, and has an output coupled to said controller for presenting the write command signal thereto.

EXHIBIT B

UNITED STATES PATENT NUMBER 5.381.530-GLOSSARY OF TERMS

TERM

DEFINITION

a programmable device for performing specific logic

functions

CPU-RESET input command

For operating in a programmed manner according to input commands

FORCE-A20 input command

Generating the CPU-RESET signal responsive to receiving the CPU-RESET input command from said microprocessor and in replacement of said controller generating the CPU-RESET signal

Generating the FORCE-A20 signal responsive to receiving a FORCE-A20 input command from said microprocessor and in replacement of said controller generating the FORCE-A20 signal

Generating the microprocessor reset signal responsive to receiving a microprocessor reset input command from said microprocessor and in replacement of said controller generating the microprocessor reset signal

Integrated circuit

Intended to cause said controller to direct system operation in a programmed manner in response to said input commands, said set of input commands comprising a FORCE-A20 input command that is intended to generate the FORCE-A20 signal

Intended to cause said controller to direct system operation in a programmed manner in

a command initiating the reset function of causing the microprocessor to return to the state it would be in if the power were turned off and then on again

the input commands cause the controller to execute a series of programmable instructions when the controller receives the input commands

a command initiating the Force-A20 function of causing the A20 line of the microprocessor to stay low

in response to receiving the CPU-RESET input command, generating the CPU-RESET signal the controller would have generated if the controller had initially received the CPU-RESET input command

in response to receiving a FORCE-A20 input command, generating the FORCE-A20 signal that the controller would have generated if the controller had initially received the FORCE-A20 input command

in response to receiving a microprocessor reset input command, generating the microprocessor reset signal that the controller would have generated if the controller had initially received the microprocessor reset input command

a small piece of semiconductive material that contains interconnected miniaturized electronic circuits, often referred to as a "chip"

intended by a program executed by the microprocessor to cause the controller to direct system operation in a programmed manner, the input commands including a command intended by the program executed by the microprocessor to produce commands to generate the FORCE-A20 signal

intended by a program executed by the microprocessor to cause the controller to direct system operation in a response to said controller input commands, said set of input commands comprising a microprocessor reset input command that is intended to generate the microprocessor reset signal

Logic device

Microprocessor reset input command

Microprocessor reset signal

Of the 8042 type

Operated using a series of software commands responsive to said selected input command

Operating using a series of software commands responsive to input commands

Producing an output signal from said logic device corresponding to said selected input command, as said system control signal, and in replacement of said system control signal directed to be produced by said controller

Said controller operating in the programmed manner responsive to the microprocessor reset input command

Said controller operating in the programmed manner responsive to the FORCE-A20 input command

Said CPU-RESET input command intended to direct the controller to produce a CPU-

programmed manner, the input commands including a microprocessor reset input command intended by the program executed by the microprocessor to produce commands to generate the microprocessor reset signal

a programmable device for performing specific logic functions

a command initiating the reset function of causing the microprocessor to return to the state it would be in if the power were turned off and then on again

a signal that causes the microprocessor to return to the state it would be in if the power were turned off and then on again

an INTEL 8042 keyboard controller

the selected input command causes the controller to execute a series of software instructions when the controller receives the selected input command

the input commands cause the controller to execute a series of software instructions when the controller receives the input commands

the logic device generating the system control signal the controller would have generated if the controller had initially received the selected input command

the controller executing a series of programmable instructions to produce the microprocessor reset signal if the controller received the microprocessor reset input command

the controller executing a series of programmable instructions to produce the FORCE-A20 signal if the controller received the FORCE-A20 input command

the CPU-RESET input command intended by a program executed by the microprocessor to cause the

RESET system control signal	controller to produce a CPU-RESET system control signal
Said FORCE-A20 input command intended to direct the controller to produce a FORCE- A20 system control signal	the FORCE-A20 input command intended by a program executed by the microprocessor to cause the controller to produce a FORCE-A20 system control signal
Said input commands intended to direct said controller to produce system control signals	the input commands intended by a program executed by the microprocessor to cause the controller to produce system control signals
Said microprocessor reset input command intended to direct the controller to produce a microprocessor reset system control signal	the microprocessor reset input command intended by a program executed by the microprocessor to cause the controller to produce a microprocessor reset system control signal
System control signals	signals used to direct the operation of, and capable of being understood by, any device that has to handle them in the system

FN1. All terms appearing in bold face type and underlined have been construed by the court and appear with their definitions in the glossary in Exhibit B. The definition for each construed term appears in italics after its first use in the patent.

S.D.Cal.,2006. Hewlett-Packard Development Co., L.P. v. Gateway, Inc.

Produced by Sans Paper, LLC.