United States District Court,
S.D. New York.

U.S. PHILIPS CORPORATION,
Plaintiff.
v.
ATMEL CORPORATION, LSI Logic Corporation,
Defendants.

No. 01 CV 9178(LAP)

April 6, 2004.

OPINION

PRESKA**, J.**

On August 25, 1987, the United States Patent and Trademark Office ("USPTO") issued to inventors Adrianus Moelands and Herman Schutte United States Patent No. 4,689,740 (" '740 patent"). The patented invention is a "Two-Wire Bus-System Comprising a Clock Wire and Data Wire for Interconnecting a Number of Stations." The plaintiff in this action, U.S. Philips Corporation ("Philips" or "Plaintiff"), is the assignee of the '740 patent, which contains 35 claims and seven figures. The '740 patent expires August 25, 2004. Here, Philips alleges that certain Atmel Corporation ("Atmel" or "Defendant") products infringe eighteen claims of the '740 patent. The parties seek construction of the eighteen claims at issue.

Facts

The '740 patent derives from patent application 317,693, which was filed with the USPTO on November 2, 1981. Its claimed invention is a "Two-Wire Bus-System Comprising a Clock Wire and a Data Wire for Interconnecting a Number of Stations." ('740 patent, Col. 1, lines 2-4.) In 1981, the '740 patent introduced a novel communication protocol that allows computers and other electronic devices to communicate with one another using only two "buses", or "wires", a "clock bus" and a "data bus". This two-wire bus system is desirable, and in wide use today, because it reduces the complexity and expense associated with predecessor systems, which required multiple buses and additional hardware and software. Philips asserts that the Defendants infringed eighteen claims of the '740 patent.

As noted above, the '740 patent is directed to a novel communication "protocol" to allow computers and similar electronic devices to communicate with one another. The wires that connect such devices and allow them to send messages back and forth are called a "buses." An electronic device connected to a bus is called a "station." Two or more stations attached to a bus create a "system." The ON/OFF switches used in computers are called "transistors." Transistors use three terminals-for the present purposes, top, bottom, and gate-to turn on and off the flow of electricity.

A typical transistor is illustrated below:

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When electricity is applied to the gate wire, the transistor turns ON bridging the gap between the top terminal and the bottom terminal and permitting electricity to flow from the top wire to the bottom wire. If

no electricity is applied to the gate, the transistor is turned OFF, and obviously, electricity does not flow from the top to the bottom of the transistor.

This flow of electricity is illustrated below:

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TABULAR OR GRAPHIC MATERIAL SET AT THIS POINT IS NOT DISPLAYABLE
In the '740 patent, a "0" corresponds to a switch in the ON position with electricity flowing from the top terminal of the transistor to the bottom terminal. The '740 patent also uses the terms "a first voltage level," "a low output impedance," or "a first logic value" to describe the "0" or ON position. That is, when a transistor is ON and electricity is flowing, there is a "first" electrical voltage level measured at the top terminal, a first "logic value," or the binary number "0," at the top terminal, and a corresponding "low" electrical impedance value measured at the top terminal. Conversely, the OFF position corresponds to a a "second" electrical voltage level measured at the top terminal, a second "logic value," or the binary number "1," at the top terminal, and a corresponding "high" electrical impedance value measured at the top terminal.

Timing Diagrams

When in time a switch turns ON and OFF, its "timing", is important for communicating over a bus. Engineers use "timing diagrams" to illustrate such timing. For example, when communicating the number "7," (0-1-1-1), the switch sequence is ON-OFF-OFF-OFF. The timing diagram and corresponding switch state would look like this:

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For communicating the number 10-1010 in binary code-the switch sequence is OFF-ON-OFF-ON and the timing diagram would look like this:

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Electronic devices use a "clock," more particularly, periodic OFF/ON or "high/low" pulses on a wire, to decide when to check the state of the switch. For example, a device can decide to check the transistor every time the clock pulse is high or "1." In that manner, a computer can determine whether it is receiving three "1" 's in sequence instead of one long "1" signal.

The following illustrations show the clock pulse timing diagram, switch timing diagram, and switch state for sending the numbers 7 and 10 in binary code-0111 and 1010 respectively:

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TABULAR OR GRAPHIC MATERIAL SET AT THIS POINT IS NOT DISPLAYABLE
The '740 Patent

The Prior Art

Prior to the invention of the '740 patent, different bus wires were used to communicate different types of signals. For example, a system might have several bus wires devoted to clock signals, several bus wires devoted to data signals, as well as several bus wires devoted to control signals. Because such clock, data, and control signals operated independently of one another, each needed a dedicated bus wire.

The need for multiple bus wires between each station made connecting a large number of stations cumbersome and required a large amount of space. In today's environment where small electronic devices, such as portable CD players or cell phones, are desirable, the old-style bus systems greatly limited the number of stations that could be used, and therefore, greatly limited the functionality of such devices.

The '740 Invention

The inventors of the '740 patent developed a solution to this multi-wire bus problem. In a nutshell, they used only two wires-one for clock signals and one for data signals-and invented a protocol for the start and stop control signals using a novel sequence of timing the data and clock switches.

The Start and Stop Control Signals and Data Signals

Not wanting to add another line to the bus, the inventors of the '740 patent wrestled with a way in which to generate start and stop control signals using only a clock wire and data wire. Finally, they struck upon the idea of keeping the clock in one state and using the transition of a data signal to communicate a control signal. A transition is when a switch changes from "1" to "0" or from "0" to "1." Thus, the inventors decided that when the clock signal is high ("1") and the data signal changes from high ("1") to low ("0")-that is, when the data transistor switches from OFF to ON-that 1-to-0 change indicates a start signal. A simple way to describe a start signal is to look at a diagram of the binary values:

```
  clock pulse interval
Clock   1   -
            >
                =
                START
Data    1   0
```

Similarly, when the clock signal is high and the data signal changes from low ("0") to high ("1"), that 0-to-1 change indicates a stop signal. The diagram for a stop signal is:

```
 clock pulse interval

Clock   1   -
            >
                =
                STOP
Data    0   1
```

Figure 3 of the '740 patent illustrates the invention with a timing diagram:

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Number 20 is the timing diagram for the clock signal. Number 22 is the timing diagram for the data signal. Box 60 represents a moment in time during which a start signal is sent on the bus-the clock signal is high ("1") and the data signal changes from high ("1") to low ("0"). At all other times while transmitting data, the data signal remains constant (either high or low) when the clock signal is high ("1") (see number 64). Box 62 represents a stop signal to be sent after the data transmission is complete. To transmit a stop signal, the clock signal is high ("1") and the data signal changes from low ("0") to high ("1"). As stated in the '740 patent:

FIG. 3 shows a time diagram of the starting and stopping of the data transport between two stations. Initially, all stations generate "1" signals on the clock wire 20 and on the data wire 22. The transport is started by one of these stations which generates a transition on the data wire from "1" to "0", while the signal on the clock wire does not change; the relevant station thus manifests itself as a new master. This signal pattern is not permissible for data transport. All other stations thus recognize the pattern as a control signal and detect that a new master of the bus has asserted itself (block 60). Subsequently, the master produces a transition on the clock line, so that the first data bit can be generated on the data wire: this bit

(64) may have the value "0" or "1".

* * *

The transmission procedure is then terminated by the master station which transmits a stop signal while the clock wire is at a "0" level. First the level on the data wire is also brought to "0". Subsequently, the level on the clock wire is brought to "1". Finally (block 62), the level on the data wire is brought to "1". This signal pattern also is not permissible in customary data transmission and is recognized as a control signal. The master thus releases the bus line, so that a next station can manifest itself as a master.

(Col. 4, lines 15-50.)

The important rule when transmitting data on the bus, *e.g.*, communicating the number "7," (0-1-1-1), is that the data signal not change at any time when the clock signal is high ("1"). Otherwise, stations on the bus will erroneously think that a start or stop signal has occurred.

The diagrams of binary values for this rule are shown below:

Clock	1	1		
			=	"0" bit
Data	0	0		

Clock	1	1		
			=	"1" bit
Data	1	1		

The inverse of that rule is that the data signal can only change when the clock signal is low ("0"). The diagrams of binary values for this rule are shown below:

Clock	0	0		
			=	change to send a "1"
Data	0	1		

Clock	0	0		
			=	change to send a "0"
Data	1	0		

Figure 2 of the '740 patent illustrates this rule-data signals can only change when the clock is low, between points 56 and 58, and must remain constant while the clock is high, between points 58 and 59:

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The '740 patent **describes this rule:**

During data transmission the data signal may only change between the instants denoted by lines 56 and 58

and must remain the same between the instants denoted by the lines 58 and 59 (i.e. the clock pulse interval including the time occupied by the edges of the clock signal). As noted below any change in the level of the data line which occurs during the clock pulse interval may be interpreted as a control signal
(Col. 3, lines 50-57.)
During the clock pulses, the signal on the data bus wire is stationary; it may change between the clock pulses. Start and stop conditions are formed by a signal combination between clock bus wire and data bus wire (60 and 62, respectively) which is not permissible in a data stream. ('740 patent. Abstract.) The entire '740 patent is built around this rule. Indeed, every asserted claim recites the rule in one fashion or another.

Litigation History

On October 17, 2001, Philips filed a complaint alleging that Atmel, among others, was infringing, contributing to the infringement of, and/or actively inducing others to infringe the '740 patent by making, using, selling, and/or offering for sale within the United States, and/or importing into the United States, products that incorporate the apparatuses, and/or practice the methods claimed in the '740 patent. On November 13, 2001, Philips filed an amended complaint ("Complaint" or "Compl.") that repeated the infringement allegations made against Atmel. (Compl.para.para. 19-30).

On January 11, 2002, Atmel filed its answer and counterclaims to the Complaint denying the infringement allegations and seeking declaratory judgments of non-infringement, invalidity and unenforceability of the '740 patent. On May 20, 2003, Atmel filed a motion for summary judgment claiming the '740 patent is invalid in that Philips failed to disclose its best mode as required by 35 U.S.C. s. 112. That motion was filed under seal and is currently pending. On November 3, 2003, Atmel also filed motions for summary judgment claiming that Philips is barred by the principles of equitable estoppel and laches from asserting infringement of the '740 patent against Atmel. Those motions were filed under seal and are currently pending.

On May 30, 2002, counsel and experts conducted a technology tutorial, and on July 14, 2002, counsel conducted a *Markman* hearing. Prior to the *Markman* hearing, the parties submitted claim construction briefs FN1 in which they provided their proposed interpretation of the terms and phrases comprising claims 1, 2, 4-5, 10, 13-14, 16-18, 21-23, 29, and 32-35.

FN1. Philips' Corrected Memorandum of Law on the Interpretation of the Asserted Claims of U.S. Patent No. 4,689,740 ("Pl.Br."), Defendants' Corporations' Memorandum Regarding Claim Construction of the Asserted Claims of U.S. Patent No. 4,689,740 dated June 23, 2004 ("Def.Br."), Philips' Reply Memorandum of Law on the Interpretation of the Asserted Claims of U.S. Patent No. 4,689,740 ("Reply Br.").

After further consultation with counsel, it appears that (1) construction of claims relating to the terms "allowing ... to assume a second voltage level" and "forcing to a first voltage level", (2) determination of whether the control unit "box" (*e.g.,* unit 36 in figure 1) does or does not represent structures well known to those skilled in the art of bus design, and (3) construction of claims relating to the terms "clock pulse interval" and "first fraction of a clock pulse interval" will substantially advance the course of the litigation. Accordingly, with counsel's consent, those issues will be determined at this time.

The Law

Claim interpretation is a question of law for the Court. Markman v. Westview Instruments, Inc., 52 F.3d 967, 979 (Fed.Cir.1995) (en banc), *aff'd,* 517 U.S. 370, 116 S.Ct. 1384, 134 L.Ed.2d 577 (1996). To interpret the claims properly, the court should look at the relevant "intrinsic evidence," which is (1) the words of the claims; (2) the patent specification; and (3) the prosecution history of the patent. *See, e.g.,* Gart v. Logitech, Inc., 254 F.3d 1334, 1340 (Fed.Cir.2001). In examining the intrinsic evidence, the Court must start with the words of the claims and with a heavy presumption that claim terms carry their ordinary meaning as viewed

by one having ordinary skill in the art. Rexnord Corp. v. Laitram Corp., 274 F.3d 1336, 1341 (Fed.Cir.2001); CCS Fitness, Inc. v. Brunswick Corp., 288 F.3d 1359, 1366 (Fed.Cir.2002); *see also* Tate Access Floors, Inc. v. Interface Architectural Resources, Inc., 279 F.3d 1357, 1369 (Fed.Cir.2002) ("strong presumption"). There is a "heavy presumption" that claim terms carry their ordinary meaning, unless a special meaning is clearly and deliberately set forth in the intrinsic evidence. *Union Carbide Chems. & Plastics Tech. Corp.,* 308 F.3d at 1177; *accord* Multiform Desiccants, Inc. v. Medzam, Ltd., 133 F.3d 1473, 1478 (Fed.Cir.1998); *accord* Texas Digital Systems, Inc. v. Telegenix, Inc., 308 F.3d 1193, 1202 (Fed.Cir.2002).

Rebutting the Presumption of Plain Meaning

The presumption of plain meaning, however, may be rebutted. It is rebutted where (1) the patentee, acting as his own lexicographer, clearly established a definition of the term different from its customary meaning, Hoechst Celanese Corp. v. BP Chemicals, Ltd., 78 F.3d 1575, 1578 (Fed.Cir.1996); Brookhill-Wilk 1, LLC v. Intuitive Surgical, Inc., 326 F.3d 1215, 1220 (Fed.Cir.2003); (2) the meaning of a claim term is so unclear from the intrinsic evidence that there is no means by which the scope of the claim may be ascertained from the language used. Bell Atl. Network Servs., Inc. v. Covad Communs. Group, Inc., 262 F.3d 1258, 1268 (Fed.Cir.2001) (quoting Johnson Worldwide Assocs. v. Zebco Corp., 175 F.3d 985, 990 (Fed.Cir.1999)); or (3) the patentee disavowed an interpretation of a claim during prosecution, Texas Digital, 308 F.3d at 1204 (citing Teleflex, Inc. v. Ficosa N. Am. Corp., 299 F.3d 1313, 1324 (Fed.Cir.2002)).

A patentee demonstrates an intent to deviate from the ordinary and accustomed meaning of a claim term or phrase by redefining it or by characterizing it in the invention using words or expressions that manifest his intent to exclude or restrict its meaning. Teleflex, 299 F.3d at 1327; *accord* Brookhill-Wilk 1, 326 F.3d at 1220 (noting that the context of the claim terms must be considered in determining their ordinary and customary meaning); Renishaw PLC v. Marposs Societa' per Azioni, 158 F.3d 1243, 1248 (Fed.Cir.1998)(noting that "there is no legitimate way to narrow the property right" besides pointing to claim terms which confine or affect a patent's scope). The patentee must have defined the term "with reasonable clarity, deliberateness, and precision" in the written description or the prosecution history in order for the court to deviate from the ordinary and customary meaning of such term. In re Paulsen, 30 F.3d 1475, 1480 (Fed.Cir.1994); *accord* Teleflex, 299 F.3d at 1326.

Absent a clear indication that the patentee intended that a claim term carry a special meaning, the court is to attribute the ordinary and customary meaning to such term. Hoechst, 78 F.3d at 1578; Markman, 52 F.3d at 979-981, Brookhill-Wilk 1, 326 F.3d at 1220.

In addition, the ordinary meaning of a term does not apply when the claim term chosen by the patentee, if given its ordinary meaning, would so deprive the claim of clarity as to require the court to resort to the other intrinsic evidence for a definite meaning. CCS Fitness, 288 F.3d at 1367 (quoting Johnson Worldwide, 175 F.3d at 990).

However, "[n]otwithstanding the fact that the claim language must be examined in light of the written description, limitations may not be read into the claims from the written description." *See* Prima Tek II L.L.C. v. Polypap S.A.R.L., 318 F.3d 1143, 65 U.S.P.Q.2d 1818, 1821 (Fed.Cir.2003), citing Comark Communications, Inc. v. Harris Corp., 156 F.3d 1182, 1187 (Fed.Cir.1998). It is the claims, not the specification, that define the metes and bounds of the invention. *E.g.,* Corning Glass Works v. Sumitomo Elec. U.S.A., Inc., 868 F.2d 1251, 1257-58 (Fed.Cir.1989).

If, and only if, the intrinsic evidence is not sufficient, the court then may use extrinsic evidence-such as expert testimony and other evidence outside the intrinsic evidence-to assist in understanding the technology or the view of those of ordinary skill in the art. Pitney Bowes, Inc. v. Hewlett-Packard Co., 182 F.3d 1298, 1309 (Fed.Cir.1999); Vitronics Corp. v. Conceptronic, Inc., 90 F.3d 1576, 1584 (Fed.Cir.1996) (a court may

rely on extrinsic evidence in "instances in which intrinsic evidence is insufficient to enable the court to determine the meaning of the asserted claims"); Markman, 52 F.3d at 980.

Extrinsic evidence may not be used, however, to vary or contradict the clear meaning of claim terms. Markman, 52 F.3d at 981. It is improper to rely on extrinsic evidence to construe a claim unless "the claim language remains genuinely ambiguous after consideration of the intrinsic evidence." Bell & Howell Document Management Prods. Co. v. Altek Sys., 132 F.3d 701, 706 (Fed.Cir.1997). This rule is important because "[p]atents should be interpreted on the basis of their intrinsic record, not on the testimony of such after-the-fact 'experts' that played no part in the creation and prosecution of the patent." *Id*. However, extrinsic evidence may be consulted to assist in understanding the underlying technology. Interactive Gift Express, Inc. v. Compuserve, Inc., 256 F.3d 1323, 1332 (Fed.Cir.2001).

Extrinsic Evidence

Extrinsic evidence consists of all evidence external to the patent and prosecution history, including expert and inventor testimony, dictionaries, and learned treatises. Bell Atlantic, 262 F.3d at 1269. This evidence may be helpful to explain scientific principles, the meaning of technical terms, and the terms of art that appear in the patent and prosecution history. Extrinsic evidence may demonstrate the state of the prior art at the time of the invention. It is useful "to show what was then old, to distinguish what was new, and to aid the court in the construction of the patent." Brown v. Piper, 91 U.S. 37, 41, 23 L.Ed. 200 (1875).

The court may also consult dictionaries, encyclopedia and treatises in ascertaining a claim term's ordinary meaning. Altiris, Inc. v. Symantec Corp., 318 F.3d 1363, 1369 (Fed.Cir.2003); Texas Digital, 308 F.3d at 1202; Vanguard Prods. Corp. v. Parker Hannifin Corp., 234 F.3d 1370, 1372 (Fed.Cir.2000). The court must identify the dictionary meaning that is most consistent with the use of the words by the inventor. Brookhill-Wilk 1, 326 F.3d at 1221-22 (examining intrinsic record where multiple, potentially consistent dictionary definitions existed for claim term at issue).

In either case, however, "extrinsic evidence may be used only to assist in the proper understanding of the disputed limitation; it may not be used to vary, contradict, expand or limit the claim language from how it is defined, even by implication, in the specification or the file history." Bell Atlantic, 262 F.3d at 1269; *accord* Vitronics, 90 F.3d at 1584-85. Extrinsic evidence may not be used, however, to support an interpretation that contradicts the plain language of the claims. *Markman* at 981.

The Disputed Claims of the '740 patent

The parties dispute construction of the numerous claims in this matter, many of which comprise or depend upon one or more elements that are expressed as a means for performing a specified function. For example, Claim 1 includes:

1. A system for data transmission comprising:

(A) at least one master transmitting station which is capable of controlling data transmission, comprising:

(a) a clock terminal;

(b) a data terminal;

(c) means for producing a clock signal ...;

(d) means for producing a start signal ...;

(e) means for producing a stop signal ...;

(f) means for transmitting binary data....

(claim 1, 14; Col. 11, lines 9-39).FN2 Central to much of the dispute regarding these claims is the parties' disagreement about whether the '740 patent sufficiently describes the structure depicted in, *e.g.,* unit 36 of Figure 1, the "control unit," and units 116 and 134 of Figure 7, the "clock control element" and the "data control element." (*E.g.,* Def. Br. pp. 10, 12-13.)

FN2. *See also, e.g.,* system claims 2, 10, 21-35 and station claims 4-5, 13-14, 29, 32-35.

The parties agree that the various "means for" elements recited in the asserted station and system claims are "means plus function" elements governed by 35 U.S.C. s. 112 para. 6. In order to construe a means-plus-function claim, the court must (1) identify the function that is recited in the claim element, and (2) identify the corresponding structure that performs the recited function. *E.g.,* Wenger Mfg., Inc. v. Coating Mach. Sys., Inc., 239 F.3d 1225, 1233 (Fed.Cir.2001). The parties do not appear to disagree as to the recited functions and also agree that the '740 patent links those recited functions to a corresponding structure that performs the recited functions, that is, to a "control unit," (*e.g.,* unit 36 of Figure 1), working in combination with data and clock transistors, *e.g.,* 48 and 50, and/or data and clock signal receivers, *e.g.,* 40 and 42. At issue, however, is whether the '740 patent describes the control unit in sufficient detail to (i) overcome Atmel's invalidity challenge under 35 U.S.C. s. 112 para. 2,FN3 and (ii) refute Defendant's assertion that the claim elements that require the control unit structure must be limited in scope by the control unit structure illustrated in Figure 7.

FN3. Because Atmel presents its "black box" argument as an invalidity defense (see Def. Br. at 10), it is their burden to show by clear and convincing evidence that one skilled in the art would not know what structure could be used to effect the functions listed. *See, e.g., Intel,* 319 F.3d at 1366.

Atmel argues that the control unit, as illustrated in Figure 1, is nothing more than an empty box, that it contains no circuitry, no components, no software or logic, and that the specification contains no description as to what the empty box contains. (*E.g.,* Def. Br. at 10) Atmel argues that Figure 7, although similarly insufficient to describe the control unit structure necessary to perform the recited functions of the '740 patent, provides some of the structure necessary to perform the functions attributed to the control unit by Philips. (Def. Br. at 10-11). Atmel also argues that the claims that rely on the control unit structure to perform their functions, and that survive their validity challenge, must be limited to the structure disclosed in Figure 7. (*E.g.,* Def. Br. at 36).

Philips contends, not surprisingly, that the control unit disclosed in the '740 patent, and illustrated in Figure 1, simply represents a wide range of electronic devices, any one of which, when connected to another station via the described two-wire bus system, could serve as the control unit. According to Philips, microcomputers, input/output processors, function generators, memories, input/output equipment, such as keyboards or displays, and sensors for physical and/or chemical quantities all may serve as the necessary control unit. (Pl. Br. at 18-19) Philips contends that even though a variety of devices may provide the necessary control unit circuitry, the '740 patent sufficiently defines the structure because a person ordinarily skilled in the art at the time the '740 patent was filed could have identified and constructed the described "control unit."

The Control Unit

A patentee may express a claim element as a means or step for performing a specified function without

reciting the structure, material, or acts in support thereof, and that claim element will be construed to cover the corresponding structure, material or acts described in the specification, and equivalents thereof. 35 U.S.C. 112 para. 6; Chiuminatta Concrete Concepts, Inc. v. Cardinal Indus., Inc., 145 F.3d 1303, 1307-08 (Fed.Cir.1998). Such an expression is commonly referred to in the industry as a "means-plus-function" expression.

A means-plus-function expression need not recite all possible means that might be used for performing the claimed function. O.I. Corp. v. Tekmar Co., Inc., 115 F.3d 1576, 1583 (Fed.Cir.1997). However, in exchange for the convenience of expressing the claim element as a means for performing a function, the scope of the claim element is limited to the corresponding structure, material or acts specified in the written description and equivalents thereof. *Id*. Terms appearing in multiple claims are construed in concert throughout the patent. Southwall Techs. Chronologies, Inc. v. Cardinal IG Co., 54 F.3d 1570, 1579 (Fed.Cir.1995).

As the court noted in Intel Corp. v. Via Technologies, Inc., 319 F.3d 1357 (Fed.Cir.2003), a structure corresponding to a means-plus-function claim that is defined in a manner that embraces multiple methods for implementing such structure is not, for that reason alone, invalid on the basis that a person ordinarily skilled in the art would not know what the structure comprises. Id. at 1366 (rejecting the defendant's contention that a means-plus-function claim was indefinite because there was an unlimited number of implementations that could modify the corresponding computer's core logic to perform the recited functions and the patent did not disclose the circuitry or other structure of any such implementations, leaving the universe of implementations undefined.) Similarly, the Federal Circuit found that structure described as a "selector" was sufficiently defined in the disclosing patent as the structure required to perform the "selectively receiving" function, even though neither the electronic structure of the selector nor the details of its electronic operation was described in the specification. S3 Inc. v.. NVIDIA Corp., 259 F.3d 1364, 1370-71 (Fed.Cir.2001). *See also* In re Dossel, 115 F.3d 942 (Fed.Cir.1997) (finding that corresponding structure described as a device that received digital data, performed mathematical computations and output the results to a display was a general-purpose computer, even though the word "computer" was not used in the specification and no computer code was quoted, and holding that such structure was adequately described.) Id. at 946-47.

Recited Functions that Correspond to the Control Unit Structure

Here, the parties agree that the control unit is claimed as corresponding structure to perform, in part, the following functions:

"means for producing a clock signal at the clock terminal by allowing the clock terminal to assume a second voltage level for each of a series of periodic clock pulse intervals and by forcing the clock terminal to a first voltage level at all other times during production of the clock signal";

(Col. 11, lines 15-21; *see also;* Claims 1-2, 4-5, 10, 13-14, 21-23, 29, 32; Figure 1; Def. Br. at 9-10; Pl. Br. at 39-40)

"means for producing a start signal which indicates that the master station is prepared to control data transmission by allowing the voltage level at the data terminal to assume a second voltage level for a first fraction of a clock pulse interval and by then forcing the voltage at the data terminal to a first voltage level during the same clock pulse interval";

(Col. 11, lines 22-30; *see also;* Claims 1-2, 4-5, 10, 13-14, 21-23, 29, 32; Def. Br. at 12; Pl. Br. at 40-41)

"means for producing a stop signal which indicates that the master station has finished controlling data transmission by forcing the voltage level at the data terminal to the first voltage level during a first fraction

of a clock pulse interval and then allowing the voltage at the data terminal to transition to the second voltage level during the same clock pulse interval";

(Col. 11, lines 30-37; *see also* Claims 1-2, 4-5, 10, 13-14, 21-23, 29, 32; Def. Br. at 14; Pl. Br. at 42)

"means for transmitting binary data by forcing the voltage at the data terminal to the first voltage level during an entire clock pulse interval to transmit a first data value and by allowing the voltage at the data terminal to assume the second voltage level during an entire clock pulse interval to transmit a second data value";

(Col. 11, lines 38-44; *see also* Claims 1-2, 4-5, 10, 13-14, 21-23, 29, 33; Def. Br. at 9; Pl. Br. at 42-43)

"means for establishing priority when a plurality of master stations simultaneously attempt to control data transmission which detect the voltage level at the data terminal and which cause the master station which contains said means for establishing priority to cease attempted control of data transmission by allowing the data terminal and the clock terminal to assume the second voltage level for at least a predetermined interval after detection of the first voltage level during a clock interval in which that master station has allowed the data terminal to assume the second voltage level";

(Col. 11, lines 46-58; *see also* Claims 1-2, 13-14, 22; Figure 6; Col. 7, line 49; Def. Br. at 20; Pl. Br. at 45-46)

"means which detect the voltage level at the clock terminal and which cause the time slot generator to start the first interval whenever the voltage level at the clock terminal changes from the second voltage level to the first voltage level;

(Col. 12, lines 61-65; *see also* Claims 5, 14; Col. 5, lines 60 through Col. 6, line 28; Def. Br. at 23-24; Pl. Br. at 44)

"means which send an acknowledge bit which directly follows said bit cell sequence."

(Col. 20, lines 56-57; *see also* Claims 34-35; Def. Br. at 56; Pl. Br. at 51-51)

"means [ ] further forming a modified signal for the clock bus under the control of said end signal"

(Col. 18, lines 39-41; *see also* Claim 23; Figure 1; Def. Br. at 40; Pl. Br. at 60)

"means which generate a clock pulse at the clock terminal which has the second logic value in each bit cell"

(Col. 19, lines 18-20; *see also* Claim 29; Def. Br. 40-41; Pl. Br. 39-40, 46, 48)

Corresponding Control Unit Structure

The structure that is disclosed in the written description of the patent is a "corresponding structure" if the written description or the prosecution history clearly links it to a function recited in a claim element. B. Braun Medical, Inc. v. Abbott Laboratories, 124 F.3d 1419, 1424 (Fed.Cir.1997). Corresponding structure may include more than just the preferred structure. Micro Chem., Inc. v. Great Plains Chem. Co., Inc., 194 F.3d 1250, 1258 (Fed.Cir.1999). Where multiple alternative structures are disclosed, the claim is generally read to include them all. *Id*. (citing Serrano v. Telular Corp., 111 F.3d 1578, 1583 (Fed.Cir.1997)). Corresponding structure to a function set forth in a means-plus-function element must actually perform the recited function, not merely enable the pertinent structure to operate as intended. Asyst Technologies, Inc. v. Empak, Inc., 268 F.3d 1364, 1371 (Fed.Cir.2001).

A structure that does not perform the recited function does not constitute a corresponding structure and does not, thus, serve as limitation of the claim element. Northrop Grumman Corp. v. Intel Corp., 325 F.3d 1346, 1352 (Fed.Cir.2003) (citations omitted). Claims must be interpreted in light of the specification, but "limitations from the specification are not to be read into the claims." Teleflex, 299 F.3d at 1326; *accord* Renishaw, 158 F.3d at 1248-50. Additionally, "the number of embodiments disclosed in the specification is not determinative of the meaning of disputed claim terms" and consequently should not be construed as a limitation on those terms. Teleflex, 299 F.3d at 1327; *accord* CCS Fitness, 288 F.3d at 1366 (Fed.Cir.2002).

Here, the parties agree that Figure 1 and Figure 7 include a control unit as part of their illustrations-Figure 1 as units 36 and 38, and Figure 7 as clock control element 116 and data control element 134. Figure 1 of the '740 patent illustrates the connectivity of two stations to a shared clock wire and a shared data wire. Both stations have a control unit, two signal receivers, a clock transistor, and a data transistor. (Figure 1; Col. 3, lines 18-24)

The specification describes the computer system to which it relates in the following passage:

The invention relates to a computer system, comprising a first number of stations which are interconnected by a two-wire line which includes a data wire for transporting a series of data bits, and a clock wire which transports a synchronizing clock signal in parallel with each data bit between at least one transmitting station and at least one receiving station. The stations may be of different types: they may be microcomputers with a data processing function, but they also may be also (error in original) input/output processors, function generators, memories, input/output equipment such as keyboards or displays, or sensors for physical and/or chemical quantities. A system of the described kind is known from U.S. Pat. No. 3,889,236.

(Col. 1, lines 7-20)

The specification links the control unit depicted in Figure 1 to its role in switching the clock transistors and the data transistors ON and OFF in the following passages, when read together:

FIG. 1 shows diagrammatically the connection of two stations to a clock wire 20 and a data wire 22. Two stations, 32, 34 each comprise two signal receivers 40, 42, 44, 46 for example amplifiers having a high input impedance. The stations furthermore comprise transistors 48, 50, 52, 54, for example MOS transistors. When one of these transistors becomes conductive, the relevant line (20, 22) assumes a low potential.

(Col. 3, lines 18-26)

The stations 32, 34 also comprise units 36, 38 which notably form the data source and the data destination for the two-wire line. The output signals thereof control the conducting and blocking of the transistors 48, 50, 52, 54. (A station will be described in more detail with reference to FIG. 7.)

(Col. 3, lines 35-41)

The specification links the changes in the voltage levels on the clock bus and the data bus to the sending of clock signals, the sending of start signals, the sending of stop signals, and the transmission of data in the following passages, when read together:

The stations are interconnected by a clock bus and a data bus. Each of the buses operates to form a wired logic function between the stations.

(Col. 1, lines 42-45)

Thus, each of the buses includes means (for example a pull-up resistor) which urges the bus toward a second voltage state in the absence of a forcing input from one of the stations. Each of the master stations includes means for producing a periodic clock signal on the clock bus by allowing the bus to assume the second voltage level during periodic clock pulse intervals and by forcing the bus to a first voltage level at all other times during production of the clock signal.

(Col. 1, lines 45-54)

the stations further comprise means for transmitting binary data by forcing the voltage on the data bus to the first voltage level during an entire clock pulse interval to transmit a first data value and by allowing the voltage on the data bus to assume the second voltage level during an entire clock pulse interval to transmit a second data value.

(Col. 1, lines 54-60)

Master stations further comprise means for producing a start signal, which indicates that the station is prepared to control data transmission, by forcing a transition of the voltage level on the data bus from the second voltage level to the first voltage level during a clock pulse interval and means for producing a stop signal which indicates that the station has finished controlling data transmission by forcing the voltage level on the data bus to the first voltage level during a first fraction of a clock pulse interval and then allowing the voltage on the data bus to transition to the second voltage level during the clock pulse interval.

(Col. 1, lines 60 through Col. 2 lines 1-4)

Figure 7 of the '740 patent contains a diagram of a station, at the register level, "in so far as it concerns the operation of the two-wire bus line." (Col 7, lines 25-26) The specification specifically notes that the station illustrated in Figure 7 is "suitable for incorporation in a microcomputer" and that the "other parts of the microcomputer have been omitted for the sake of simplicity.

(Col. 7, lines 26-29)

The specification links the functions in a specific station, like that depicted in Figure 7, with that station's microcomputer in the following passages:

The internal clock of the microcomputer is connected to input 100.

(Col. 7, lines 29-30)

The register 102 can receive a write control signal WRS1 and a read control signal RDS1 which are formed elsewhere in the computer. The register 104 is filled under the control of a write control signal WRS2 which is also formed elsewhere in the microcomputer.

(Col. 7, lines 39-44)

The signals are supplied by the central control system of the microcomputer. The data control element 134 also receives the signal ESO from the register 102. This signal controls an output line amplifier in the data control element 134 which is connected to the data wire. If ESO is zero, the station continuously generates a "1" signal for the data wire.

(Col. 9, lines 34-40)

Here, the determination of whether the corresponding structure that performs these functions is sufficiently identifiable is relatively simple because all of the evidence, both intrinsic and extrinsic, leads to the same conclusion. I start with the ordinary meaning of the words of the claim.FN4 Because the term "control" is at issue, I note that Webster's Ninth Collegiate Dictionary ("Webster's") defines the term "control" as "a mechanism used to regulate or guide the operation of a machine, apparatus, or system." (Webster's at 285, Plaintiff's Ex. E) The Comprehensive Dictionary of Electrical Engineering ("CDEE") defines the term "controller" as "a unit that directs the operation of a subsystem within a computer." (CDEE at 139, Plaintiff's Ex. F) Comparing the '740 patent to other patents issued between 1976 and 1980, the filing date of the '740 patent, I note that a significant number of patents describe control units similar to that described in the '740 patent. *See e.g.,* U.S. Pat. Nos. 4,020,472; 4,218,740. This evidence, which Atmel does not disagree with, is sufficient to determine the meaning of control unit and thus the clock control element and the data control element. Based thereon, I find that the control unit reflected in Figure 1 of the '740 patent and the clock control element and data control element reflected in figure 7 are sufficiently described to a person skilled in the art.FN5

FN4. There is no indication in the claims or the specifications that the inventors intended the term "control" to have any meaning other than it ordinary meaning.

FN5. As is clear from the language of the claim ("means for producing ...") and contrary to Defendant's argument, the '740 patent does not seek to incorporate the signals referred to as corresponding structure of, for example, control unit 36. *See* Northrup, 325 F.3d at 1352. Rather, the claims of the '740 patent concern methods and apparatuses *for producing* certain combinations of signals.

Even if it were necessary to resort to the testimonial evidence, the Clark and Reed submissions explain persuasively that the term "control unit" was a structure known to those skilled in the art in 1980. (*See, e.g.,* Clark Report, pp. 27-41, Plaintiff's Ex. G; Clark Dec., para.para. 45-54, Plaintiff's Ex. H; Clark Tr., pp 48-52, Plaintiff's Ex. I; Reed Report, pp. 12-22, Plaintiff's Ex. J; Reed Tr., pp 239-247, 252, Plaintiff's Ex. K). Defendants' expert is not to the contrary. Dr. Rhyne agreed that "a person of skill in the art at that time [of the filing of the '740 patent] ... could make [the] control circuitry" described in box 36. (Rhyne Tr. pp 98-99, Plaintiff's Ex. L). Indeed, he went on to testify that he "had taught probably hundreds of students at [that] point as to exactly how to do that...." (Id. at 99)

Accordingly, based on all the evidence, I find that the control units, as illustrated in Figure 1 and otherwise described in the '740 patent in Figure 7, are sufficiently described such that a person ordinarily skilled in the art at the time could have identified them and constructed them and, accordingly, that the claims that rely upon them do not fail the requirements of 35 U.S.C. 112 para. 2. Because I so find, I decline Defendant's invitation to import the structure limitations from Figure 7 into the means-plus-function claims of the '740 patent.

"Forcing", "Allowing" and "Clock Pulse Interval"

As noted in the fact section above, the '740 patent claims a novel two-wire bus protocol with unique start and stop control signals. The terms "forcing", "allowing" and "clock pulse interval" appear in, for example, claims 16-18 and are used to describe, in part, the functions of transmitting a clock signal, transmitting a start signal, transmitting a stop signal and transmitting binary data.

The Defendant argues that two transitions are required to cause a periodic clock signal at the clock terminal, a low to high transition (allowing) and a high to low transition (forcing), and that without both there is no clock signal. (Def. Br. at 27.)

Defendant argues that the phrase "allowing ... to assume a second voltage level" must include the act of turning a transistor from ON to OFF and that the phrase "forcing ... to a first voltage level" must include the act of turning a transistor from OFF to ON. (Def. Br. at 26-27.) In other words, if a switch is already turned OFF, it must be turned ON and then OFF again to "allow." Similarly, they argue that if it is already ON, it must be turned OFF and then ON again to "force." Defendants, arguments are without merit.

At the outset, Defendants' proposed interpretation is inconsistent with the claim language itself. Claim 16 describes "allowing" and "forcing" as continuous acts which occur over a period of time-like holding down a doorbell buzzer for thirty seconds-not as instantaneous acts-like turning ON or OFF a light switch. For example, the step of "transmitting a clock signal" requires "allowing the clock terminal ... to assume a second voltage level during each of a series of periodic clock pulse intervals" and then "forcing ... to a first voltage level at all other times." Similarly, the steps of "transmitting a start signal" and "transmitting a stop signal" require allowing or forcing "during a first fraction of a clock pulse interval." Also, the step of "transmitting binary data" requires allowing or forcing "during an entire clock pulse interval." The act of switching ON-to-OFF, or OFF-to-ON, is not recited or relevant to the claim. In other words, there is nothing in the claim that requires a transistor that is in the OFF state to be switched ON and then OFF again to "allow" or the reverse-ON-OFF-ON-to "force."

Defendants' proposed "turning the switch" interpretation for "allowing" and "forcing" is also contrary to the patent specification. A basic tenet of claim construction is that "[t]he construction that stays true to the claim language and most naturally aligns with the patent's description of the invention will be, in the end, the correct construction." Renishaw PLC v. Marposs Societa' per Azioni, 158 F.3d 1243, 1250 (Fed.Cir.1998); see also Brookhill-Wilk 1, LLC v. Intuitive Surgical, Inc., 326 F.3d 1215, 1222 (Fed.Cir.2003) ("the intrinsic record must always be consulted to identify which of the different possible [ordinary] meanings is most consistent with the use of the words by the inventor"). Here, Defendants' interpretations conflict with not just one part of the '740 specification, by many.

For example, the start and stop signals described in the '740 patent are illustrated below:

Start and Stop Signals Shown in the '740 Patent

TABULAR OR GRAPHIC MATERIAL SET AT THIS POINT IS NOT DISPLAYABLE
If the Defendants' "changing the switch" interpretation were adopted, the start and the stop signals would look as follows: FN6

FN6. See Defendants' slide numbers 31 (start) and 30 (stop), presented during the May 30, 2003 tutorial. (Exhibit B, pp. 30-31.)

TABULAR OR GRAPHIC MATERIAL SET AT THIS POINT IS NOT DISPLAYABLE
TABULAR OR GRAPHIC MATERIAL SET AT THIS POINT IS NOT DISPLAYABLE
According to the Defendants' interpretation, a composite start signal, two-bit data transmission, and stop signal would appear as follows:

TABULAR OR GRAPHIC MATERIAL SET AT THIS POINT IS NOT DISPLAYABLE
The stark contrast between the signals illustrated in Figure 3 of the '740 patent and those presented by Defendants confirms that the latter interpretation is not correct. The specification contains other descriptions that conflict with Defendants' interpretation. (*E.g.,* '740 patent, Col. 1, line 48; Col. 2, line 8; Col. 3, lines 15-50.)

The plain meaning of the phrase "allowing ... to assume a second voltage level" requires only that the transistor be turned OFF, or kept turned OFF (*i.e.,* kept in a nonconducting state), so that the voltage stays

at a high ("1") logic level for the relevant time period. Similarly, the plain meaning of the phrase "forcing ... to a first voltage level" requires only that the transistor be turned ON, or kept turned ON (*i.e.,* kept in a conducting state), so that the voltage is held at a low ("0") logic level for the relevant time period. When those definitions are applied consistently to the patent claims, they correspond exactly to the clock, start, stop, and data signals shown in Figures 2 and 3 of the '740 patent. (*See* figures on pp. 30, 32, 34, and 36 of Pl. Br.) FN7 Accordingly, Philips' proposed interpretations for the "allowing" and "forcing" elements are the proper constructions to be followed.

FN7. Defendants' argument that Philips' proposed claim construction is in some way "inconsistent" is without merit. (Def. Br. at 28-30.) Philips' interpretations are entirely consistent as demonstrated by, *inter alia,* the "allowing" and "forcing" illustrations in Philips' opening brief.

Clock Pulse Interval

The parties agree that a "clock pulse interval" is the time interval during which the signal on the clock bus is high (logic "1"), including the rising and falling edges. However, Defendants seek to add an additional limitation-that clock pulse intervals be "periodic," i.e., that all clock pulse intervals occur at regular intervals.FN8

FN8. The dictionary definition for "periodic" is: "occurring or recurring at regular intervals." (Webster's at 875, Exhibits in Support of U.S. Philips Corp.'s Reply Memorandum of Law on the Interpretation of the Asserted Claims of U.S. Patent No. 4,689,740 ("Reply Br. Ex."), Ex. C)

It is true that the '740 patent describes "periodic" clock pulse intervals. For example, "periodic" clock pulses are used when transmitting binary data. ('740 patent, Col. 4, lines 64-65.) However, the '740 patent also teaches that not all clock pulse intervals are "periodic." For example, the specification makes clear that the clock signal is only periodic between a start signal and a stop signal: "The master station only maintains the periodic nature of the clock signal between the start condition 60 and the stop condition 62." ('740 patent, Col. 4, lines 64-65.) After a stop signal, the bus is free and the associated clock pulse interval lasts for an indefinite, non-periodic length of time until the start of the next message: "The bus returns to the 'free' condition after the formation of the stop condition, block 62 on FIG. 3." ('740 patent, Col. 5, lines 46-48.) The claims reflect this basic truth. When a clock pulse interval is meant to be periodic, the claims recite "periodic clock pulse interval." At other times, it is referred to only as a "clock pulse interval," or a "fraction of a clock pulse interval." Thus, the patent expressly provides that the clock pulse interval is periodic at some times and not periodic at others, and there is no basis to construe "clock pulse interval" as always being periodic. Accordingly, I find Philips' construction to be correct.

A First Fraction Of A Clock Pulse Interval

Defendants also argue that "a first fraction of a clock pulse interval" must begin at the rising edge of the clock pulse interval. (Def. Br. at 31.) Again, Defendants' interpretation is unsupported by the claim language and '740 specification. The '740 patent describes the start signal as "a transition on the data wire from '1' to '0', while the signal on the clock wire [remains '1']." ('740 patent, Col. 4, lines 19-21.) Thus, the key requirement is that the signals on the clock and data wires must be high (or "1") for some fraction of time-a "first" fraction-before the transition on the data wire. After the transition on the data wire, the signal on the data wire must be low (or "0") for some fraction of time-a "second" fraction-while the clock wire remains high (or "1").

Those fractions of time are illustrated below on Figure 3 of the '740 patent:

TABULAR OR GRAPHIC MATERIAL SET AT THIS POINT IS NOT DISPLAYABLE
Thus, the term "first" does not refer to the beginning of a clock pulse interval." Instead, it refers to the first "fraction," that is, before another "fraction" in time. The dictionary definition for "first" is completely consistent with this interpretation: "1 a: before another in time, space, or importance b: for the first time 2: in preference to something else: SOONER." (Webster's at 466, Reply Br., Ex. D.)

Defendants' interpretation would require the clock to switch to low after each stop signal and then back to high before the next start signal. There is nothing in the claims or the '740 specification that would require this unnecessary switching. Indeed, the '740 patent describes the exact opposite-that after a stop signal, the clock and data wires remain high ("1") until the next start signal is issued. (*See, e.g.,* '740 patent, Col. 4, lines 64-66.) Thus, Defendants' interpretation is incorrect, because it would exclude this preferred embodiment of a clock pulse. *See, e.g.,* Burke Inc. v. Bruno Indep. Living Aids Inc., 183 F.3d 1334, 1341 (Fed.Cir.1999) ("The district court's claim interpretation [ ] would exclude the preferred embodiment described in the specification and, thus, cannot be sustained."); Johns Hopkins Univ. v. Cellpro Inc., 152 F.3d 1342, 1355 (Fed.Cir.1998). Accordingly, I find Philips' construction to be correct.

Conclusion

The interpretation of the asserted claims of U.S. Patent No. 4,689,740 is as set out above is SO ORDERED.

S.D.N.Y.,2004.
U.S. Philips Corp. v. Atmel Corp.