United States District Court,
D. New Jersey.

MOSAID TECHNOLOGIES INCORPORATED,
Plaintiff.
v.
SAMSUNG ELECTRONICS CO., LTD., Samsung Electronics America, Inc., Samsung Semiconductor, Inc., and Samsung Austin Semiconductor, L.P,
Defendants.
Infineon Technologies North America Corp,
Plaintiff.
v.
Mosaid Technologies Incorporated,
Defendant.
Mosaid Technologies Incorporated,
Counterclaimant.
v.
Infineon Technologies North America Corp., Infineon Technologies AG, Infineon Technologies Holding North America Corp., and Infineon Technologies Richmond LLP,
Counterdefendants.

Nos. 01-CV-4340 (WJM), 03-CV-4698 (WJM)

March 22, 2004.

ORDER

WILLIAM J. MARTINI**, District Judge.**

This matter having come before the Court to establish the meaning of disputed terms contained in U.S. Patent Nos. 5,214,602, 5,751,643, 5,822,253, 6,278,640, 6,603,703 B2, 5,828,620, 6,055,201, 6,236,581 B1 and 6,580,654 B2; and the parties having presented exhibits, briefs and arguments; and the Court having set forth the reasons for its interpretations in an accompanying opinion,

IT IS on this 23rd day of March, 2004 hereby,

ORDERED that the disputed claim terms shall have the following meanings:

1. "V_{dd}" means "the substantially constant positive source-drain supply voltage in a MOS circuit."

2. "means for applying" is a means-plus-function limitation. Its function is "applying the V_{pp} supply voltage level directly to the word line through the source-drain circuit of an FET." Its corresponding structure includes "level shifter 6 and transistor 14A or level shifter 6, transistor 14A and a secondary decoder."

Further, the patentee disclaimed the use of a double bootstrapping circuit and a capacitor boosting circuit.

3. "applying circuitry" means "circuitry that applies without using a double bootstrapping circuit or a capacitor boosting circuit ."

4. "applying the controlled high voltage V_{pp} to the word line" means "putting on the controlled voltage V_{pp} to the word line through the source drain circuit of a pass FET without using a double bootstrapping circuit or a capacitor boosting circuit."

5. "from one of the latched, level shifted control signals applying a controlled high voltage, from the controlled high voltage supply, to a selected word line" means "to put on a controlled high voltage, from the controlled high voltage supply, to a selected word line without using a double bootstrapping circuit or a capacitor boosting circuit."

6. "from one of the latched, level shifted control signals applying a controlled high voltage greater than the stored voltage to a selected word line" means "to put on a controlled high voltage greater than the stored voltage to a selected word line without using a double bootstrapping circuit or a capacitor boosting circuit."

7. "from the latched, level shifted controls signals, applying a controlled voltage to the selected word line" means "to put on a controlled voltage to the selected word line without using a double bootstrapping circuit or a capacitor boosting circuit."

8. "applies the controlled high voltage V_{pp} from the high voltage supply to a word line" means "to put on the controlled high voltage V_{pp} from the high voltage supply to a word line without using a double bootstrapping circuit or a capacitor boosting circuit."

9. "V_{pp}" means "a substantially constant high supply voltage at or higher than V_{dd} plus a transistor threshold voltage."

10. "directly" means "without any intervening circuitry."

11. "connected" and "coupled" mean "directly united, joined, or linked together."

12. "means for receiving" is indefinite. As a result, the Court finds that claims 2, 3 and 4 of U.S. Patent No. 5,214,602 ("the '602 patent") are invalid as indefinite pursuant to 35 U.S .C. s. 112 para.para. 2 and 6.

13. "level shifter driving means" is indefinite. As a result, the Court finds that claims 3 and 4 of the '602 patent are invalid as indefinite pursuant to 35 U.S.C. s. 112 para.para. 2 and 6.

14. "word line driver circuit" means "a circuit that applies a driving input voltage to a single word line or a group of word lines ."

15. "word line selection signals" means "signals derived from address information that select a single word line or a group of word lines."

16. "select signals" means "signals derived from address information that select a single word line or a group

of word lines."

17. "word line control signals" means "signals used to control the application of a voltage to a single word line or a group of word lines."

18. "control signals" means "signals used to control the application of a voltage to a single word line or a group of word lines."

19. "latching level shifter" means "a level shifter including a feedback loop that will indefinitely retain at least one data state in the absence of any new control signal to change the state."

20. "level shifter with latching" means "a level shifter including a feedback loop that will indefinitely retain at least one data state in the absence of any new control signal to change the state."

21. "latching the level shifted control signals" means "using a feedback loop to store and retain the boosted states of the control signals."

22. "to ... latch" means "to indefinitely retain at least one data state with a feedback loop in the absence of any new control signal to change the state."

23. "DC voltage supply" means "a supply that provides two or more substantially constant output voltages."

24. "switching circuit alternately connecting" means "alternately connecting the first terminal of the boosting capacitor at one time to the voltage supply and at a different time to the capacitive load."

25. "alternately switching" means "alternately switching the first terminal of the boosting capacitor at one time to the voltage supply and at a different time to the capacitive load."

26. "switching circuit ... alternating the level" means "alternately connecting the second terminal of the boosting capacitor at one time to a low level of the DC voltage supply and at a different time to a high level of the DC voltage supply without the use of clock sources to charge the boosting capacitor."

27. "correct level required to turn on a selected memory cell access transistor" means "a voltage level sufficient to fully turn on a memory cell access transistor but not so high that it will damage the transistor."

28. "decoder circuit" means "a circuit that decodes word line address information and supplies the regulated boosted voltage to the word line without using double bootstrapping."

29. "word line decoder" means "a circuit that decodes word line address information and supplies the regulated boosted voltage to the word line without using double bootstrapping."

30. "switching means" is a means-plus-function limitation. Its functions are: "1) alternately connecting the first terminal of the boosting capacitor to the voltage supply and to the capacitive load; and 2) alternating the level of the voltage supply connected to the second terminal of the boosting capacitor." Its corresponding structure includes: "1) transistors 23 and 24; and 2) transistors 25 and 26."

IT IS FURTHER ORDERED that the agreed upon claim terms shall have the following meanings:

31. "high V_{pp} supply voltage source" means "a circuit that generates V_{pp}."

32. "controlled high voltage V_{pp} supply" means "a circuit that generates V_{pp}."

33. "controlled high voltage supply" means "a circuit that generates a substantially constant high supply voltage."

34. "a high voltage supply which supplies a controlled high voltage V_{PP}" means "a circuit that generates V_{pp}."

35. "a voltage supply which supplies a controlled voltage" means "a circuit that generates a substantially constant supply voltage."

36. "V_{dd} logic levels" means "logic levels in which the high level is V_{dd}."

37. "V_{pp} logic levels" means "logic levels in which the high level is V_{pp}."

38. "decoding address signals" means "producing output signals based on input address signals."

39. "switch" means "a device for making, breaking, or changing the connection of a circuit, but not a transistor introducing a threshold voltage drop or a transistor configured as a diode."

40. "boosted clock signal" means "a clock signal that has been boosted above the high level of the DC voltage supply."

41. "boosted voltage level" means "a voltage level that has been boosted above the high level of the DC voltage supply."

42. "unregulated boosted voltage" means "a boosted voltage level that is not controlled."

43. "level shifter" means "a circuit that accepts digital input signals at one pair of voltage levels and delivers output signals at a different pair of voltage levels, where at least one of those voltage levels changes."

44. "control signals being set and reset" means "control signals being placed in a zero or one state by only V_{dd} level signals."

45. "dynamic random access memory" means "a dynamic form of random access memory that uses, as its memory storage elements, capacitors that are built into the integrated circuit; the data stored on the capacitors requiring periodic refreshing."

46. "random access memory" means "a memory that permits access to any of its address locations in any desired sequence with similar access time to each location."

47. "means for selecting" is a means-plus-function claim limitation. Its function is "selecting the word line." Its structure is "NAND gate 5."

48. "high logic level voltage V_{dd} bit charge storage capacitor" means "a bit charge storage capacitor that stores a high logic level voltage V_{dd}."

49. "transistor threshold voltage/threshold voltage" means "the minimum voltage between the gate and source of a MOS transistor at which the channel begins to conduct current."

50. "P-channel FET/p-channel transistor" means "a field effect transistor where source and drain are regions of p-type conductivity, and holes are used to conduct current in the channel region."

51. "N-channel FET/n-channel transistor" means "a field effect transistor where source and drain are regions of n-type conductivity, and electrons are used to conduct current in the channel region."

52. "transistor damaging voltage" means "a voltage that instantaneously causes the gate oxide to rupture."

D.N.J.,2004.
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